

HD74AC112/HD74ACT112

Dual JK Negative Edge-Triggered Flip-Flop

REJ03D0244-0200Z
(Previous ADE-205-364 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC112/HD74ACT112 features individual J, K, Clock and asynchronous Set and Clear inputs to each flip-flop. When the clock goes High, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may change when the clock is High and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Features

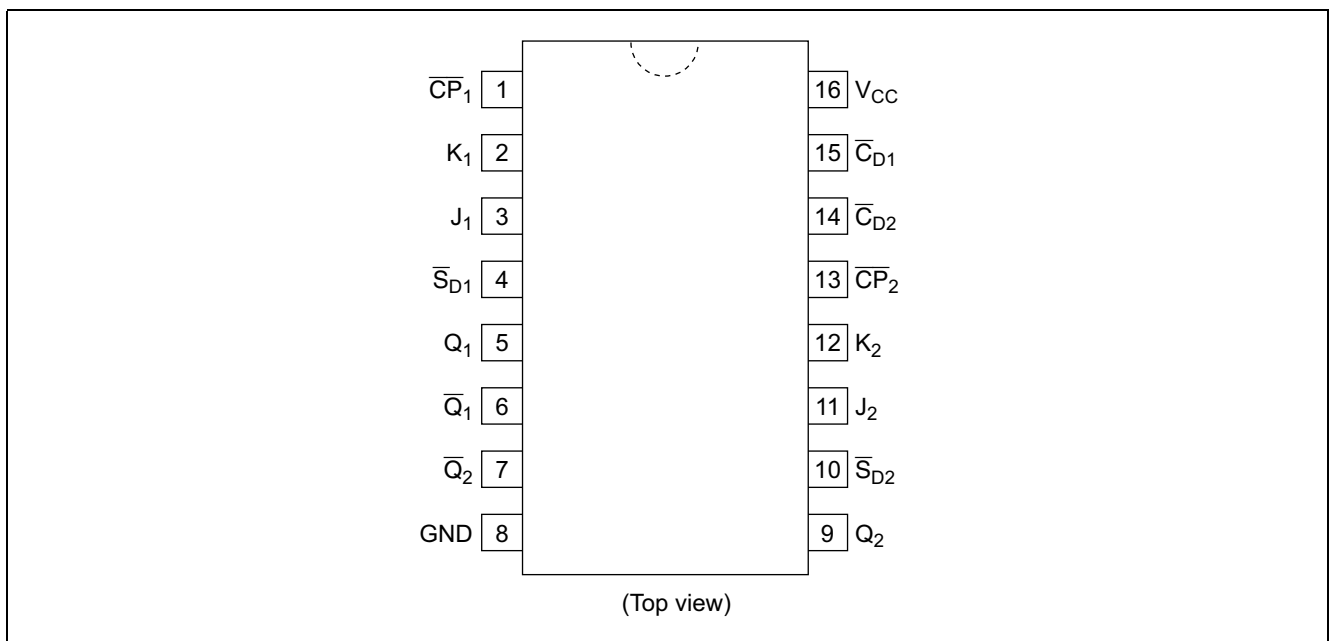
- Outputs Source/Sink 24 mA
- HD74ACT112 has TTL-Compatible Inputs
- Ordering Information: Ex. HD74AC112

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC112FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC112RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

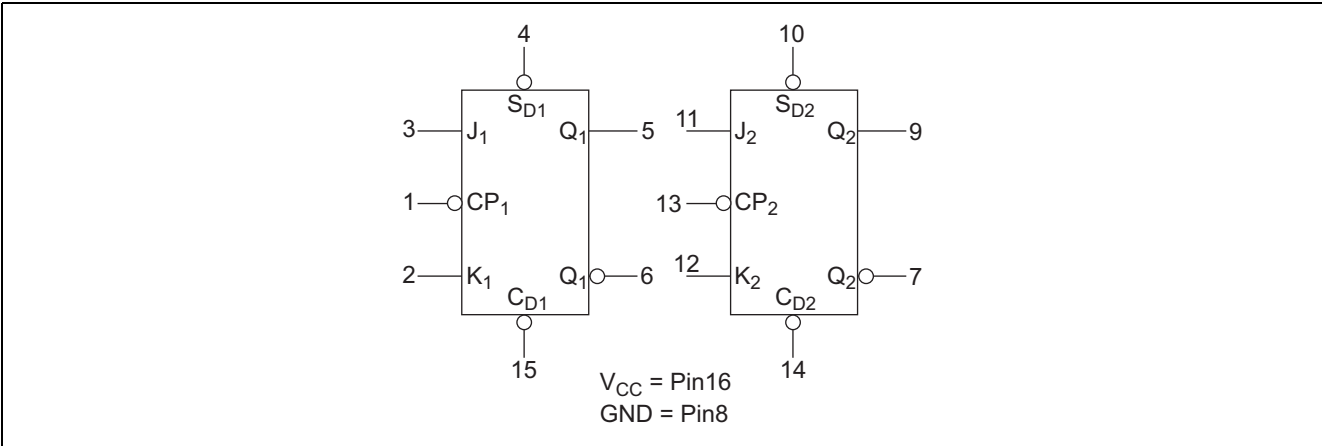
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol



Pin Names

- J_1, J_2, K_1, K_2 Data Inputs
- $\overline{CP}_1, \overline{CP}_2$ Clock Pulse Inputs (Active Falling Edge)
- $\overline{C}_{D1}, \overline{C}_{D2}$ Direct Clear Inputs (Active Low)
- $\overline{S}_{D1}, \overline{S}_{D2}$ Direct Set Inputs (Active Low)
- $Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$ Outputs

Asynchronous Inputs:

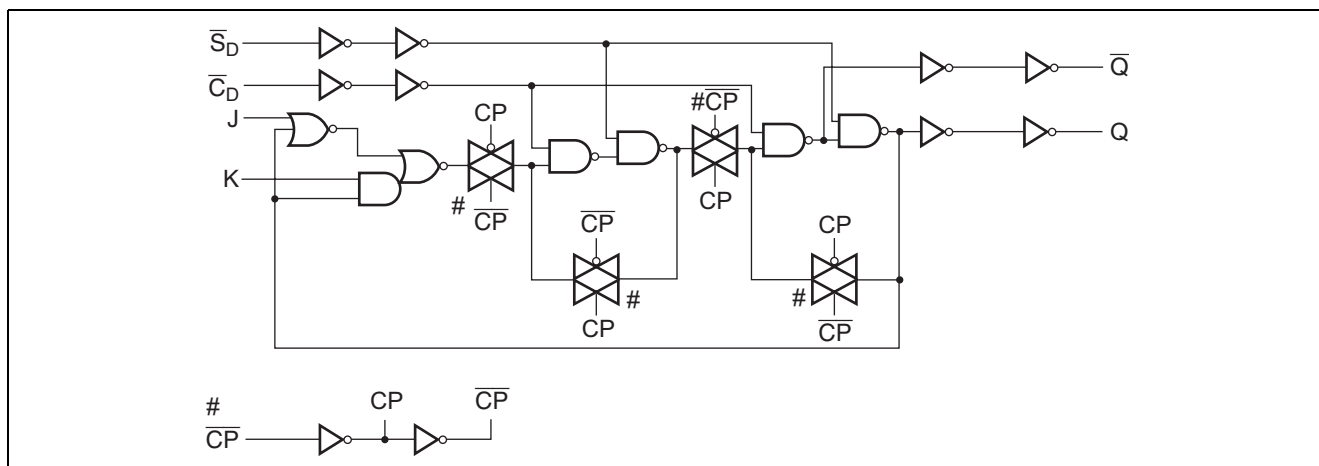
- Low input to $\overline{S}_D$ sets Q to High level
- Low input to $\overline{C}_D$ sets Q to Low level
- Clear and Set are independent of clock
- Simultaneous Low on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ High

Truth Table

Inputs		Outputs
@ t_n		@ t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}_n$

- t_n : Bit time before clock pulse.
- t_{n+1} : Bit time after clock pulse.
- H : High Voltage Level
- L : Low Voltage Level

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	-0.5 to 7	V	
DC input diode current	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	V_I	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	I_{OK}	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	V_O	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	I_O	± 50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	± 50	mA	
Storage temperature	Tstg	-65 to +150	$^{\circ}C$	

Recommended Operating Conditions: HD74AC112

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	$^{\circ}C$	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	t_r, t_f	8	ns/V	$V_{CC} = 3.0V$
				$V_{CC} = 4.5 V$
				$V_{CC} = 5.5 V$

DC Characteristics: HD74AC112

Item	Sym- bol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Condition
			min.	typ.	max.	min.	max.		
Input Voltage	V _{IH}	3.0	2.1	1.5	—	2.1	—	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	3.15	2.25	—	3.15	—		
		5.5	3.85	2.75	—	3.85	—		
	V _{IL}	3.0	—	1.50	0.9	—	0.9		V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	—	2.25	1.35	—	1.35		
		5.5	—	2.75	1.65	—	1.65		
Output voltage	V _{OH}	3.0	2.9	2.99	—	2.9	—	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 µA
		4.5	4.4	4.49	—	4.4	—		
		5.5	5.4	5.49	—	5.4	—		
		3.0	2.58	—	—	2.48	—		V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA
		4.5	3.94	—	—	3.80	—		
		5.5	4.94	—	—	4.80	—		
	V _{OL}	3.0	—	0.002	0.1	—	0.1		V _{IN} = V _{IL} or V _{IH} I _{OUT} = 50 µA
		4.5	—	0.001	0.1	—	0.1		
		5.5	—	0.001	0.1	—	0.1		
		3.0	—	—	0.32	—	0.37		V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA
		4.5	—	—	0.32	—	0.37		
		5.5	—	—	0.32	—	0.37		
									I _{OL} = 24 mA
									I _{OL} = 24 mA
Input leakage current	I _{IN}	5.5	—	—	±0.1	—	±1.0	µA	V _{IN} = V _{CC} or GND
Dynamic output current*	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} = 1.1 V
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} = 3.85 V
Quiescent supply current	I _{CC}	5.5	—	—	4.0	—	40	µA	V _{IN} = V _{CC} or ground

*Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions: HD74ACT112

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V _{CC}	2 to 6	V	
Input and output voltage	V _I , V _O	0 to V _{CC}	V	
Operating temperature	Ta	-40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V _{IN} 0.8 to 2.0 V	tr, tf	8	ns/V	V _{CC} = 4.5V V _{CC} = 5.5V

DC Characteristics: HD74ACT112

Item	Sym- bol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Condition			
			min.	typ.	max.	min.	max.					
Input voltage	V _{IH}	4.5	2.0	1.5	—	2.0	—	V	V _{OUT} = 0.1 V or V _{CC} -0.1 V			
		5.5	2.0	1.5	—	2.0	—					
	V _{IL}	4.5	—	1.5	0.8	—	0.8		V _{OUT} = 0.1 V or V _{CC} -0.1 V			
		5.5	—	1.5	0.8	—	0.8					
Output voltage	V _{OH}	4.5	4.4	4.49	—	4.4	—	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 µA			
		5.5	5.4	5.49	—	5.4	—					
		4.5	3.94	—	—	3.80	—		V _{IN} = V _{IL}	I _{OH} = -24 mA		
		5.5	4.94	—	—	4.80	—			I _{OH} = -24 mA		
	V _{OL}	4.5	—	0.001	0.1	—	0.1		V _{IN} = V _{IL} or V _{IH} I _{OUT} = 50 µA			
		5.5	—	0.001	0.1	—	0.1					
		4.5	—	—	0.32	—	0.37		V _{IN} = V _{IL}	I _{OL} = 24 mA		
		5.5	—	—	0.32	—	0.37			I _{OL} = 24 mA		
	Input current	I _{IN}	5.5	—	—	±0.1	—		±1.0	µA	V _{IN} = V _{CC} or GND	
	I _{CC} /input current	I _{CCT}	5.5	—	0.6	—	—		1.5	mA	V _{IN} = V _{CC} -2.1 V	
Dynamic output current*	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} = 1.1 V			
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} = 3.85 V			
Quiescent supply current	I _{CC}	5.5	—	—	4.0	—	40	µA	V _{IN} = V _{CC} or ground			

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC112

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	125	—	—	100	—	MHz
		5.0	150	—	—	125	—	
Propagation delay C _P to Q or Q̄	t _{PLH}	3.3	1.0	11.0	14.0	1.0	15.0	ns
		5.0	1.0	8.5	11.0	1.0	12.0	
Propagation delay C _P to Q or Q̄	t _{PHL}	3.3	1.0	11.0	14.0	1.0	15.0	
		5.0	1.0	8.5	11.0	1.0	12.0	
Propagation delay C _D , S _D to Q or Q̄	t _{PLH}	3.3	1.0	9.5	12.5	1.0	13.5	
		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay C _D , S _D to Q or Q̄	t _{PHL}	3.3	1.0	11.5	14.5	1.0	15.5	
		5.0	1.0	9.0	11.0	1.0	12.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC112

Item	Symbol	V_{CC} (V)*1	Ta = +25°C CL = 50 pF		Ta = −40°C to +85°C CL = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time J or K to $\overline{C_P}$	t_{su}	3.3	3.0	5.5	6.0	ns
		5.0	2.0	4.5	4.5	
Hold time $\overline{C_P}$ to J or K	t_h	3.3	−1.5	0.0	0.0	
		5.0	−0.5	0.0	0.0	
Pulse width $\overline{C_P}$ or $\overline{C_D}$ or $\overline{S_D}$	t_w	3.3	2.0	5.5	7.0	
		5.0	2.0	4.5	5.0	
Recovery time $\overline{C_D}$ or $\overline{S_D}$ to $\overline{C_P}$	t_{rec}	3.3	1.5	3.5	3.5	
		5.0	1.0	3.0	3.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT112

Item	Symbol	$V_{CC} (V)^{*1}$	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	5.0	100	—	—	80	—	MHz
Propagation delay $\overline{C_P}$ to Q or $\overline{Q}$	t_{PLH}	5.0	1.0	10.5	13.0	1.0	14.0	ns
Propagation delay $\overline{C_P}$ to Q or $\overline{Q}$	t_{PHL}	5.0	1.0	10.5	13.0	1.0	14.0	
Propagation delay $\overline{C_D}$, $\overline{S_D}$ to Q or $\overline{Q}$	t_{PLH}	5.0	1.0	8.0	10.0	1.0	11.0	
Propagation delay $\overline{C_D}$, $\overline{S_D}$ to Q or $\overline{Q}$	t_{PHL}	5.0	1.0	10.5	12.5	1.0	13.5	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT112

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = −40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time J or K to $\overline{C}_P$	t _{SU}	5.0	2.5	7.0	8.0	ns
Hold time $\overline{C}_P$ to J or K	t _H	5.0	0.0	1.5	1.5	
Pulse width $\overline{C}_P$ or $\overline{C}_D$ or $\overline{S}_D$	t _W	5.0	4.5	7.0	8.0	
Recovery time $\overline{C}_D$, $\overline{S}_D$ to $\overline{C}_P$	t _{REC}	5.0	−2.5	3.0	3.0	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

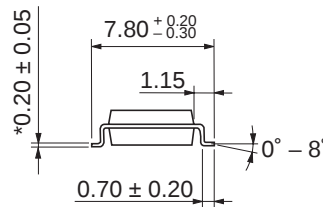
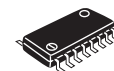
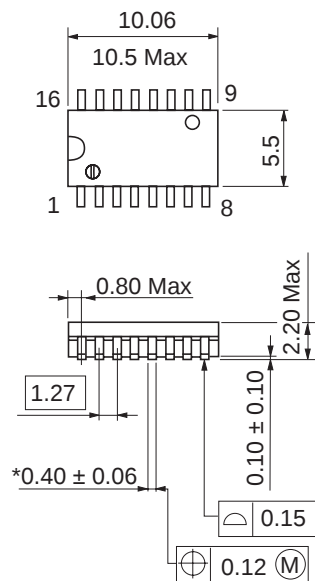
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 V$
Power dissipation capacitance	C_{PD}	35.0	pF	$V_{CC} = 5.0 V$

Package Dimensions

As of January, 2003

Unit: mm

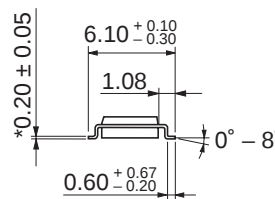
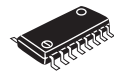
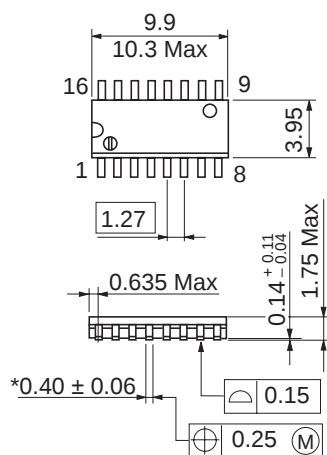


*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001