

74HC4024-Q100

7-stage binary ripple counter

Rev. 3 — 16 February 2024

Product data sheet

1. General description

The 74HC4024-Q100 is a 7-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q0 to Q6). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- CMOS input levels
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

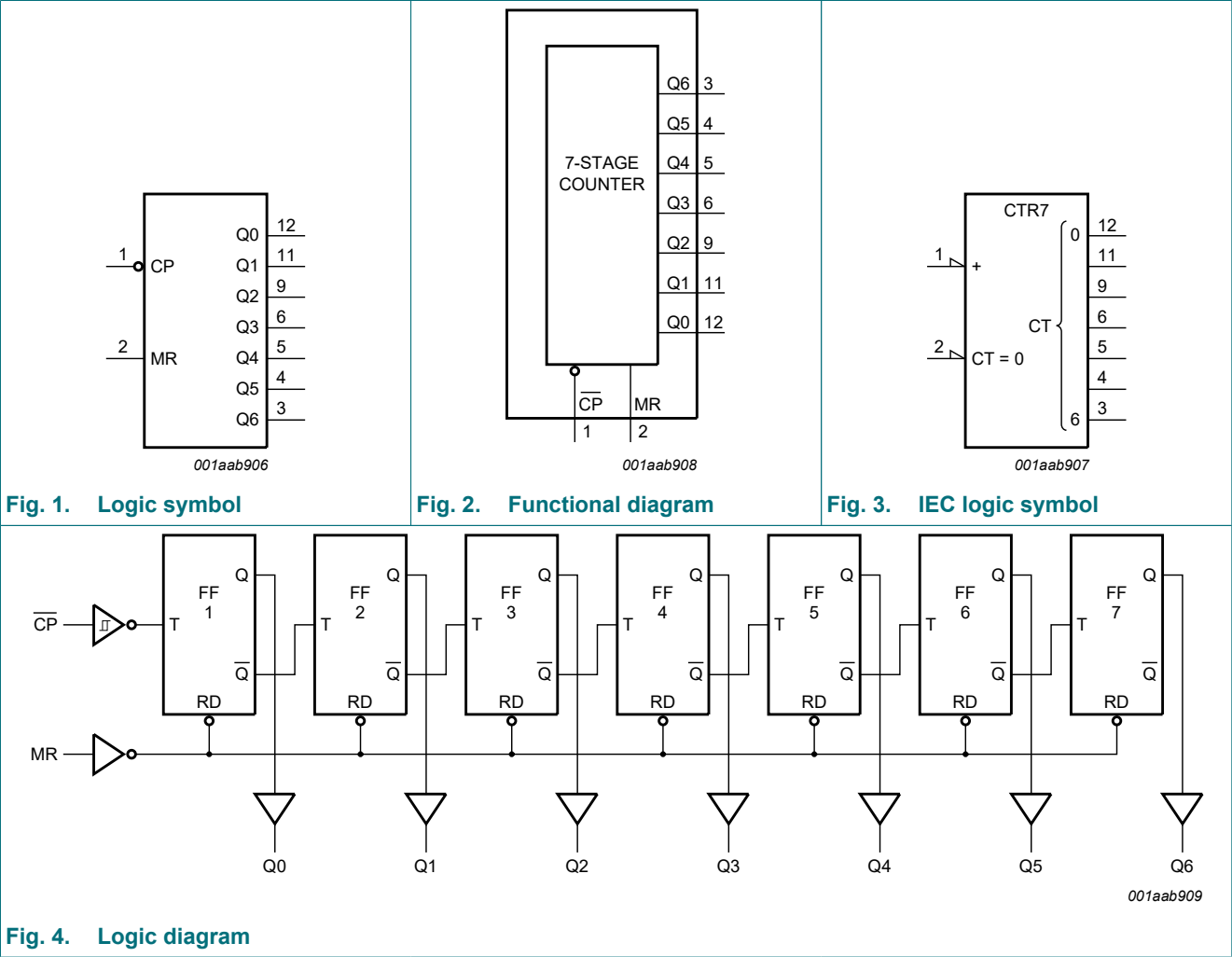
- Frequency dividing circuits
- Time delay circuits.

4. Ordering information

Table 1. Ordering information

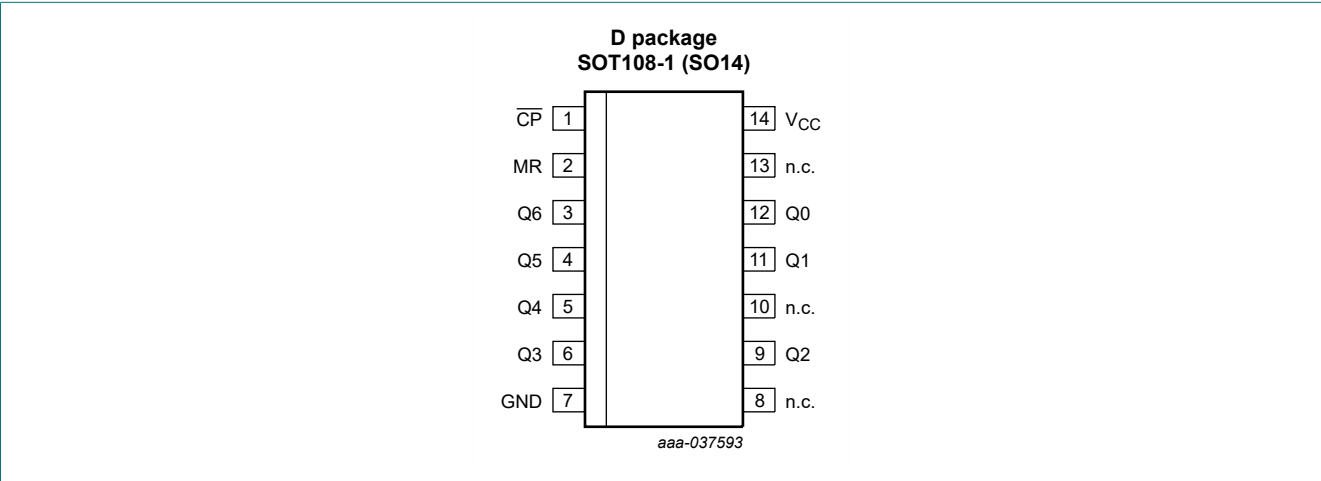
Type number	Package			
	Temperature range	Name	Description	Version
74HC4024D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
CP	1	clock input (HIGH-to-LOW, edge-triggered)
MR	2	master reset input (active HIGH)
Q6, Q5, Q4, Q3, Q2, Q2, Q1, Q0	3, 4, 5, 6, 9, 11, 12	parallel output
GND	7	ground (0 V)
n.c.	8, 10, 13	not connected
V _{CC}	14	positive supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition;
↓ = HIGH-to-LOW clock transition.

Input		Output
MR	CP	Qn
H	X	L
L	↑	no change
	↓	count

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	ns/V
		V _{CC} = 4.5 V	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	ns/V
T _{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	µA
C _I	input capacitance		-	3.5	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.84	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.34	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	µA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	µA

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = 25 °C						
t _{pd}	propagation delay	$\overline{CP}$ to Q0; see Fig. 5 [1]				
		V _{CC} = 2.0 V	-	47	175	ns
		V _{CC} = 4.5 V	-	17	35	ns
		V _{CC} = 6.0 V	-	14	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	14	-	ns
		Qn to Qn+1; see Fig. 5 [1]				
		V _{CC} = 2.0 V	-	25	80	ns
		V _{CC} = 4.5 V	-	9	16	ns
		V _{CC} = 6.0 V	-	7	14	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Q0; see Fig. 5				
		V _{CC} = 2.0 V	-	63	200	ns
		V _{CC} = 4.5 V	-	23	40	ns
		V _{CC} = 6.0 V	-	18	34	ns
t _t	transition time	see Fig. 5 [2]				
		V _{CC} = 2.0 V	-	19	75	ns
		V _{CC} = 4.5 V	-	7	15	ns
		V _{CC} = 6.0 V	-	6	13	ns
t _W	pulse width	$\overline{CP}$ HIGH or LOW; see Fig. 5				
		V _{CC} = 2.0 V	80	17	-	ns
		V _{CC} = 4.5 V	16	6	-	ns
		V _{CC} = 6.0 V	14	5	-	ns
		MR HIGH; see Fig. 5				
		V _{CC} = 2.0 V	80	22	-	ns
		V _{CC} = 4.5 V	16	8	-	ns
		V _{CC} = 6.0 V	14	6	-	ns
t _{rec}	recovery time	MR to $\overline{CP}$; see Fig. 5				
		V _{CC} = 2.0 V	50	6	-	ns
		V _{CC} = 4.5 V	10	2	-	ns
		V _{CC} = 6.0 V	9	2	-	ns
f _{max}	maximum frequency	CP; see Fig. 5				
		V _{CC} = 2.0 V	6.0	27	-	MHz
		V _{CC} = 4.5 V	30	82	-	MHz
		V _{CC} = 6.0 V	35	98	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	90	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} [3]	-	25	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
t _{pd}	propagation delay	$\overline{CP}$ to Q0; see Fig. 5 [1]				
		V _{CC} = 2.0 V	-	-	220	ns
		V _{CC} = 4.5 V	-	-	44	ns
		V _{CC} = 6.0 V	-	-	37	ns
		Qn to Qn+1; see Fig. 5 [1]				
		V _{CC} = 2.0 V	-	-	100	ns
		V _{CC} = 4.5 V	-	-	20	ns
		V _{CC} = 6.0 V	-	-	17	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Q0; see Fig. 5				
		V _{CC} = 2.0 V	-	-	250	ns
		V _{CC} = 4.5 V	-	-	50	ns
		V _{CC} = 6.0 V	-	-	43	ns
t _t	transition time	see Fig. 5 [2]				
		V _{CC} = 2.0 V	-	-	95	ns
		V _{CC} = 4.5 V	-	-	19	ns
		V _{CC} = 6.0 V	-	-	16	ns
t _w	pulse width	$\overline{CP}$ HIGH or LOW; see Fig. 5				
		V _{CC} = 2.0 V	100	-	-	ns
		V _{CC} = 4.5 V	20	-	-	ns
		V _{CC} = 6.0 V	17	-	-	ns
		MR HIGH; see Fig. 5				
		V _{CC} = 2.0 V	100	-	-	ns
		V _{CC} = 4.5 V	20	-	-	ns
		V _{CC} = 6.0 V	17	-	-	ns
t _{rec}	recovery time	MR to $\overline{CP}$; see Fig. 5				
		V _{CC} = 2.0 V	65	-	-	ns
		V _{CC} = 4.5 V	13	-	-	ns
		V _{CC} = 6.0 V	11	-	-	ns
f _{max}	maximum frequency	CP; see Fig. 5				
		V _{CC} = 2.0 V	4.8	-	-	MHz
		V _{CC} = 4.5 V	24	-	-	MHz
		V _{CC} = 6.0 V	28	-	-	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
t _{pd}	propagation delay	$\overline{CP}$ to Q0; see Fig. 5 [1]				
		V _{CC} = 2.0 V	-	-	265	ns
		V _{CC} = 4.5 V	-	-	53	ns
		V _{CC} = 6.0 V	-	-	45	ns
		Qn to Qn+1; see Fig. 5 [1]				
		V _{CC} = 2.0 V	-	-	120	ns
		V _{CC} = 4.5 V	-	-	24	ns
		V _{CC} = 6.0 V	-	-	20	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Q0; see Fig. 5				
		V _{CC} = 2.0 V	-	-	300	ns
		V _{CC} = 4.5 V	-	-	60	ns
		V _{CC} = 6.0 V	-	-	51	ns
t _t	transition time	see Fig. 5 [2]				
		V _{CC} = 2.0 V	-	-	110	ns
		V _{CC} = 4.5 V	-	-	22	ns
		V _{CC} = 6.0 V	-	-	19	ns
t _w	pulse width	$\overline{CP}$ HIGH or LOW; see Fig. 5				
		V _{CC} = 2.0 V	120	-	-	ns
		V _{CC} = 4.5 V	24	-	-	ns
		V _{CC} = 6.0 V	20	-	-	ns
		MR HIGH; see Fig. 5				
		V _{CC} = 2.0 V	120	-	-	ns
		V _{CC} = 4.5 V	24	-	-	ns
		V _{CC} = 6.0 V	20	-	-	ns
t _{rec}	recovery time	MR to $\overline{CP}$; see Fig. 5				
		V _{CC} = 2.0 V	75	-	-	ns
		V _{CC} = 4.5 V	15	-	-	ns
		V _{CC} = 6.0 V	13	-	-	ns
f _{max}	maximum frequency	CP; see Fig. 5				
		V _{CC} = 2.0 V	4.0	-	-	MHz
		V _{CC} = 4.5 V	20	-	-	MHz
		V _{CC} = 6.0 V	24	-	-	MHz

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit

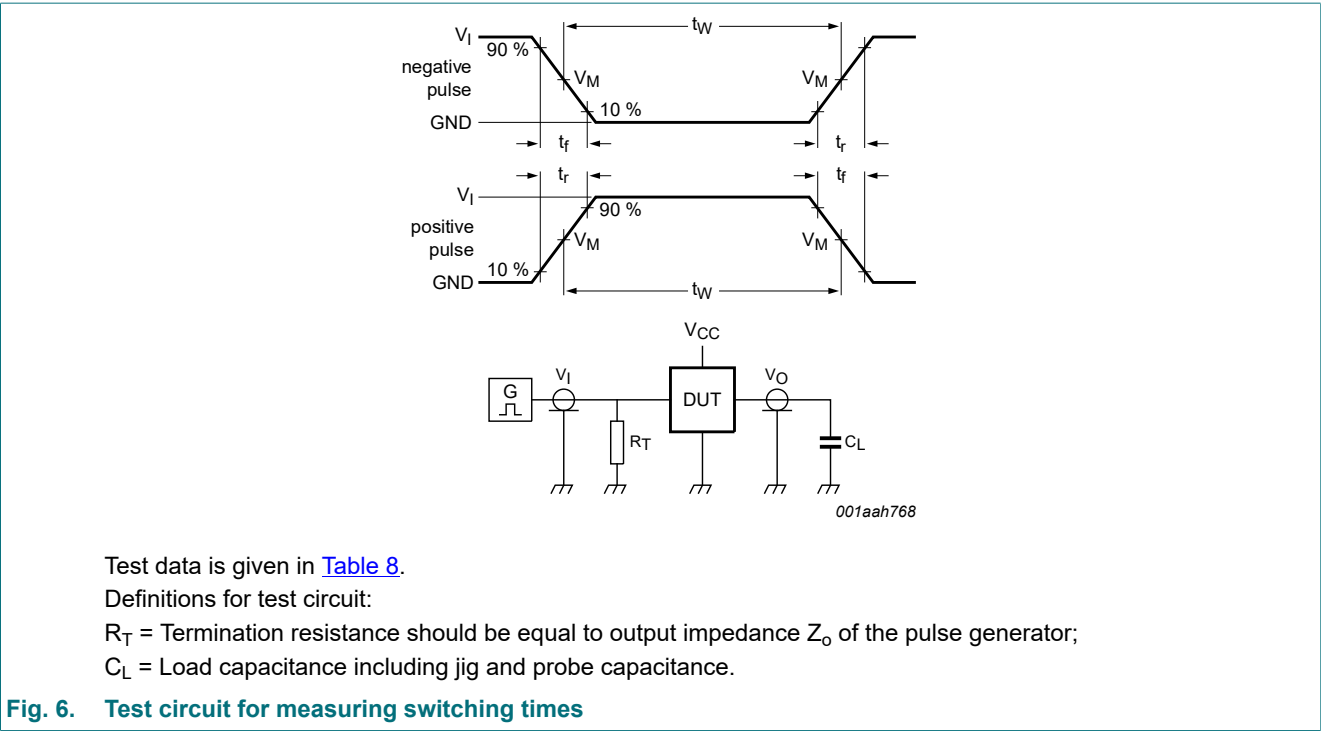
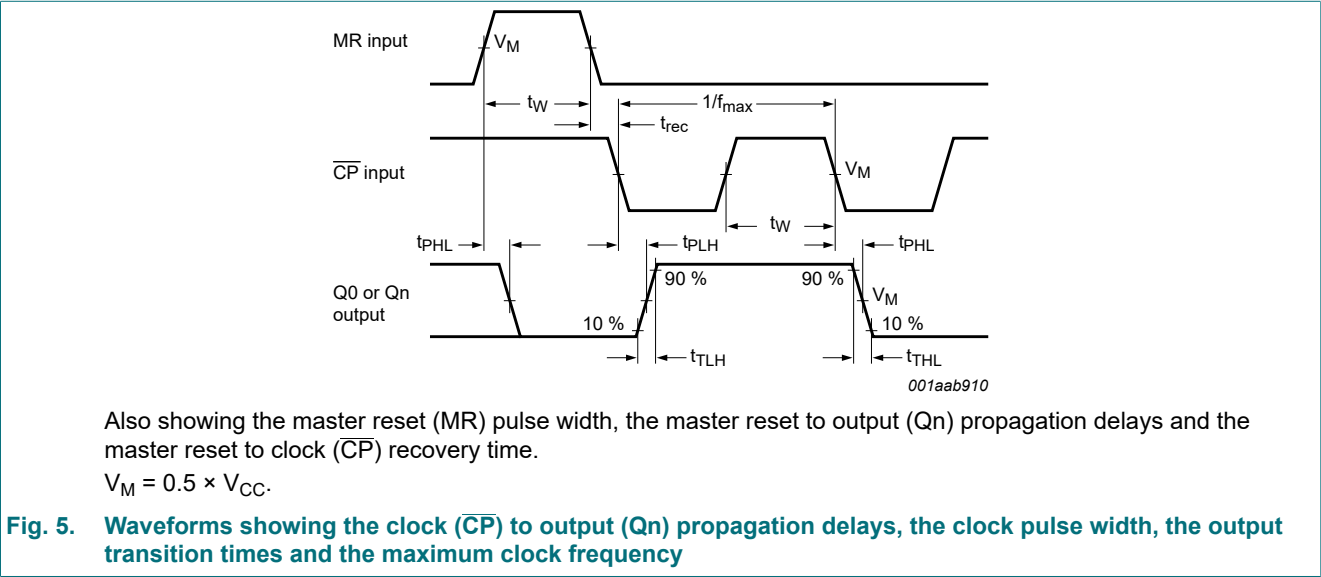


Table 8. Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

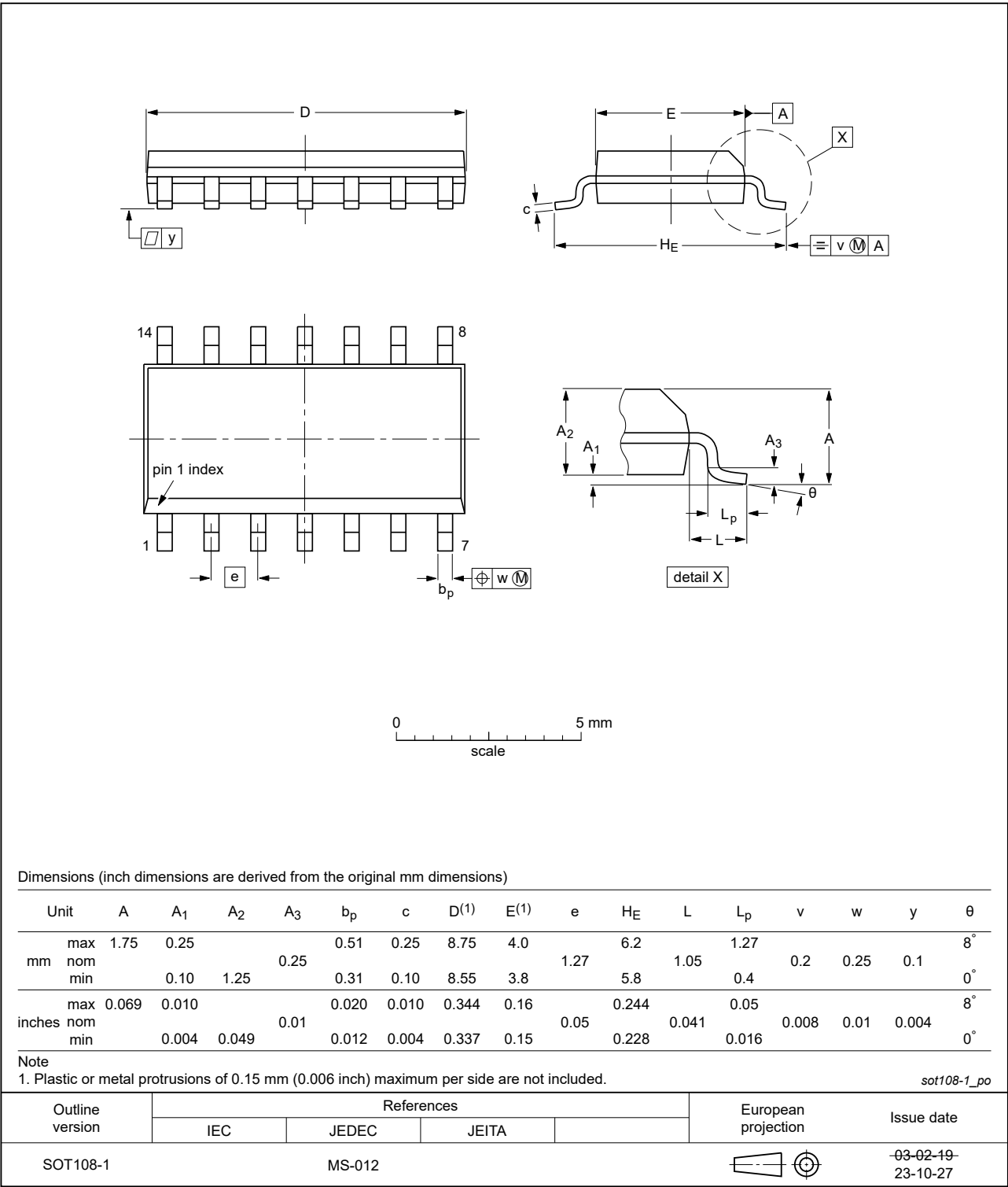


Fig. 7. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4024_Q100 v.3	20240216	Product data sheet	-	74HC4024_Q100 v.2
Modifications:	• Section 2: : ESD specification updated according to the latest JEDEC standard. • Section 8: Derating values for P_{tot} total power dissipation updated. • Fig. 7: Aligned SO package outline drawing to JEDEC MS-012			
74HC4024_Q100 v.2	20181123	Product data sheet	-	74HC4024_Q100 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74HC4024PW-Q100 (SOT402-1/TSSOP14) removed.			
74HC4024_Q100 v.1	20131127	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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