High Speed Digital Isolator
2500 Vrms 2ch

BM67220FV-C

General Description

The BM67220FV-C is a high-speed isolator IC used in electric vehicles and hybrid vehicles. This IC features dielectric strength of 2500 Vrms between I/O. Maximum propagation delay time is 45 ns.

Key Specification

- Supply Voltage Range: 4.5V to 5.5V
- Propagation Delay: 45ns (Max)
- Stand-by Current: 0μA (Typ)
- Operating Temperature Range: -40°C to +125°C

Features

1. Dielectric strength of 2500 Vrms between I/O
2. Maximum propagation delay time of 45 ns
3. Built-in 2ch uni-directional propagation
4. AEC-Q100 Qualified
5. UL1577 Recognized:File No. E356010

Package

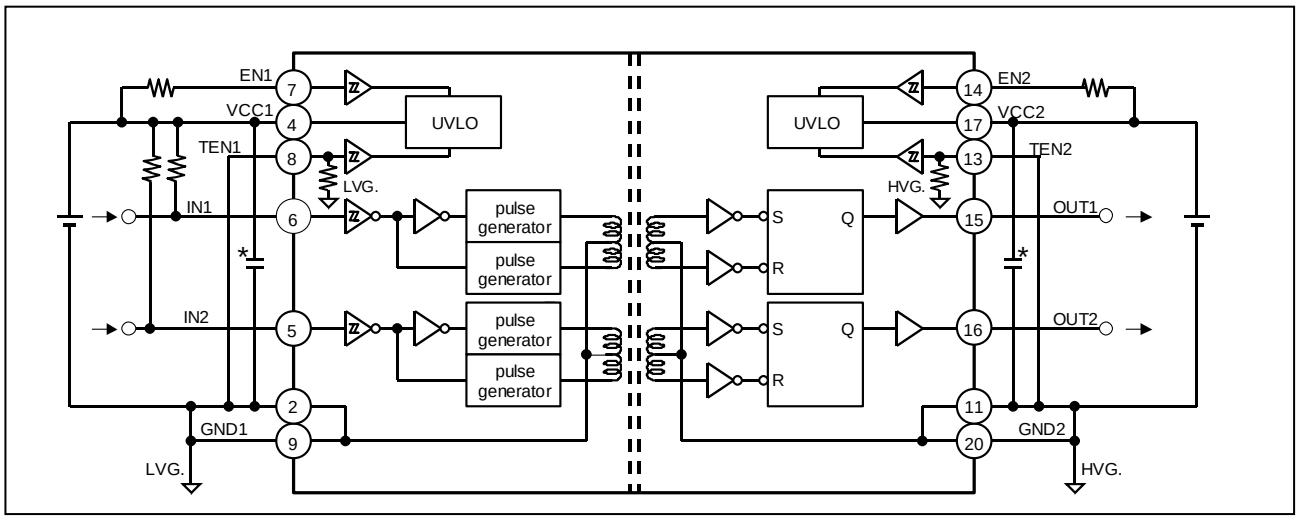
W(Typ) x D(Typ) x H(Max)

SSOP-B20W
6.50mm x 8.10mm x 2.01mm

Applications

Propagation of logic signal within electric and hybrid vehicles

Typical Application Circuit



* Please connect bypass capacitor directly to the IC pin.

Figure 1. BM67220FV-C Application Example

Pin Configuration

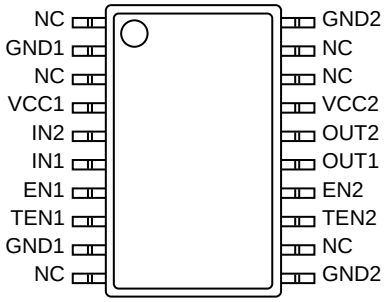


Figure 2. BM67220FV-C Package (SSOP-B20W)

Pin Description

No.	Pin Name	Function	No.	Pin Name	Function
1	NC	No Connection	20	GND2	Ground 2
2	GND1	Ground 1	19	NC	No Connection
3	NC	No Connection	18	NC	No Connection
4	VCC1	Power supply 1	17	VCC2	Power supply 2
5	IN2	Input 2	16	OUT2	Output 2
6	IN1	Input 1	15	OUT1	Output 1
7	EN1	Enable input 1	14	EN2	Enable input 2
8	TEN1	Test mode input 1	13	TEN2	Test mode input 2
9	GND1	Ground 1	12	NC	No Connection
10	NC	No Connection	11	GND2	Ground 2

Description of Operation

1. Input/Output logic
The input/output logic levels for the BM67220FV-C are as shown in the table below.

No.	EN1	EN2	IN1	IN2	OUT1	OUT2
1	L	L	X	X	L	L
2	L	H	L	L	*	*
3			L	H	*	*
4			H	L	*	*
5			H	H	*	*
6	H	L	L	L	L	L
7			L	H	L	L
8			H	L	L	L
9			H	H	L	L
10	H	H	L	L	L	L
11			L	H	L	H
12			H	L	H	L
13			H	H	H	H

* Retains its previous state

In case EN1 and EN2 pins are "L" as in no. 1, the logic of OUT1 pin and OUT2 pin becomes "L".
In case EN1 pin is "L" and EN2 pin is "H" as in no. 2 ~ 5, the logic of OUT1 pin and OUT2 pin will retain its previous state.
In case EN2 pin is "L" and EN1 pin is "H" as in no. 6 ~ 9, the logic of OUT1 pin and OUT2 pin becomes "L".
In case EN1 and EN2 pins are "H" as in no. 10 ~ 13, the output logic of OUT1 (OUT2) pin changes according to the input logic of IN1 (IN2) pins.
Likewise, since pull up/pull down resistor has not been connected to IN1, IN2, EN1 and EN2 pins, it is necessary to connect external resistor in case you would like to fix the input logic of IN1, IN2, EN1 and EN2 pins.

2. TEN pins
The TEN pins serve as a test enable pin, respectively.
Please connect to GND to avoid the possibility of chip malfunction.

3. Output pin voltage
Logic levels for output pins are indicated in the truth table in Sections 1, 6, and 7. However, it may be assumed that such logic levels disable the output circuit to fully turn ON at a low voltage when turning ON or OFF the power supply, thus putting the output pin into the high impedance state.

4. Under Voltage Lock Out (UVLO) function
This IC has a built-in UVLO function to prevent the IC from malfunctioning whenever the power supply voltage drops.
It triggers the UVLO state when VCC1 pin and VCC2 pin are changed to 3.8V (Typ) or less and becomes in operational state when changed to 4.0V (Typ) or more.
If VCC1 drops to 3.8V or less, both OUT1 and OUT2 pins retain its state.
If VCC2 drops to 3.8V or less, both OUT1 and OUT2 pins will be set to “L” logic level.
In case VCC2 pin voltage was changed from 3.8V (Typ) or less to 4.0V (Typ) or more at 4.0V (Typ) or more for VCC1 pin voltage, the output logic of OUT1 pin and OUT2 pin becomes "L".
In case VCC1 pin voltage was changed from 3.8V (Typ) or less to 4.0V (Typ) or more at 4.0V (Typ) or more for VCC2 pin voltage, the output logic of OUT1 (OUT2) pin changes according to the input logic of input IN1 (IN2) pin.

5. Under Voltage Lock Out (UVLO) function masking time
This IC provides masking time for the UVLO function. The masking time is set to 10 µsec (Typ).

6. Input/Output logic levels with power supply turned OFF
The following table shows the output logic levels according to the order in which the power supply turns OFF.

No.	Power Supply	IN1	IN2	OUT1	OUT2
1	VCC1	L	L	L	L
2		L	H	L	H
3		H	L	H	L
4		H	H	H	H
5	VCC2	L	L	L	L
6		L	H	L	L
7		H	L	L	L
8		H	H	L	L

The output logic of OUT1 pin and OUT2 pin is in a maintained state in case VCC1 is turned OFF as in no. 1 ~ 4.
The output logic of OUT1 pin and OUT2 pin is “L” in case VCC2 is turned OFF as in no. 5 ~ 8.

7. Output logic levels with power supply turned ON
The following table shows the output logic levels according to the order in which the power supply turns ON.

No.	Turning-ON Order1	Turning-ON Order2	IN1	IN2	OUT1	OUT2
1	VCC1	VCC2	L	L	L	L
2			L	H	L	L*
3			H	L	L*	L
4			H	H	L*	L*
5	VCC2	VCC1	L	L	L	L
6			L	H	L	H
7			H	L	H	L
8			H	H	H	H

*Different input and output logic

In case VCC1 is turned ON first as in no. 1 ~ 4, a signal from VCC1 side to the circuit of VCC2 side cannot be received because of the cancellation by the signal before the circuit of VCC2 (receiving) side rises.
For that reason, the output logic of OUT1 pin and OUT2 pin become "L" and the output logic does not match with the input logic as in no. 2, 3, 4*.

Timing Chart

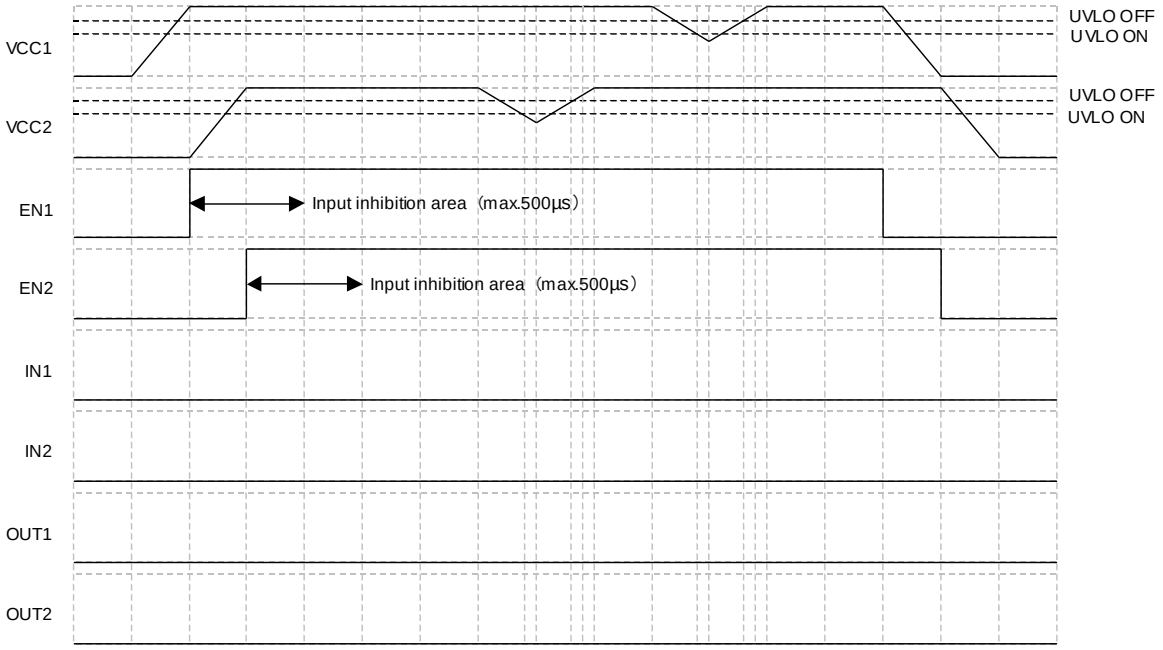


Figure 3. VCC1 to VCC2 (IN1=L, IN2=L)

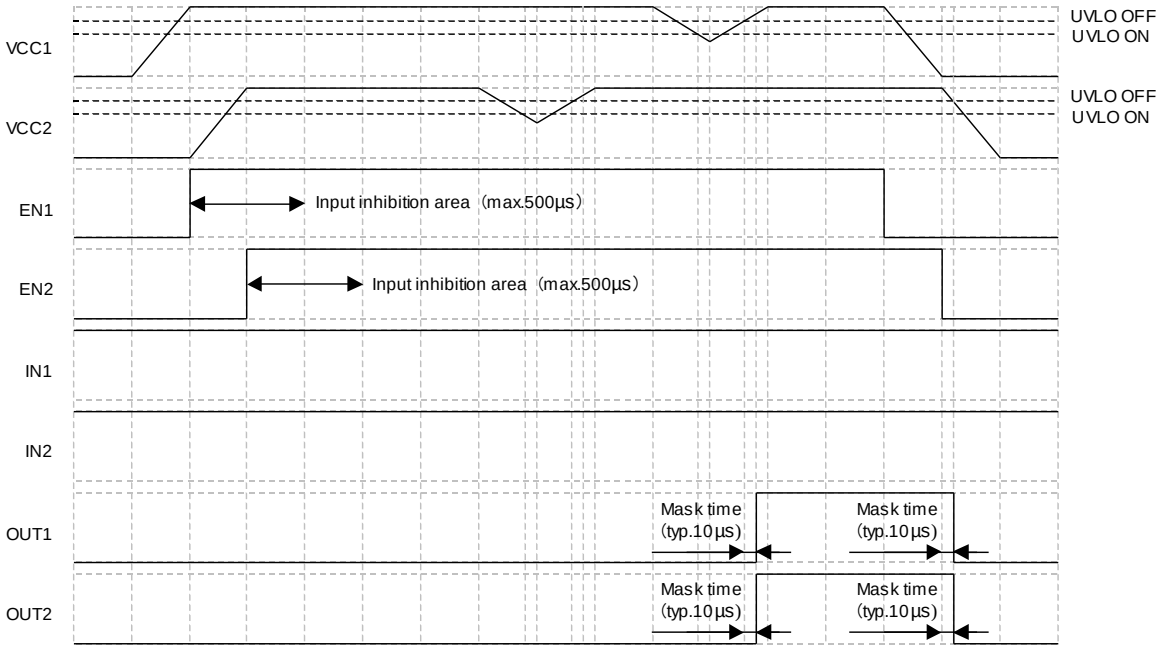


Figure 4. VCC1 to VCC2 (IN1=H, IN2=H)

Timing Chart - continued

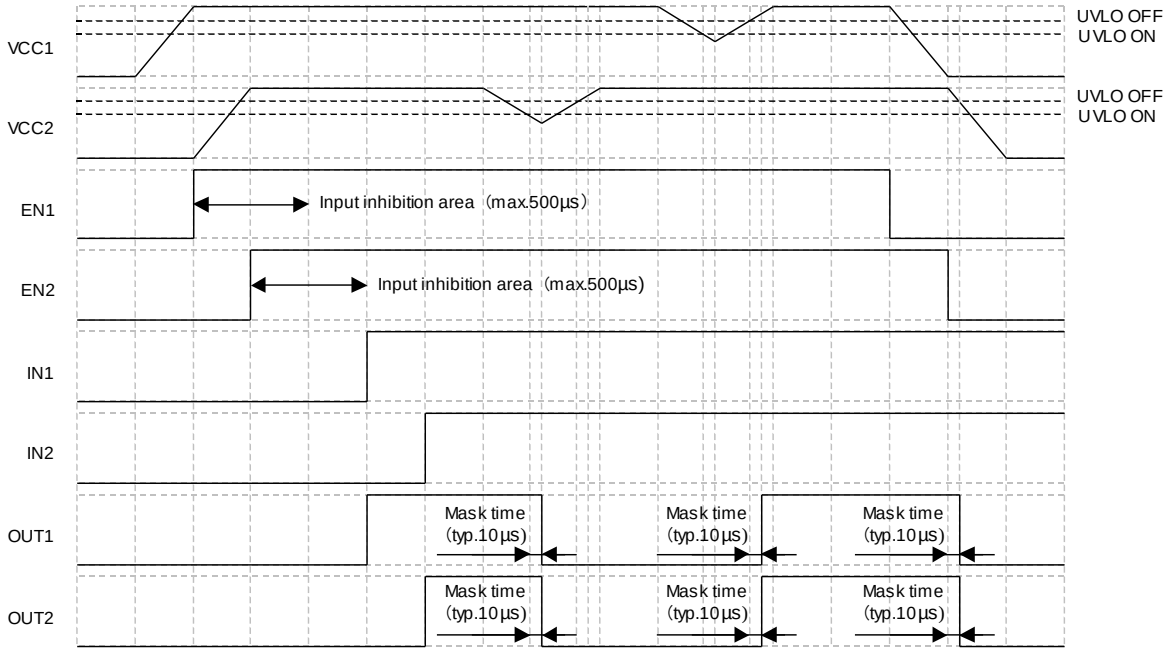


Figure 5. VCC1 to VCC2 (IN1=L to H, IN2=L to H)

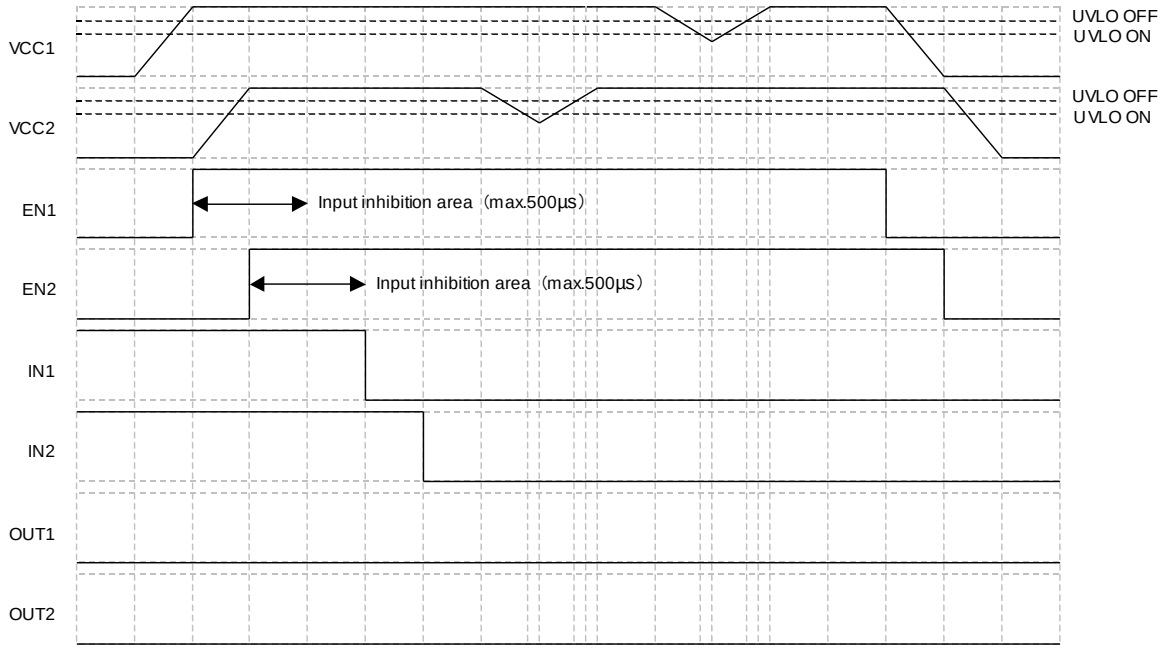


Figure 6. VCC1 to VCC2 (IN1=H to L, IN2=H to L)

Timing Chart - continued

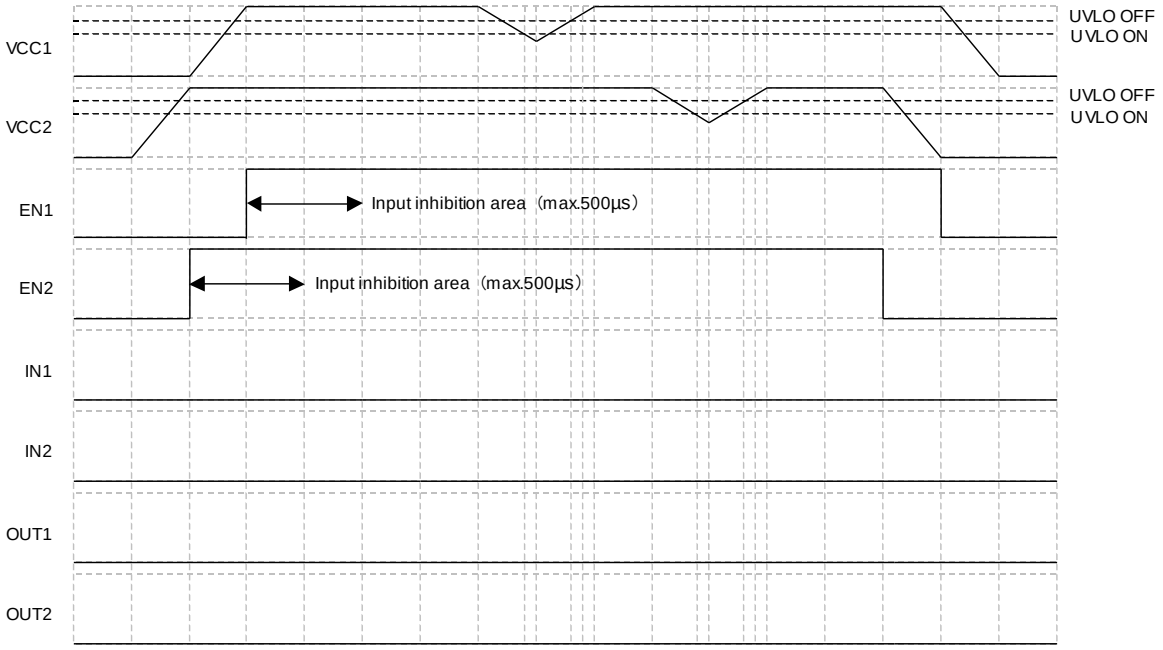


Figure 7. VCC2 to VCC1 (IN1=L, IN2=L)

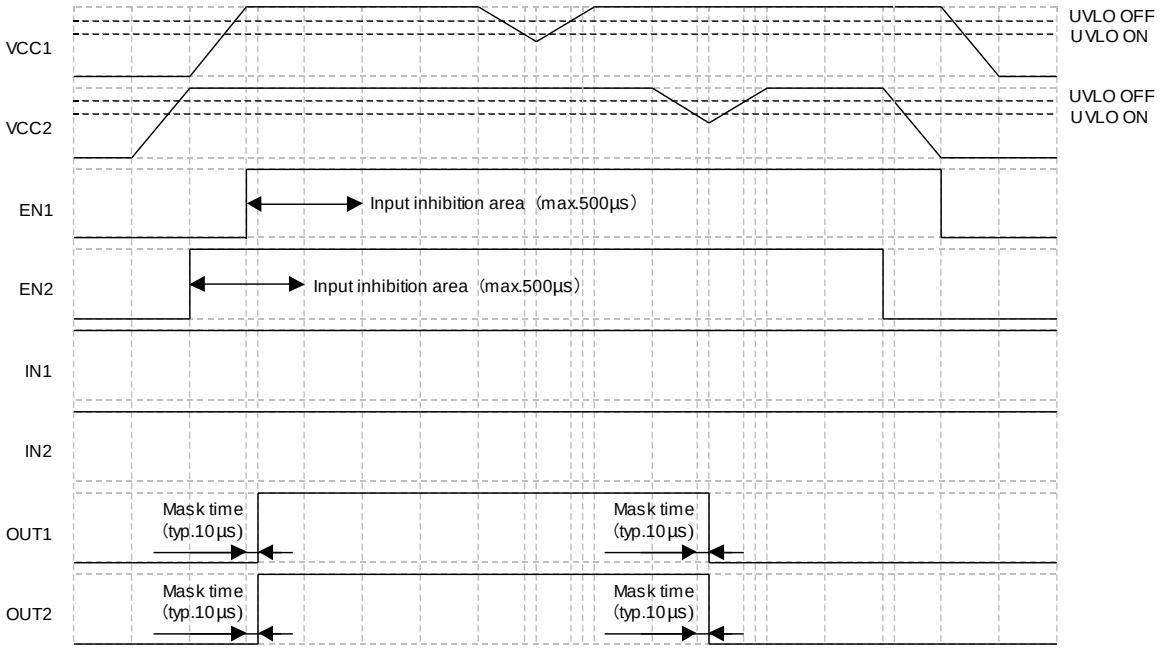


Figure 8. VCC2 to VCC1 (IN1=H, IN2=H)

Timing Chart - continued

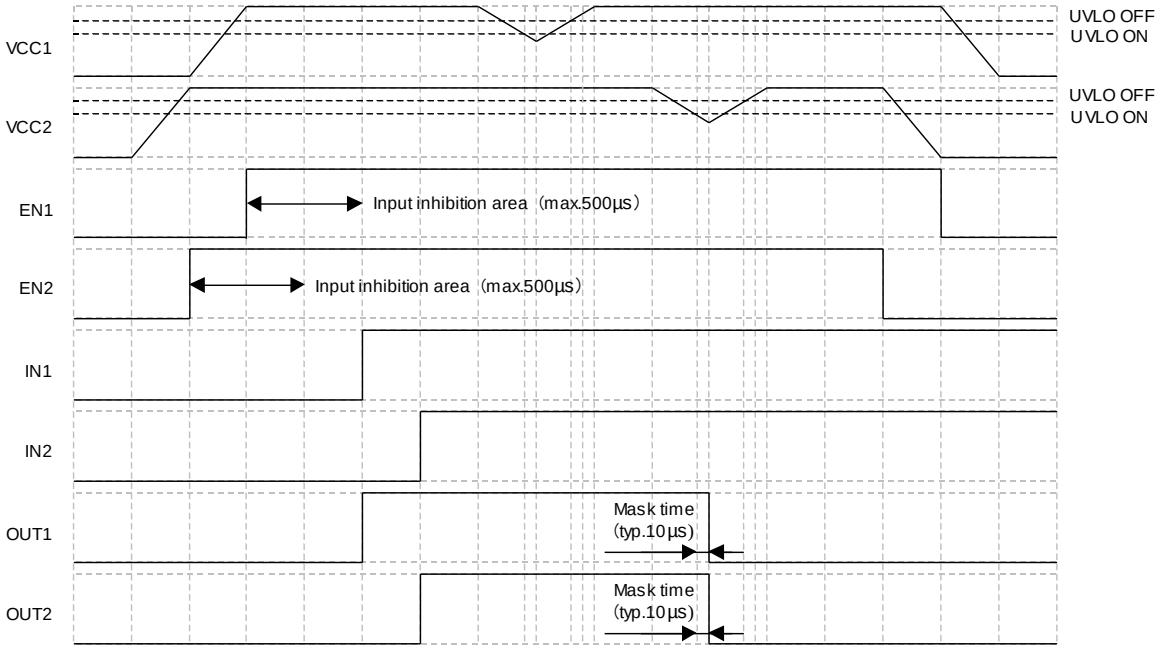


Figure 9. VCC2 to VCC1 (IN1=L to H, IN2=L to H)

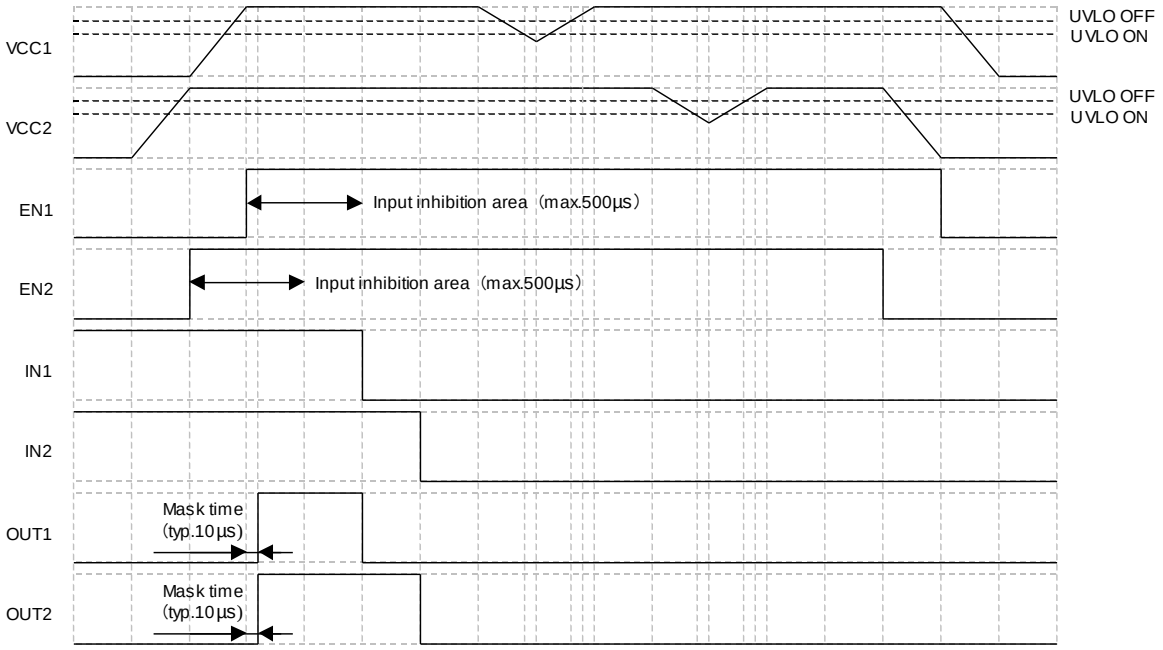


Figure 10. VCC2 to VCC1 (IN1=H to L, IN2=H to L)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
		BM67220FV-C	
Power Supply Voltage 1	V_{CC1}	7.0(Note 1)	V
Power Supply Voltage 2	V_{CC2}	7.0(Note 2)	V
IN1 Pin Voltage	V_{IN1}	-0.3 to +7.0(Note 1)	V
IN2 Pin Voltage	V_{IN2}	-0.3 to +7.0(Note 1)	V
OUT1 Pin Voltage	V_{OUT1}	-0.3 to +7.0(Note 2)	V
OUT2 Pin Voltage	V_{OUT2}	-0.3 to +7.0(Note 2)	V
Output Current	$I_{OMAX(OUT)}$	±10(Note 3)	mA
GND1-GND2 Ground Potential	V_{GND}	2500	Vrms
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Power Dissipation	Pd	1.19(Note 4)	W
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) Reference to GND1.
(Note 2) Reference to GND2.
(Note 3) Should not exceed Pd and ASO.
(Note 4) Derate by 9.52mW/°C when operating above Ta=25°C, when mounted on a glass epoxy board measuring 70 mm × 70 mm × 1.6 mm (including a copper foil area of 3% or less).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings

Recommended Operating Conditions

Parameter	Symbol	BM67220FV-C	Unit
Power Supply Voltage 1	V_{CC1}	4.5 to 5.5(Note 5)	V
Power Supply Voltage 2	V_{CC2}	4.5 to 5.5(Note 6)	V

(Note 5) Relative to GND1
(Note 6) Relative to GND2

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage/1Min	V_{ISO}	2500	Vrms
Insulation Test Voltage/1s	V_{ISO}	3000	Vrms

UL1577 Ratings Table

Following values are described in UL Report.

Parameter	Values	Units	Conditions
Side 1 Circuit Current	0.21	mA	VCC1=5V
Side 2 Circuit Current	0.21	mA	VCC2=5V
Side 1 Consumption Power	1.05	mW	VCC1=5V
Side 2 Consumption Power	1.05	mW	VCC2=5V
Isolation Voltage	2500	Vrms	
Maximum Operating (Ambient) Temperature	125	℃	
Maximum Junction Temperature	150	℃	
Maximum Strage Temperature	150	℃	
Maximum Data Transmission Rate	20	MHz	

Electrical Characteristics (All values at Ta=-40°C to125°C and VCC=4.5V to 5.5V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<Whole>						
VCC1 Power Supply Current, Quiescent	$I_{CC1STBY}$	-	0	10	µA	EN1 = 0
VCC2 Power Supply Current, Quiescent	$I_{CC2STBY}$	-	0	10	µA	EN2 = 0
VCC1 Power Supply Current, DC	I_{CC1Q}	-	0.21	0.42	mA	V_{IN} = 0 or V_{CC}
VCC2 Power Supply Current, DC	I_{CC2Q}	-	0.21	0.42	mA	V_{IN} = 0 or V_{CC}
VCC1 Power Supply Current, 10kbps	I_{CC10k1}	-	0.23	0.50	mA	f_{IN} : 5kHz
VCC2 Power Supply Current, 10kbps	I_{CC10k2}	-	0.22	0.48	mA	f_{IN} : 5kHz
VCC1 Power Supply Current, 1Mbps	I_{CC1M1}	-	1.36	3.20	mA	f_{IN} : 500kHz
VCC2 Power Supply Current, 1Mbps	I_{CC1M2}	-	0.40	1.00	mA	fin : 500kHz
IN1,IN2 Input Inhibition Area	t_{IN}	-	-	500(Note 7)	µs	
<Output Pin: OUT1 And OUT2>						
High-Level Output Voltage	V_{OH}	V_{CC}-0.5	V_{CC}-0.3	V_{CC}	V	I_O=-4mA
Low-Level Output Voltage	V_{OL}	0	0.2	0.4	V	I_O=4mA

(Note 7) Please do not switch the input signal IN1 and IN2 between t_{IN} sections. Output may not match the logic input.

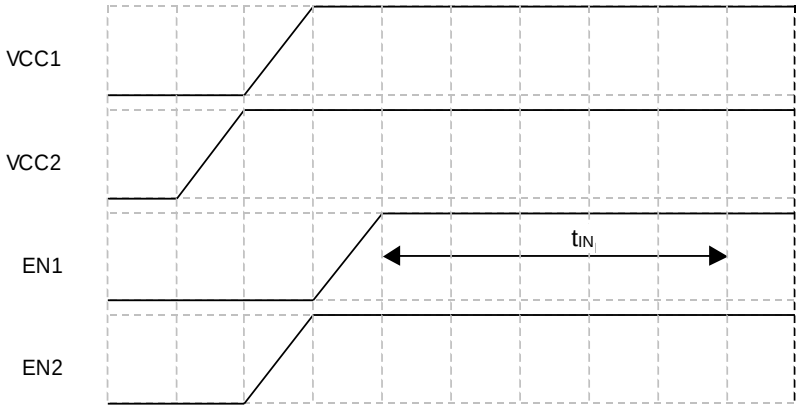


Figure 11. IN1, IN2 Input inhibition area

Electrical Characteristics - continued

(All values at Ta=-40°C to +125°C and V_{CC}=4.5V to 5.5V, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<Input Pin: IN1 And IN2>						
Input current	I_{IN}	-	0	10	µA	$V_{IN}=V_{CC}$
High-Level Input Threshold	V_{INH}	V_{CC}×0.7	-	V_{CC}	V	
Low-Level Input Threshold	V_{INL}	0	-	V_{CC}×0.3	V	
<Enable Pin: EN1 And EN2>						
Input Current	I_{EN}	-	0	10	µA	$V_{EN}=V_{CC}$
High-Level Input Threshold	V_{ENH}	V_{CC}×0.7	-	V_{CC}	V	
Low-Level Input Threshold	V_{ENL}	0	-	V_{CC}×0.3	V	
<Test Pin: T_EN1 And T_EN2>						
Input Current	I_{TEN}	30	50	70	µA	$V_{T\_EN}=V_{CC}$
High-Level Input Threshold	V_{TENH}	V_{CC}×0.7	-	V_{CC}	V	
Low-Level Input Threshold	V_{TENL}	0	-	V_{CC}×0.3	V	
<Switching Characteristics>						
Propagation Delay (Low to High)	t_{PLH}	10	20	45	ns	
Propagation Delay (High to Low)	t_{PHL}	10	20	45	ns	
Propagation Distortion	$\|t_{PLH} - t_{PHL}\|$	-	0	8	ns	
Rise Time	t_r	-	2.5	-	ns	
Fall Time	t_f	-	2.5	-	ns	
Common-Mode Transient Immunity	CM_L	-	35	-	kV/µs	Design Assurance

Input/Output Timing

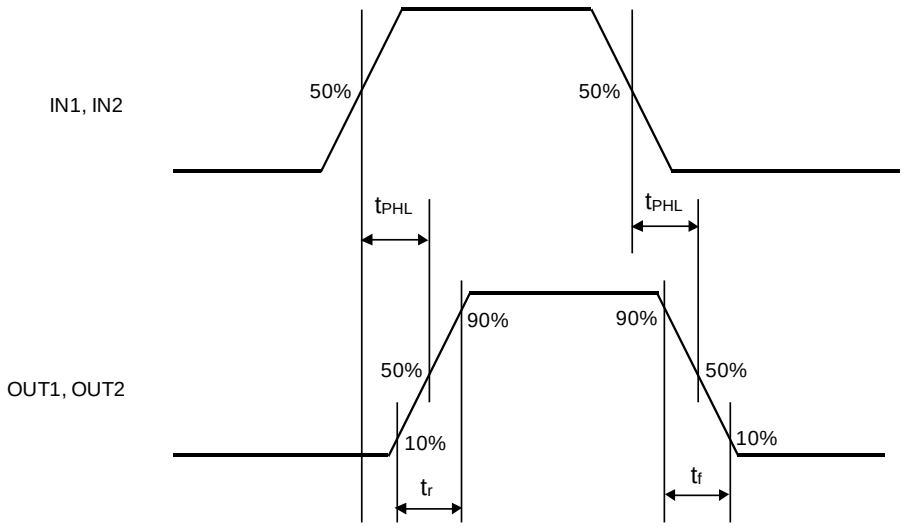


Figure 12. Input/Output Timing Chart

Typical Performance Curve

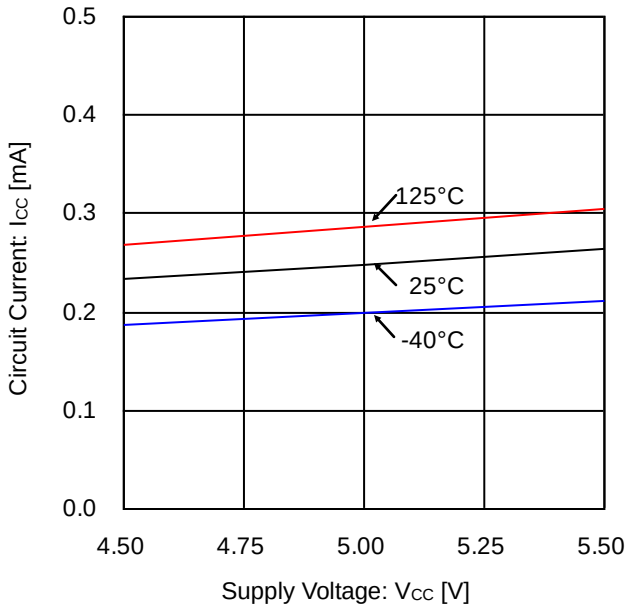


Figure 13. Circuit Current vs Supply Voltage
(VCC1 Power Supply Current)

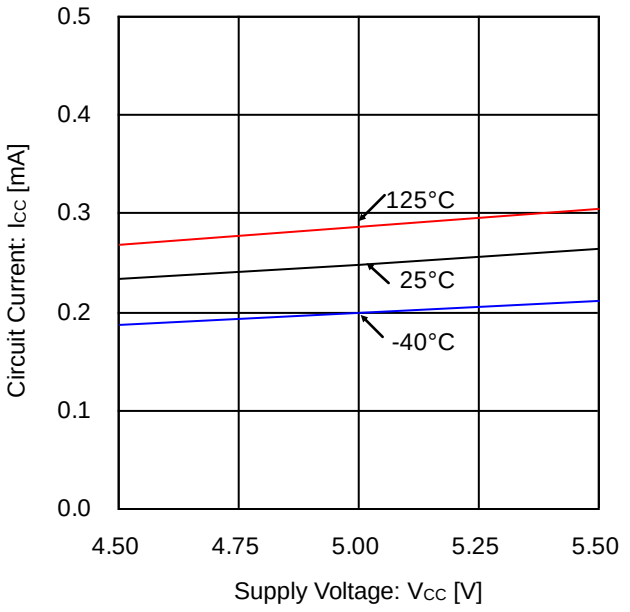


Figure 14. Circuit Current vs Supply Voltage
(VCC2 Power Supply Current, DC)

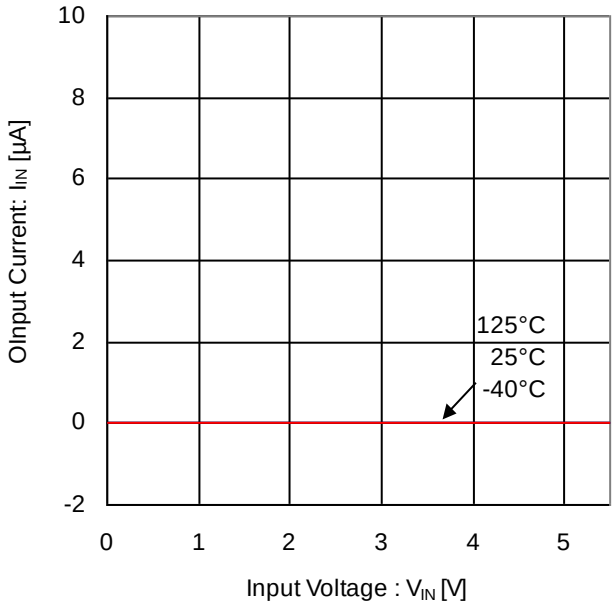


Figure 15. Input Current vs Input Voltage
(Input Current at Input Pin)

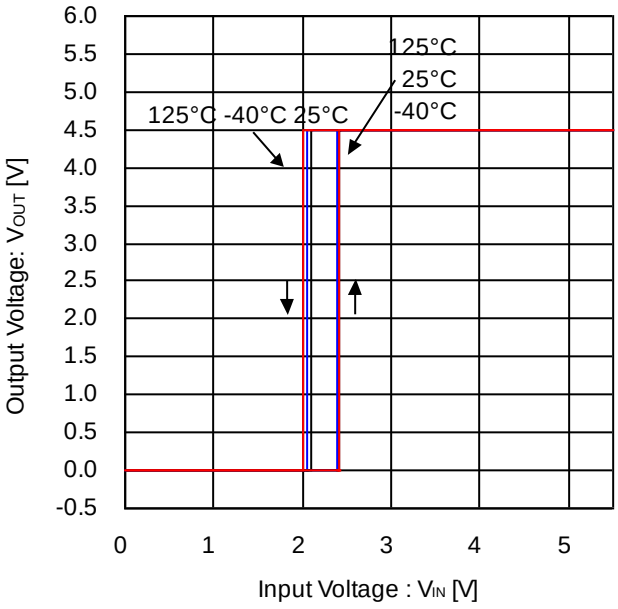


Figure 16. Input Voltage vs Input Voltage
(High-/Low-level Input Threshold, V_{CC1}, V_{CC2} = 4.5V)

Typical Performance Curve - continued

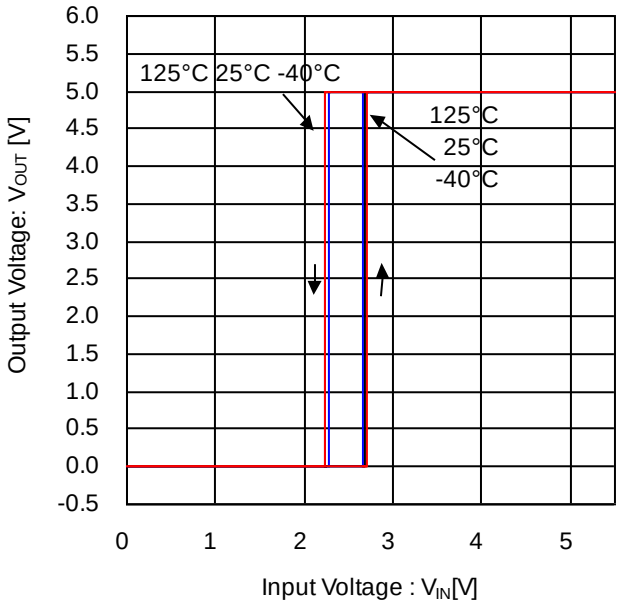


Figure 17. Output Voltage vs Input Voltage
(High-/Low-level Input Threshold, V_{CC1}, V_{CC2} = 5.0V)

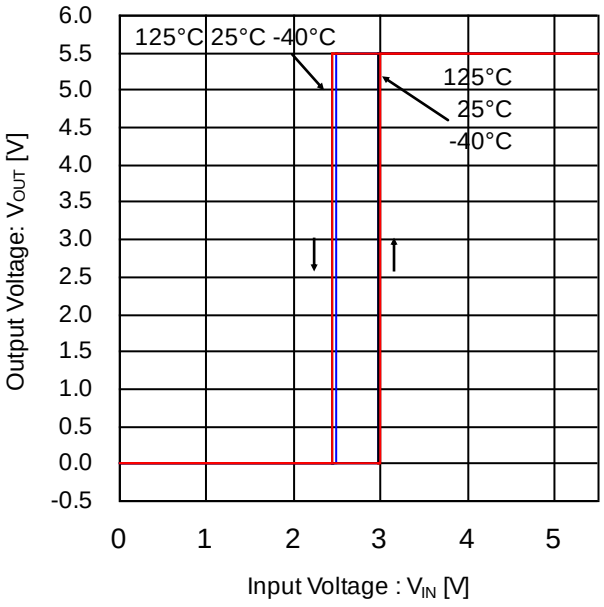


Figure 18. Output Voltage vs Input Voltage
(High-/Low-level Input Threshold, V_{CC1}, V_{CC2} = 5.5V)

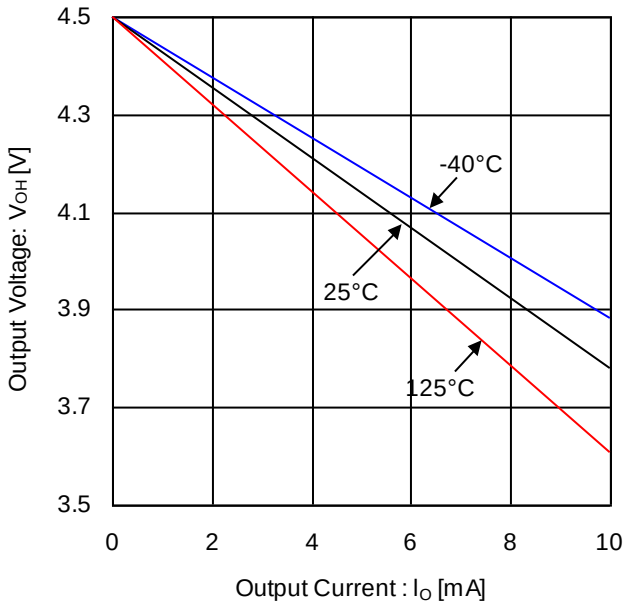


Figure 19. Output Voltage vs Output Current
(High-level Output Voltage, V_{CC1}, V_{CC2} = 4.5V)

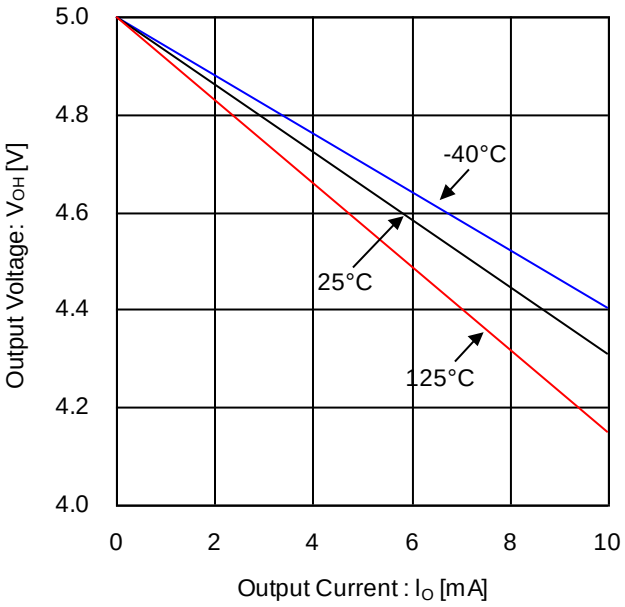


Figure 20. Output Voltage vs Output Current
(High-level Output Voltage, V_{CC1}, V_{CC2} = 5.0V)

Typical Performance Curve - continued

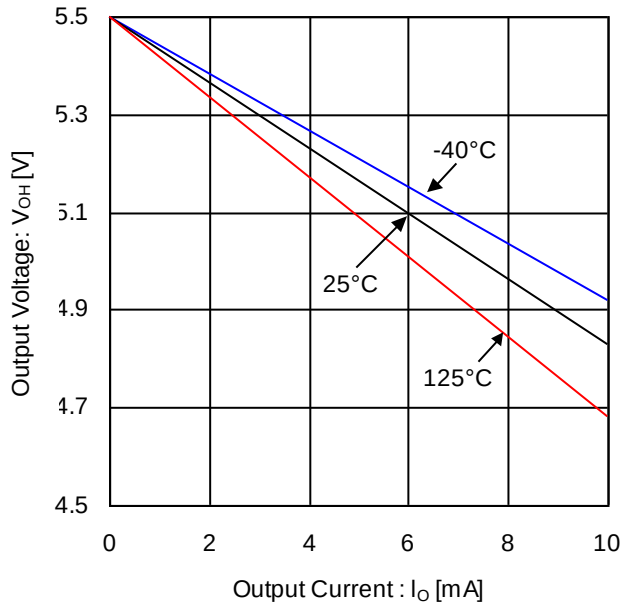


Figure 21. Output Voltage vs Output Current
(High-level Output Voltage, V_{CC1}, V_{CC2} = 5.5V)

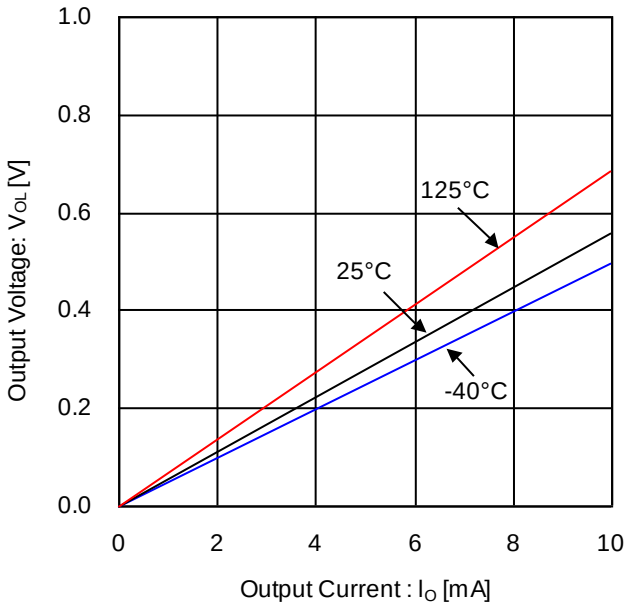


Figure 22. Output Voltage vs Output Current
(Low-level Output Voltage, V_{CC1}, V_{CC2} = 4.5V)

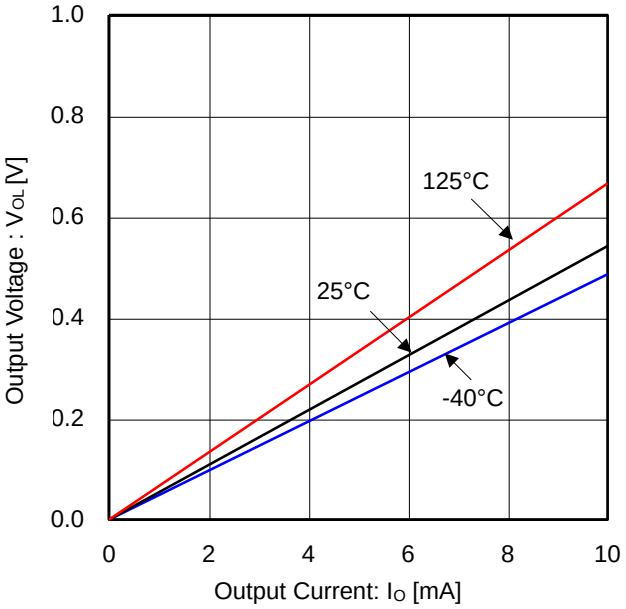


Figure 23. Output Voltage vs Output Current,
(Low-level Output Voltage, V_{CC1}, V_{CC2} = 5.0V)

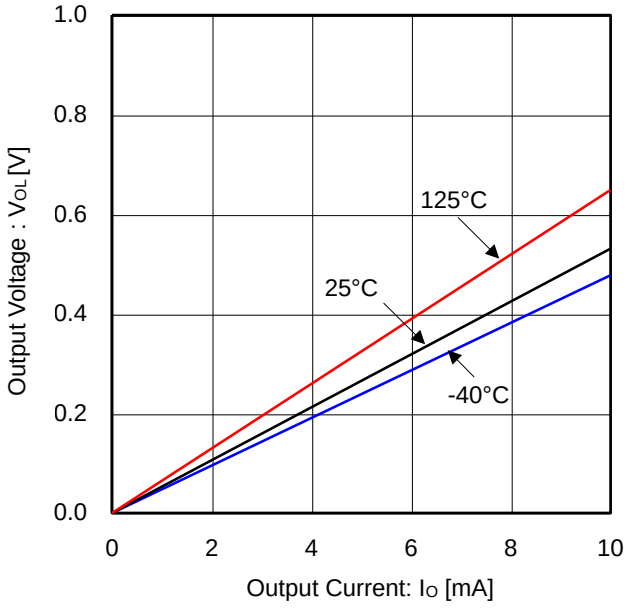


Figure 24. Output Voltage vs Output Current
(Low-level Output Voltage, V_{CC1}, V_{CC2} = 5.5V)

Typical Performance Curve - continued

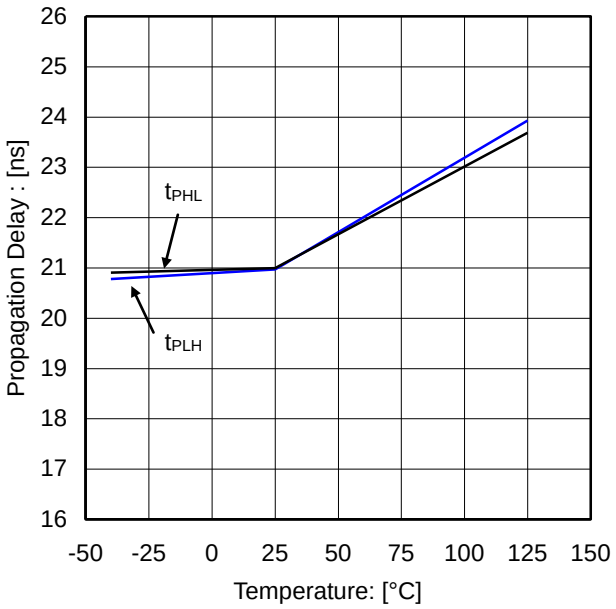


Figure 25. Propagation Delay vs Temperature
(V_{CC1}, V_{CC2} = 4.5V)

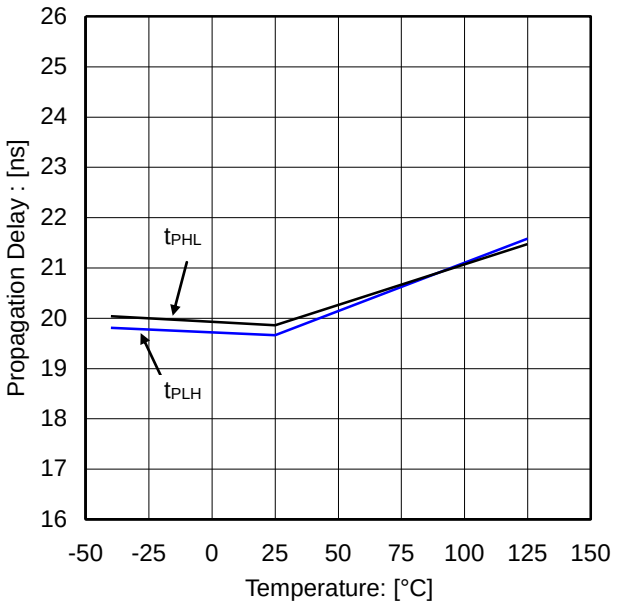


Figure 26. Propagation Delay vs Temperature
(V_{CC1}, V_{CC2} = 5.0V)

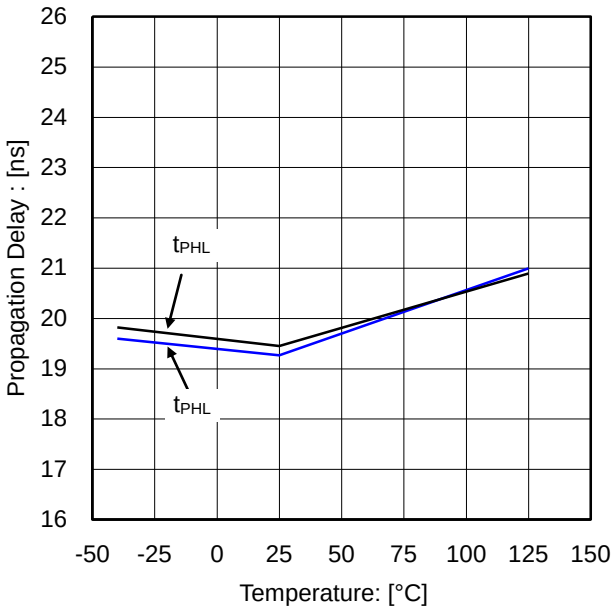


Figure 27. Propagation Delay vs Temperature
(V_{CC1}, V_{CC2} = 5.5V)

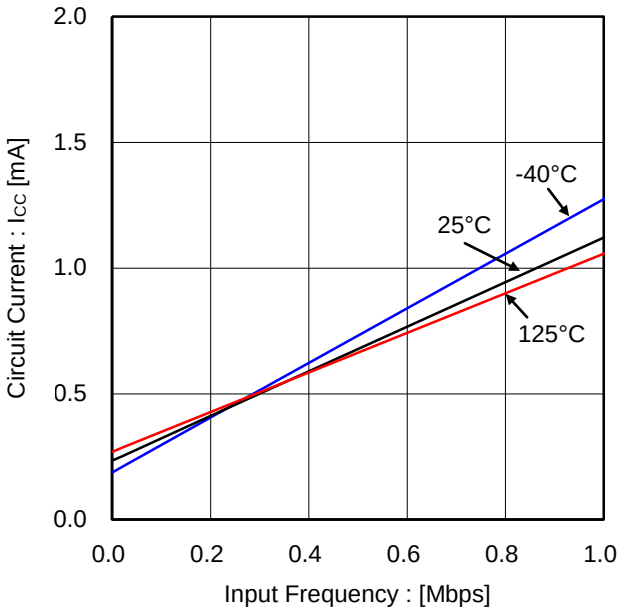


Figure 28. Circuit Current vs Input Frequency
(VCC1 Power Supply Current ,V_{CC1}, V_{CC2} = 4.5V)

Typical Performance Curve - continued

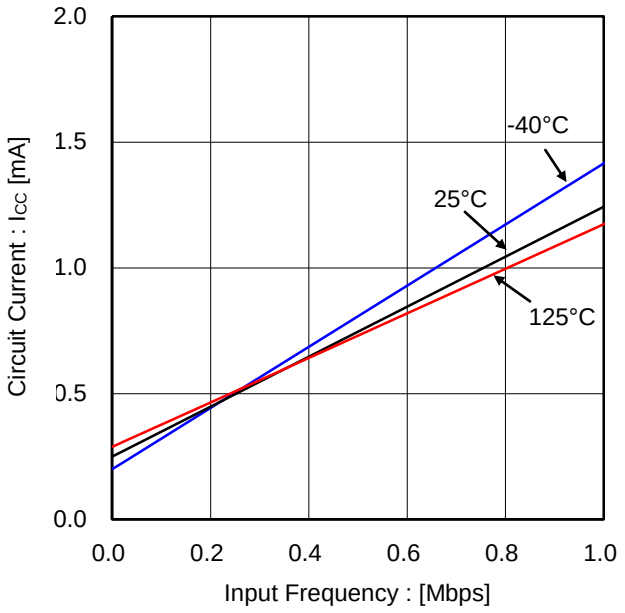


Figure 29. Circuit Current vs Input Frequency
(VCC1 Power Supply Current , V_{CC1}, V_{CC2} = 5.0V)

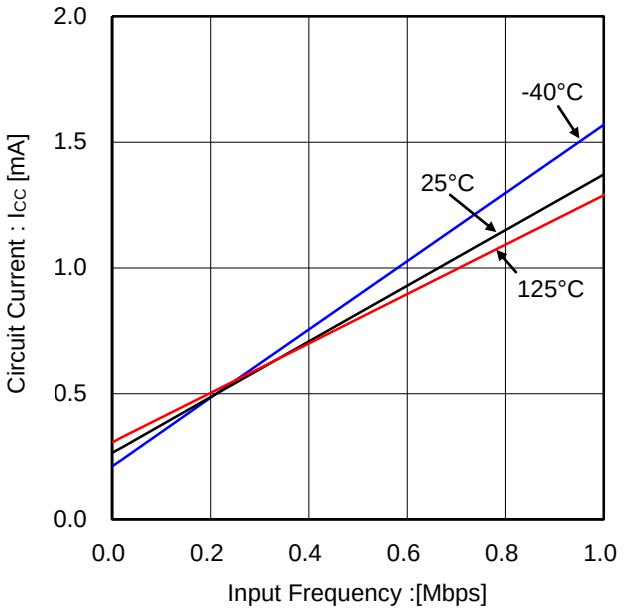


Figure 30. Circuit Current vs Input Frequency
(VCC1 Power Supply Current V_{CC1}, V_{CC2} = 5.5V)

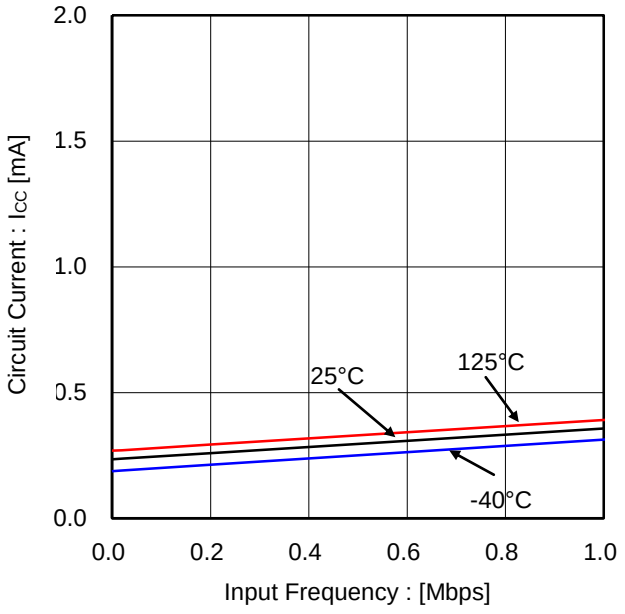


Figure 31. Circuit Current vs Input Frequency
(VCC2 Power Supply Current, V_{CC1}, V_{CC2} = 4.5V)

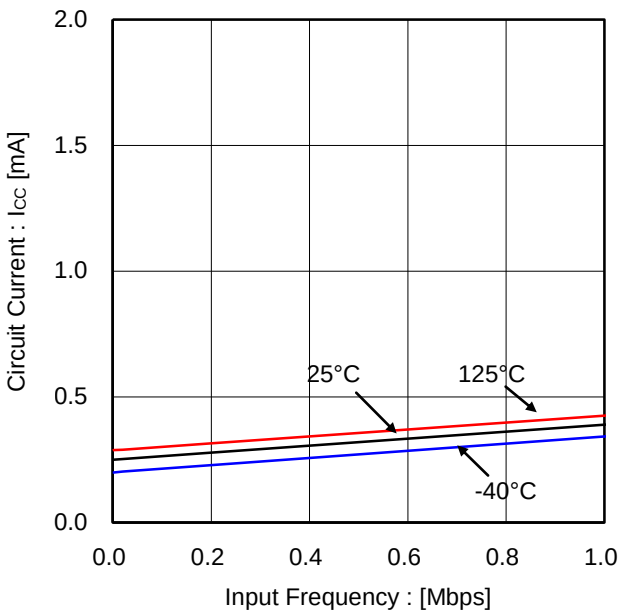


Figure 32. Circuit Current vs Input Frequency
(VCC2 Power Supply Current, V_{CC1}, V_{CC2} = 5.0V)

Typical Performance Curve - continued

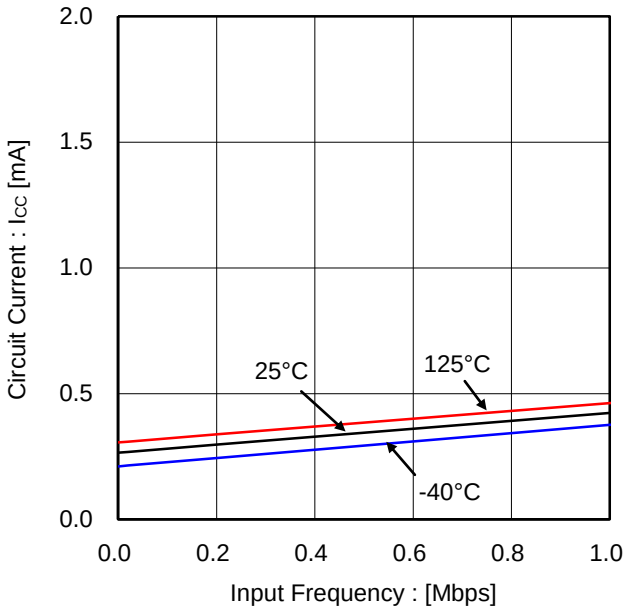


Figure 33. Circuit Current vs Input Frequency
(VCC2 Power Supply Current, V_{CC1}, V_{CC2} =5.5V)

I/O Equivalent Circuit

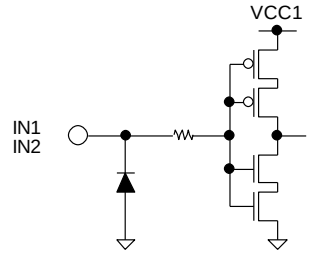


Figure 34. IN1, IN2

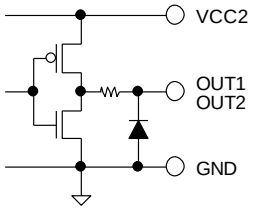


Figure 35. OUT1, OUT2

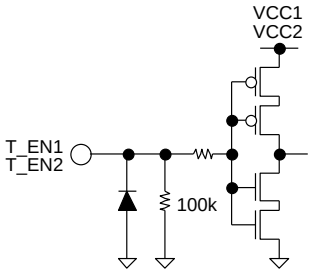


Figure 36. T_EN1, T_EN2

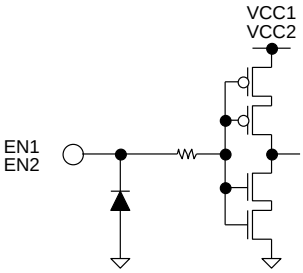


Figure 37. EN1, EN2

Power Dissipation Reduction Characteristics

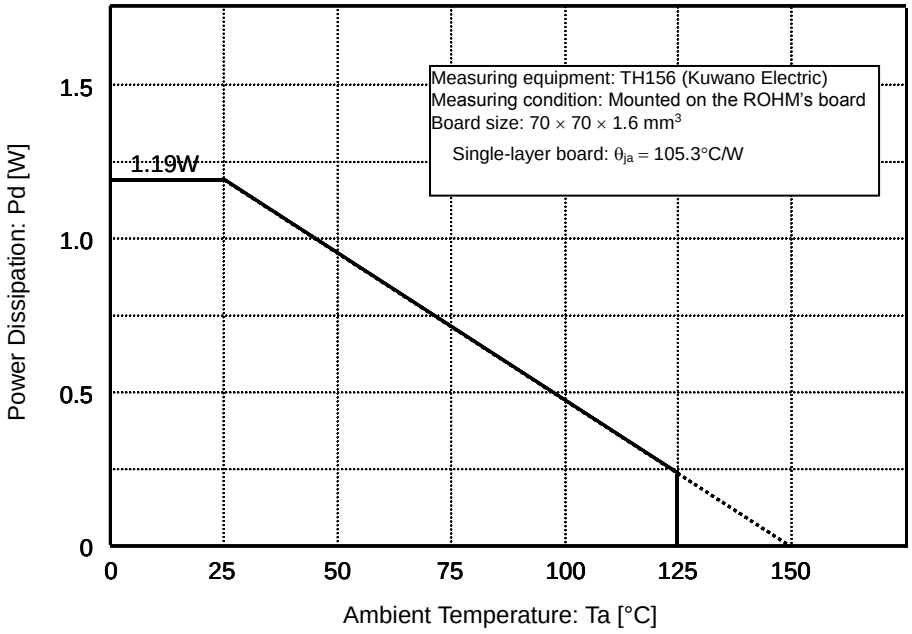


Figure 38. SSOP-B20W Power Dissipation Reduction Curve

Thermal Dissipation

In consideration of the power consumption (P), package power dissipation (Pd), and ambient temperature (Tj) of this IC, ensure that the operating temperature of the chip will not exceed 150°C. If Tj is beyond 150°C, parasitic elements may malfunction and may cause leakage current to increase. Constantly using the IC under the said conditions may deteriorate the IC and further lead to its breakdown. Strictly keep Tjmax at 150°C under any circumstances.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

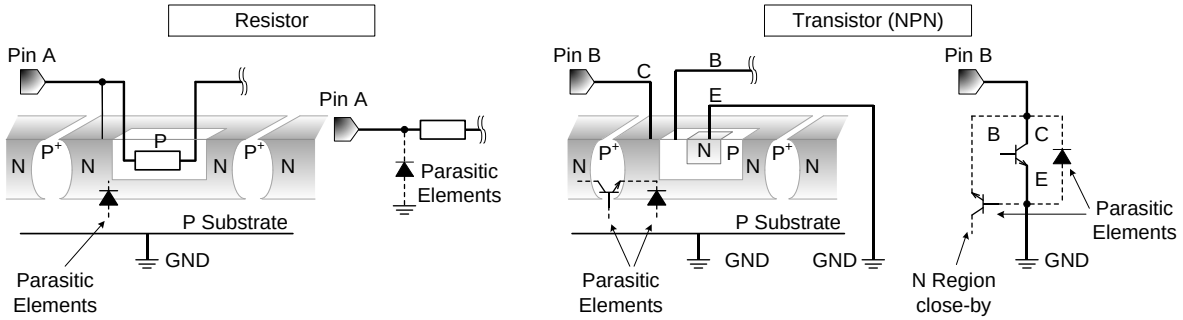
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Appendix: Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

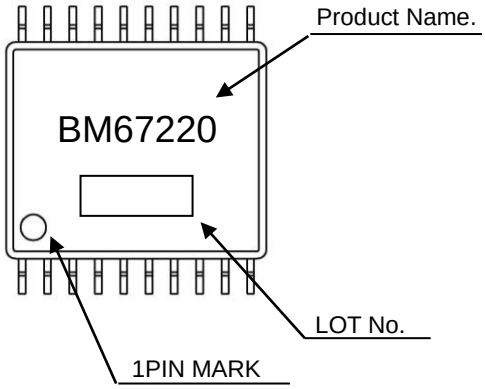
Ordering Information

B M 6 7 2 2 0 F V	-	CE 2

- Part Number
- Package FV : SSOP-B20W
- Packaging and forming specification E2: Embossed tape and reel

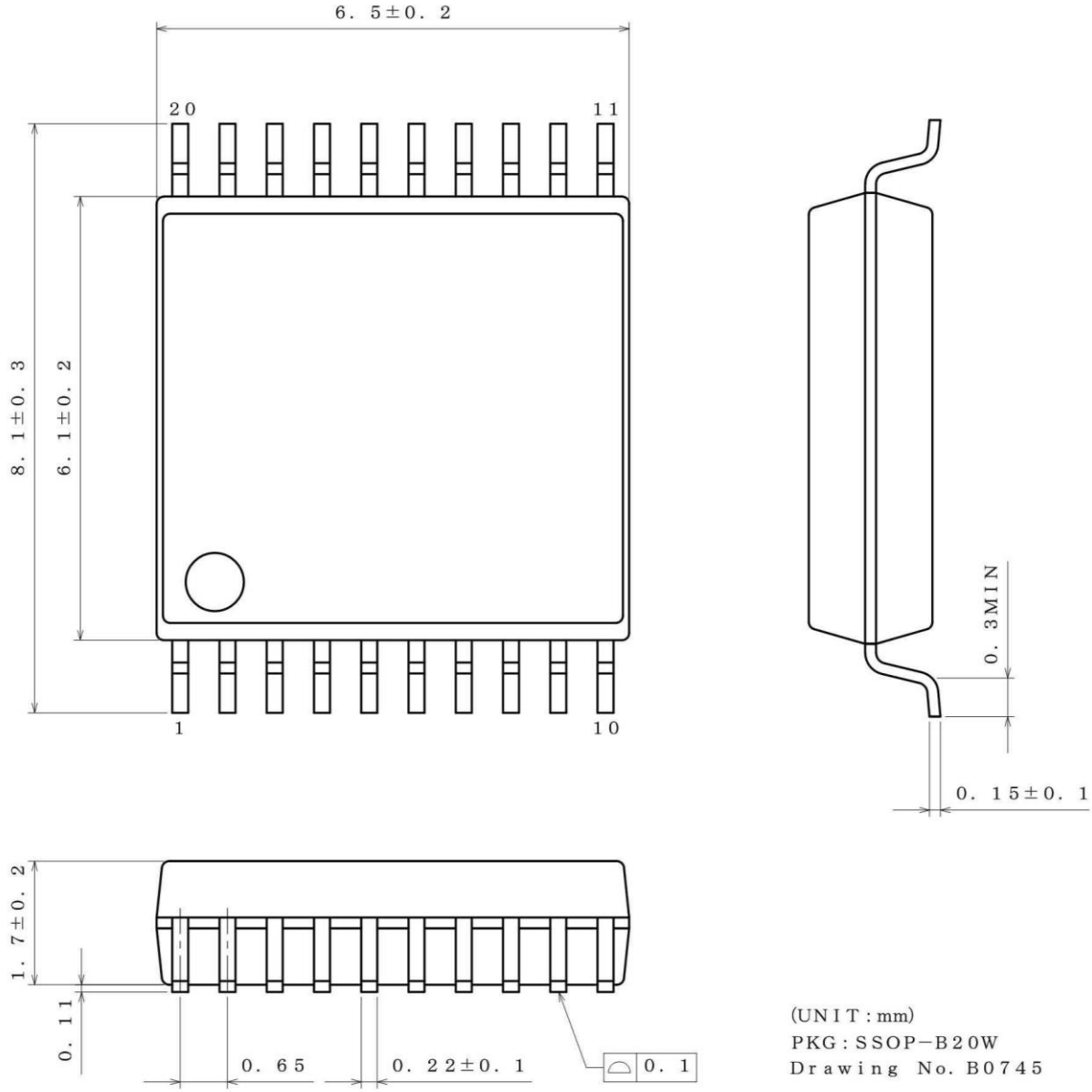
Marking Diagram

SSOP-B20W
TOP VIEW



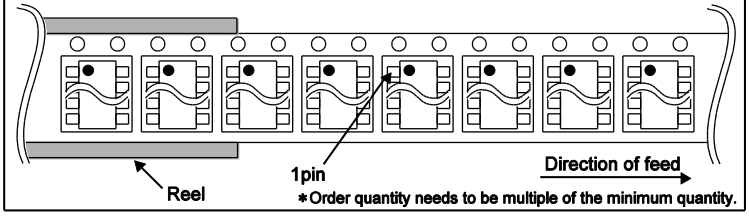
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B20W



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
25.Jun.2012	001	New Release
26.Oct.2012	002	P.3 Fix typo about 4) Under voltage lock out. P.7 Fix typo about figure 8.sequence. P.10 Fix typo about Electrical Characteristics about IN1, IN2 Input inhibition area.
20.Dec.2012	003	P.5~P.8 Fix typo about input inhibition area. P.11 Add minimum propagation delay. P.21 Delete description.
05.Mar.2013	004	P.1 Add a description 4) AEC-Q100 Qualified at Features Applied new style and improved understandability.
25.Dec.2015	005	P.1 Add a description 5) UL1577 Recognized at Features P.9 Add UL1577 Ratings Table

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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Precaution for Disposition

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