

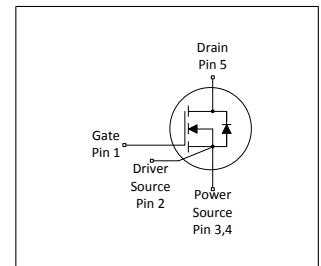
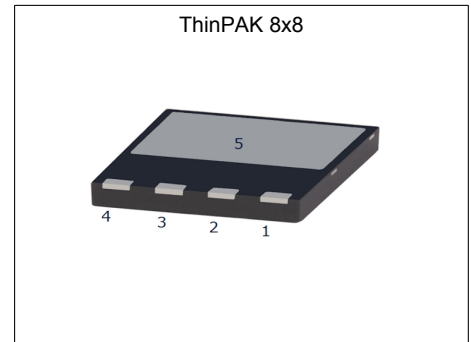
MOSFET

600V CoolMOS™ CP Power Transistor

The CoolMOS™ CP series offers devices which provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler..

ThinPAK

ThinPAK is a new leadless SMD package for HV MOSFETs. The new package has a very small footprint of only 64mm² (vs. 150mm² for the D²PAK) and a very low profile with only 1mm height (vs. 4.4mm for the D²PAK). The significantly smaller package size, combined with benchmark low parasitic inductances, provides designers with a new and effective way to decrease system solution size in power-density driven designs.



Features

- Reduced board space consumption
- Increased power density
- Short commutation loop
- Smooth switching waveform
- easy to use products
- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Qualified according to JEDEC (J-STD20 and JESD22) for target applications (Server, Adapter)
- Pb-free plating, Halogen free

Potential applications

Server, Adapter

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{ds} @ T_{jmax}$	650	V
$R_{DS(on),max}$	0.199	Ω
$Q_{g,typ}$	32	nC
$I_{D,pulse}$	63	A
$E_{oss} @ 400V$	6.1	μJ
Body diode di_F/dt	200	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPL60R199CP	PG-VSON-4	6R199P	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	16.4 10.0	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	63	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	436	mJ	$I_D = 6.6\text{ A}$; $V_{DD} = 50\text{ V}$
Avalanche energy, repetitive ³⁾	E_{AR}	-	-	0.66	mJ	$I_D = 6.6\text{ A}$; $V_{DD} = 50\text{ V}$
Avalanche current, repetitive ³⁾	I_{AR}	-	-	6.6	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 480\text{ V}$
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	139	W	$T_C = 25^\circ\text{C}$
Operating Temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Storage Temperature	T_{stg}	-40	-	125	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	16.4	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	63	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ⁴⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{ V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	200	A/ μs	$V_{DS} = 0 \dots 400\text{ V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ see table 8

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.9	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient ⁵⁾	R_{thJA}	-	-	45	$^\circ\text{C/W}$	SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^\circ\text{C}$	reflow MSL2a

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR} \cdot f$; Pulse width t_p limited by $T_{j,max}$

⁴⁾ Identical low side and high side switch with identical R_G

⁵⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70 μm) for drain connection. PCB is vertical without air stream cooling.

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{ V}$, $I_D=0.25\text{ mA}$
Gate threshold voltage	$V_{(GS)th}$	2.5	3	3.5	V	$V_{DS}=V_{GS}$, $I_D=0.66\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.18 0.47	0.199 -	Ω	$V_{GS}=10\text{ V}$, $I_D=9.9\text{ A}$, $T_j=25\text{ °C}$ $V_{GS}=10\text{ V}$, $I_D=9.9\text{ A}$, $T_j=150\text{ °C}$
Gate resistance	R_G	-	2	-	Ω	$f=1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1520	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	72	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	69	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=0\dots480\text{ V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	180	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{ V}$, $V_{DS}=0\dots480\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=9.9\text{ A}$, $R_G=3.3\Omega$; see table 9
Rise time	t_r	-	5	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=9.9\text{ A}$, $R_G=3.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	50	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=9.9\text{ A}$, $R_G=3.3\Omega$; see table 9
Fall time	t_f	-	5	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=9.9\text{ A}$, $R_G=3.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	$V_{DD}=480\text{ V}$, $I_D=9.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	11	-	nC	$V_{DD}=480\text{ V}$, $I_D=9.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	32	-	nC	$V_{DD}=480\text{ V}$, $I_D=9.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=480\text{ V}$, $I_D=9.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0\text{ V}$, $I_F=9.9\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	340	-	ns	$V_R=400\text{ V}$, $I_F=9.9\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ see table 8
Reverse recovery charge	Q_{rr}	-	5.5	-	μC	$V_R=400\text{ V}$, $I_F=9.9\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ see table 8
Peak reverse recovery current	I_{rrm}	-	33	-	A	$V_R=400\text{ V}$, $I_F=9.9\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ see table 8

4 Electrical characteristics diagrams

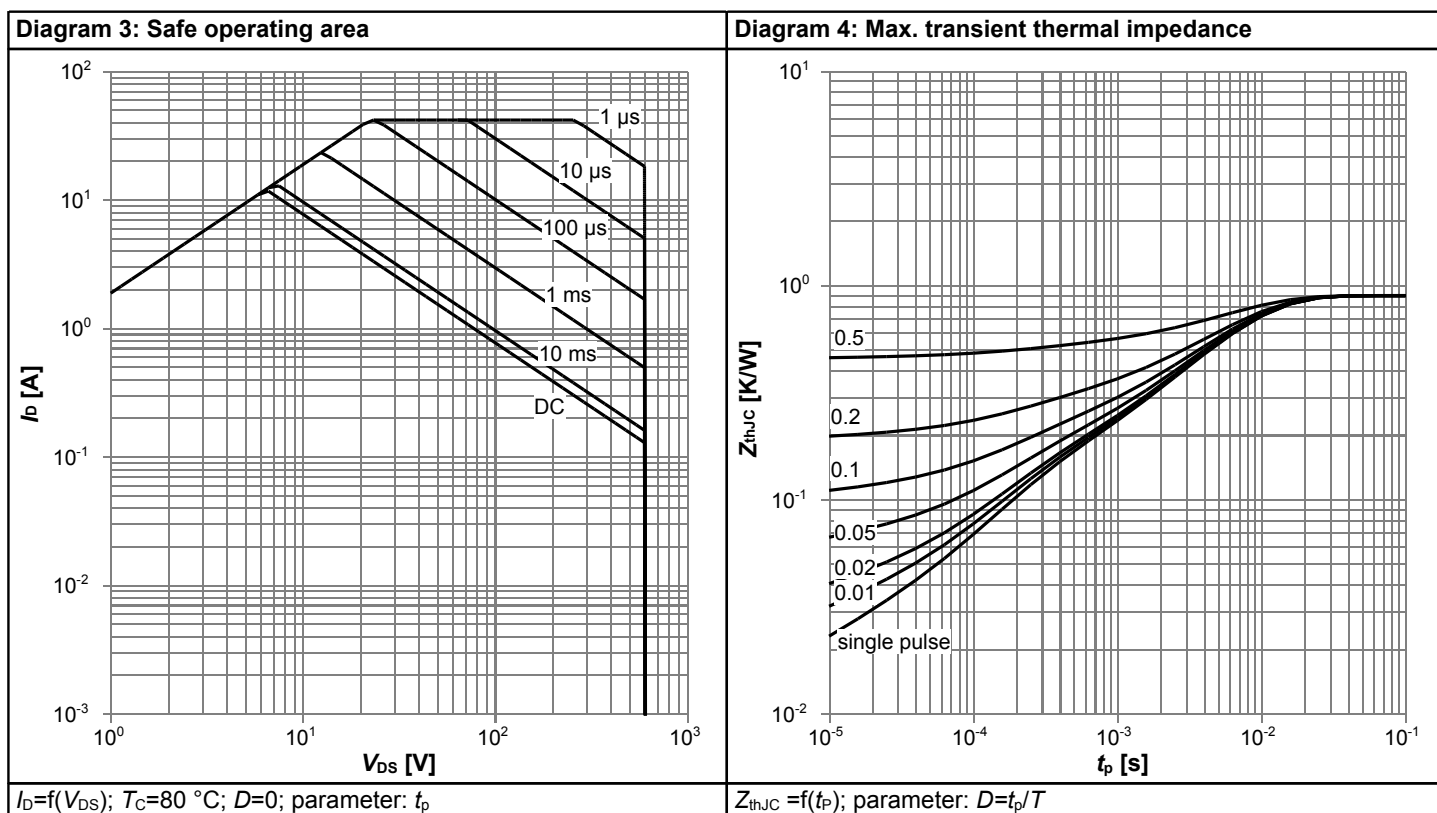
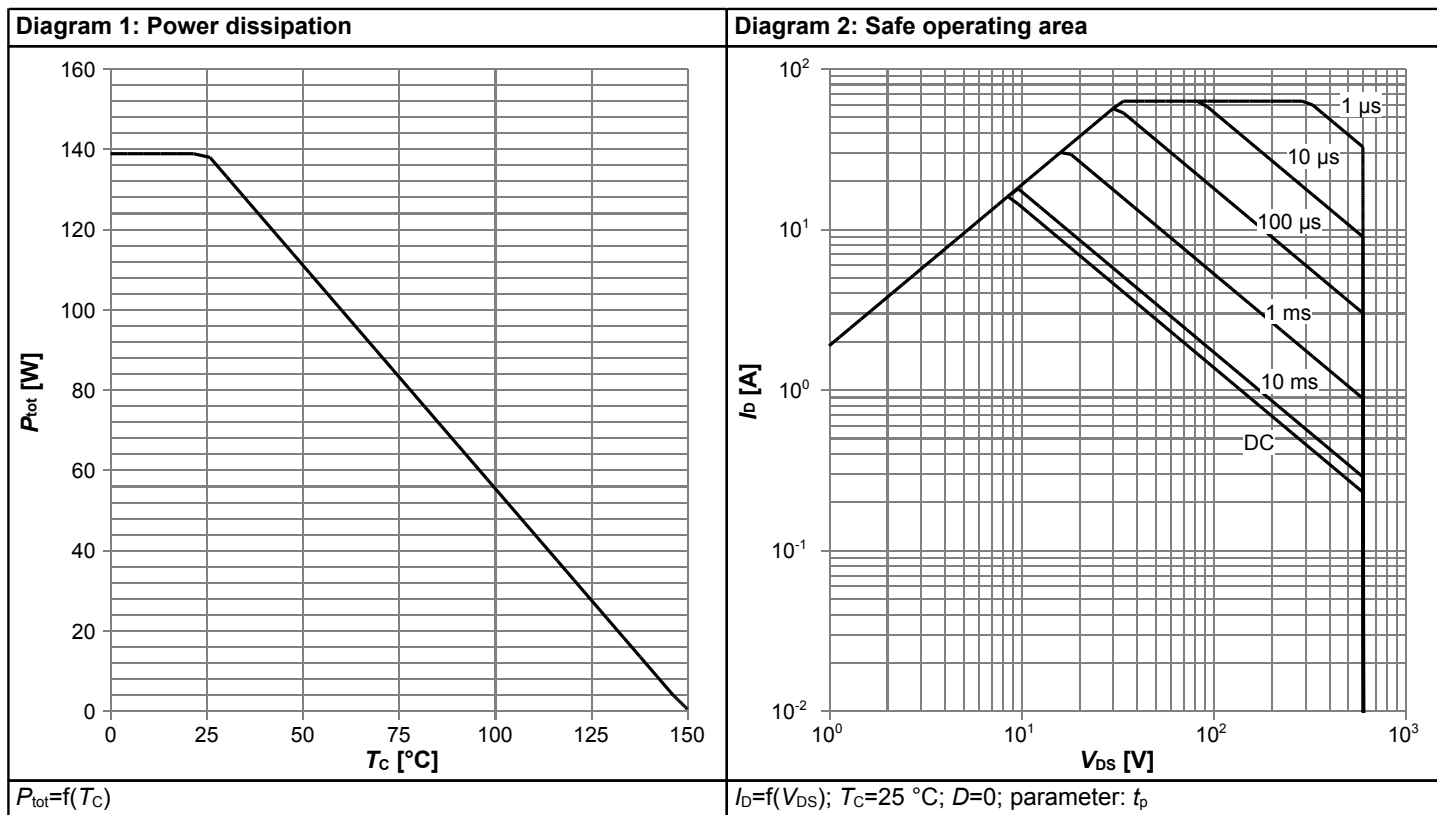
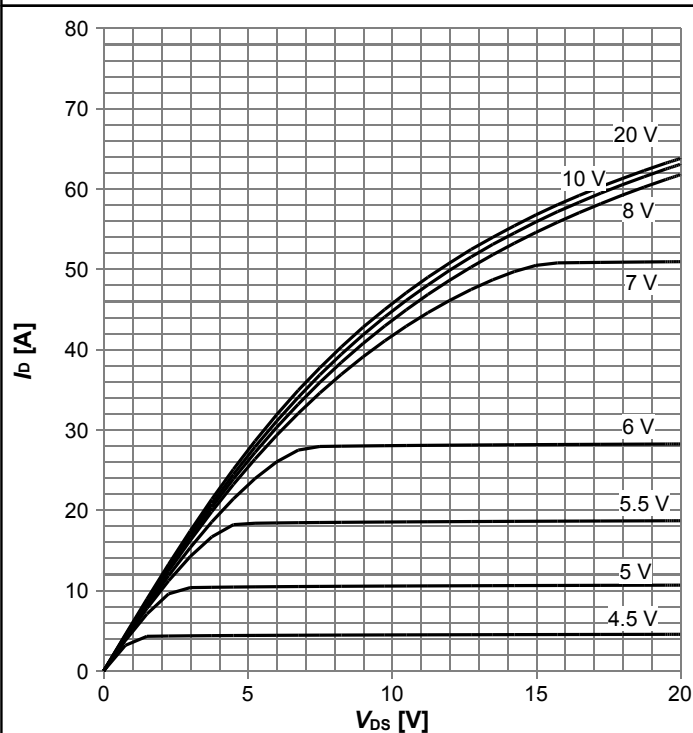
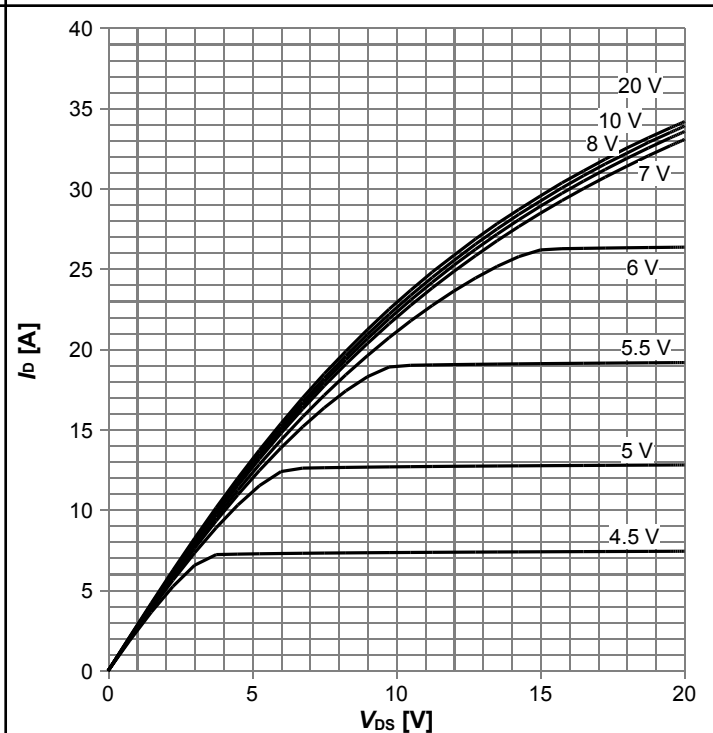


Diagram 5: Typ. output characteristics



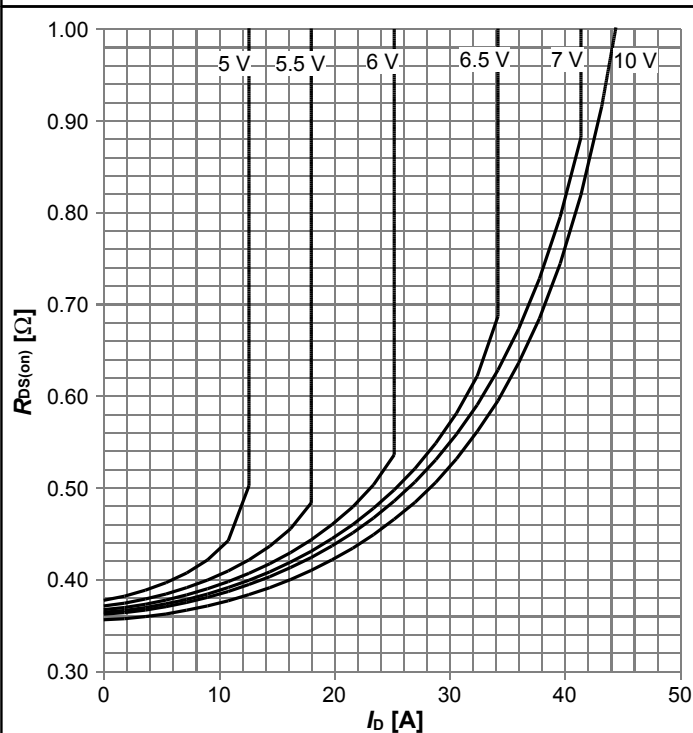
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



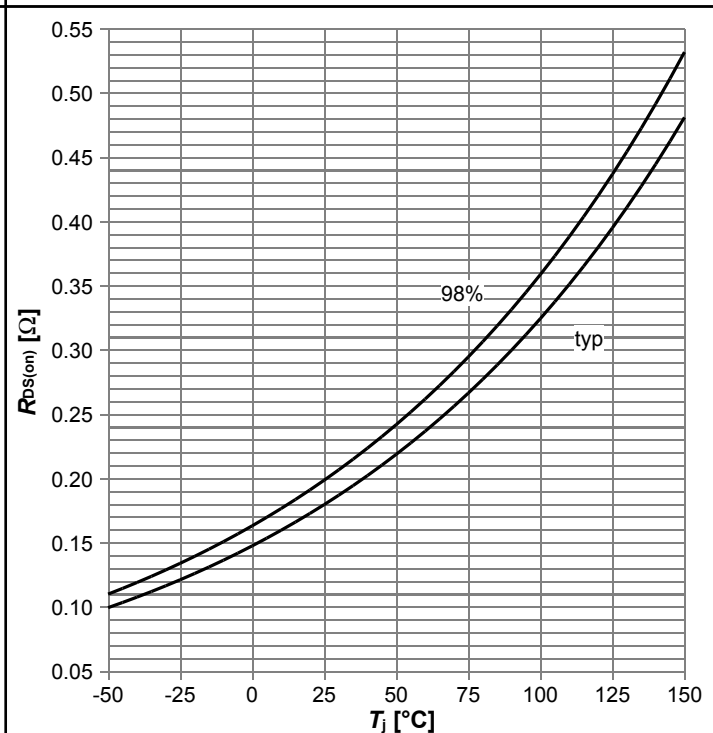
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



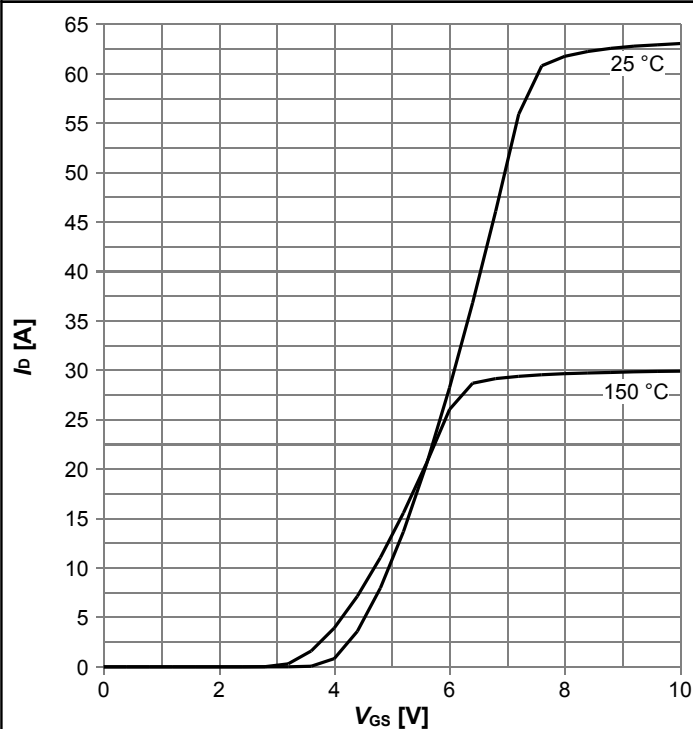
$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



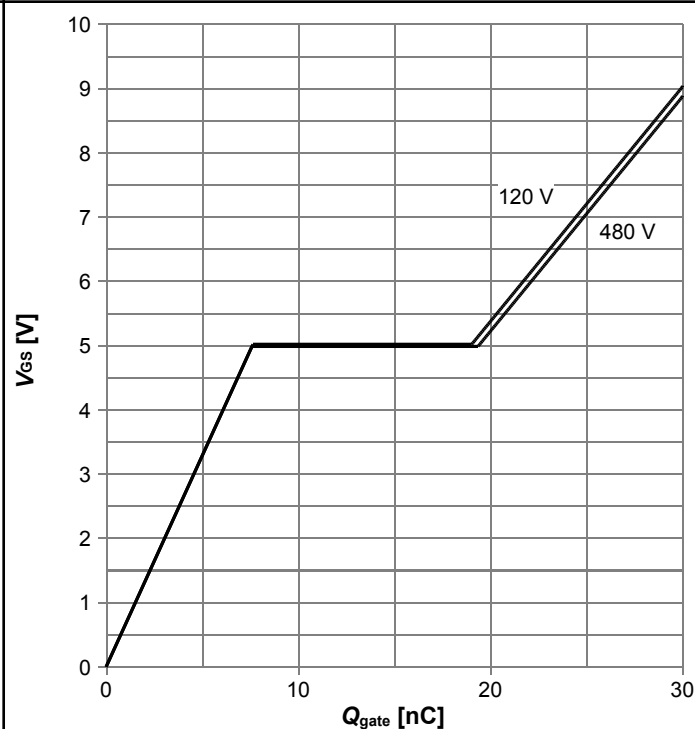
$R_{DS(on)} = f(T_j)$; $I_D = 9.9\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



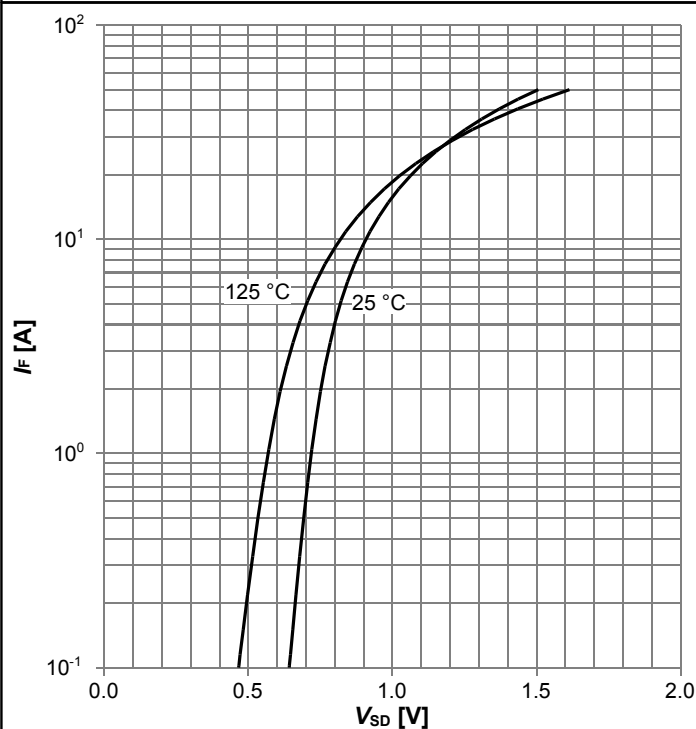
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



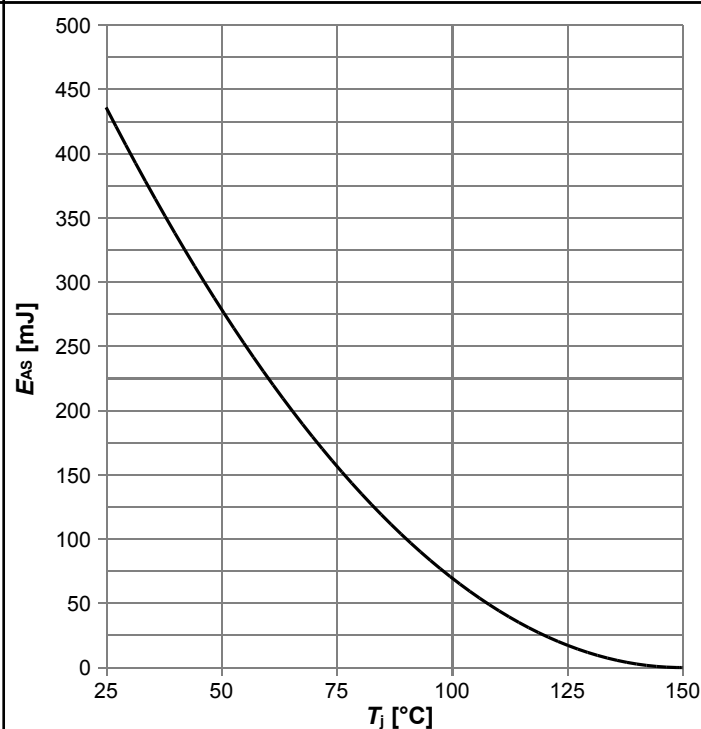
$V_{GS} = f(Q_{gate})$; $I_D = 9.9$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



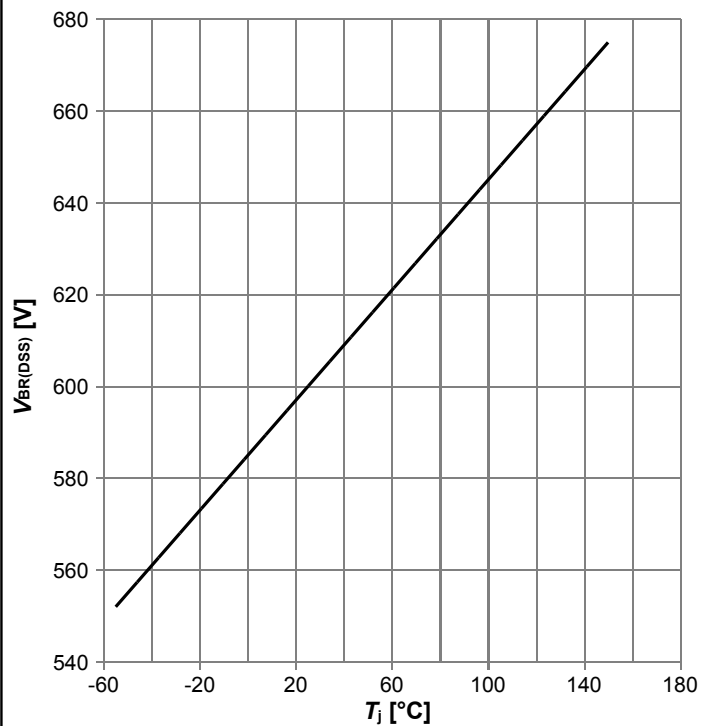
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



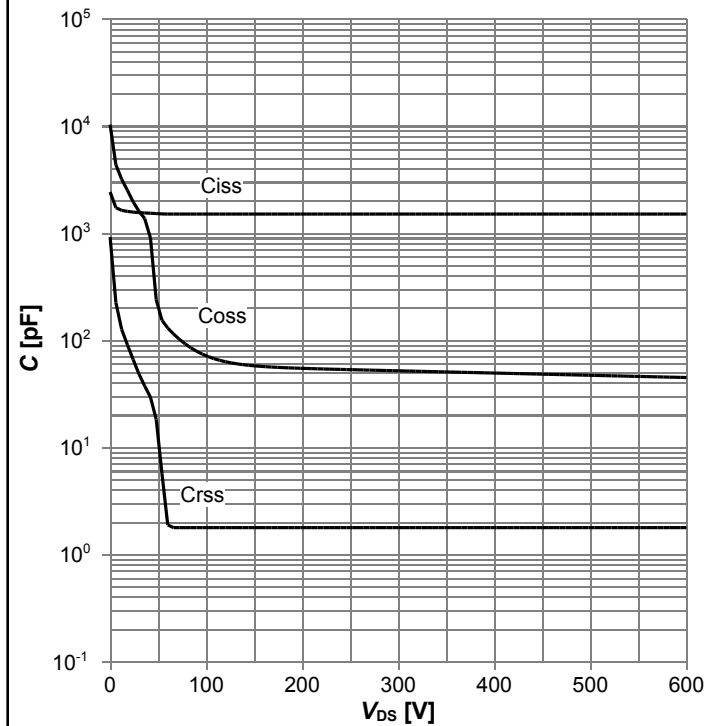
$E_{AS} = f(T_j)$; $I_D = 6.6$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



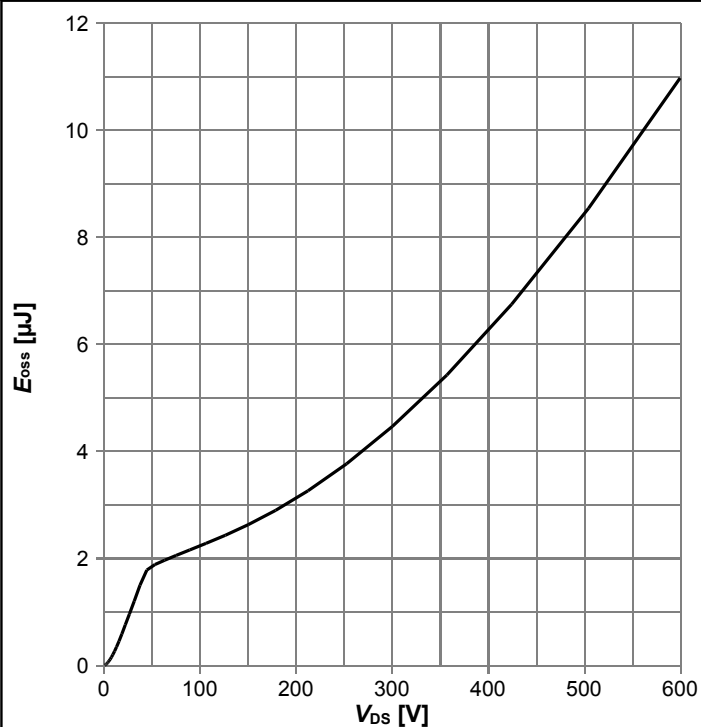
$V_{BR(DSS)} = f(T_J); I_D = 0.25 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

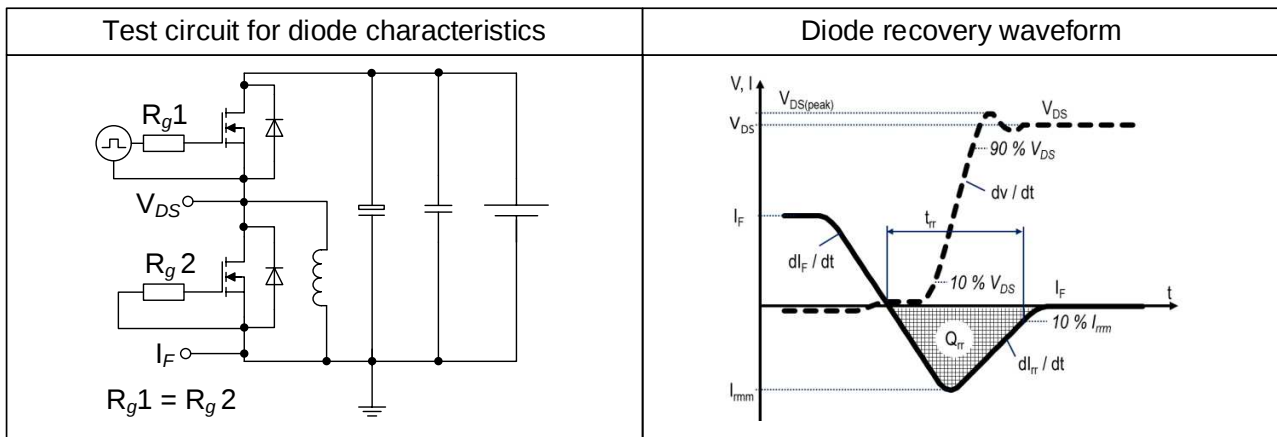


Table 9 switching times (ss)

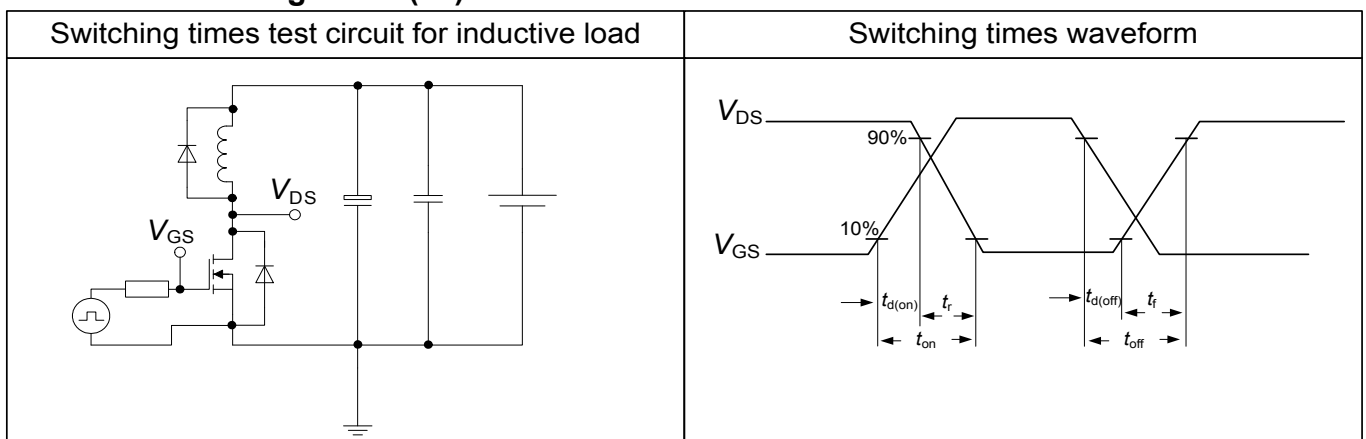
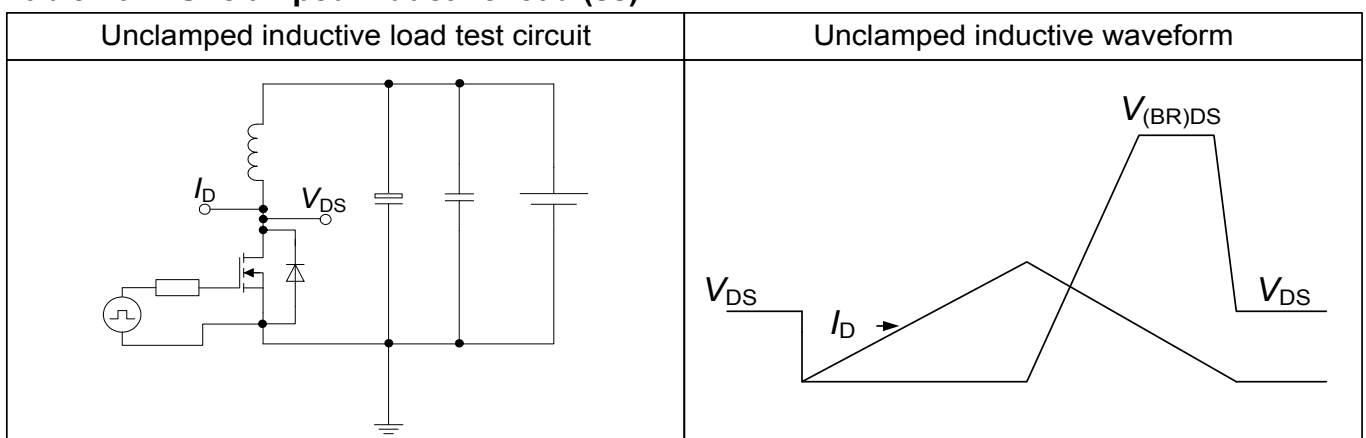


Table 10 Unclamped inductive load (ss)



6 Package Outlines

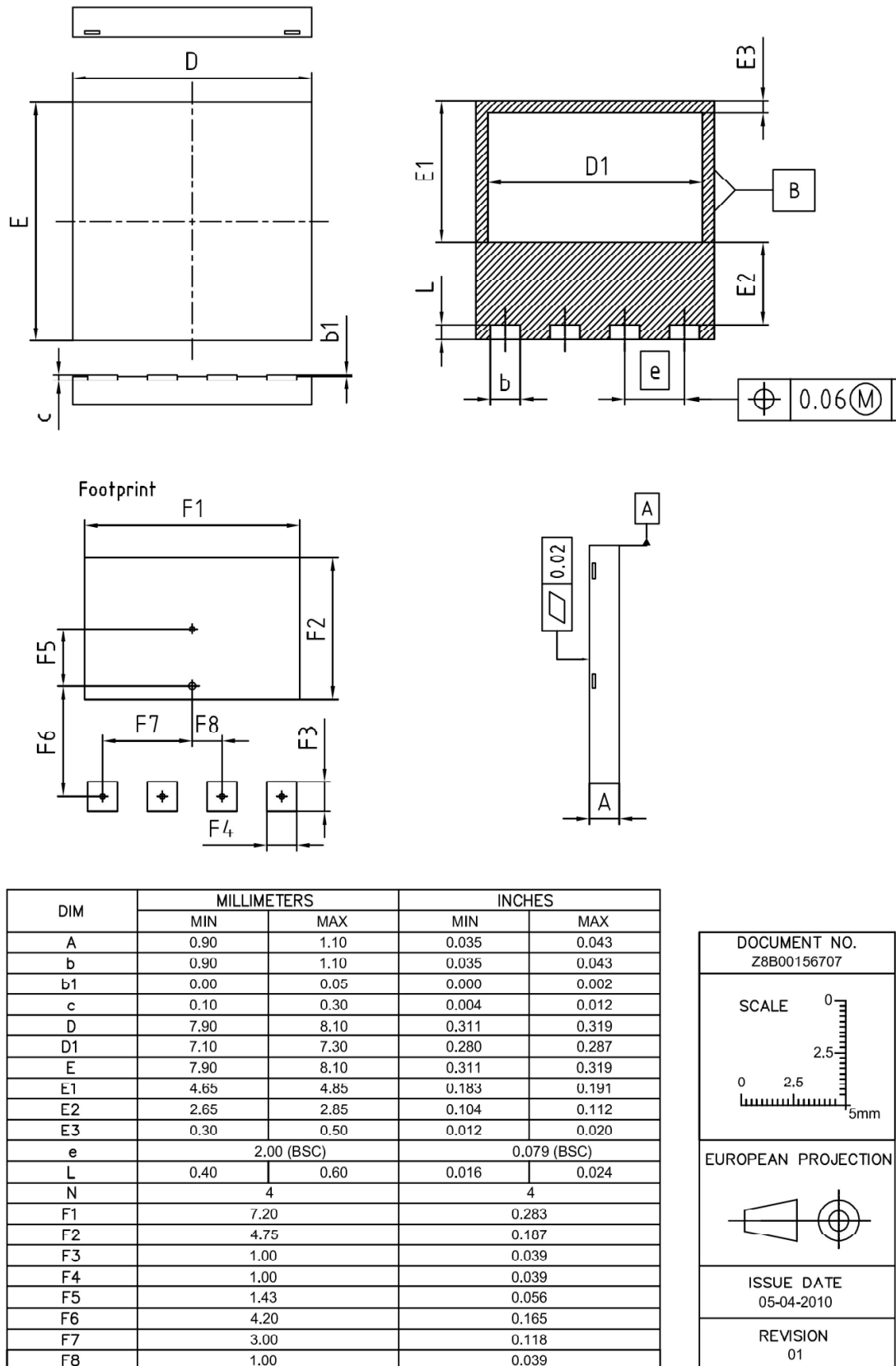


Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPL60R199CP

Revision: 2017-09-06, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2015-10-23	Update of ID pulse according to SOA Diagram on page 2 and 3
2.4	2017-09-06	Updated MSL; style updated

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