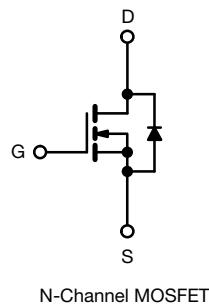


Power MOSFET



PRODUCT SUMMARY

V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.270
Q_g max. (nC)	76	
Q_{gs} (nC)	21	
Q_{gd} (nC)	34	
Configuration	Single	

FEATURES

- Low figure-of-merit $R_{on} \times Q_g$
- 100 % avalanche tested
- High peak current capability
- dv/dt ruggedness
- Improved t_{rr}/Q_{rr}
- Improved gate charge
- High power dissipations capability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free	SiHS20N50C-E3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C) ^a	V_{GS} at 10 V	20	A
		11	
Pulsed drain current ^b	I_{DM}	80	
Linear derating factor		1.8	W/°C
Single pulse avalanche energy ^c	E_{AS}	361	mJ
Maximum power dissipation	P_D	250	W
Reverse diode dv/dt ^d	dv/dt	5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

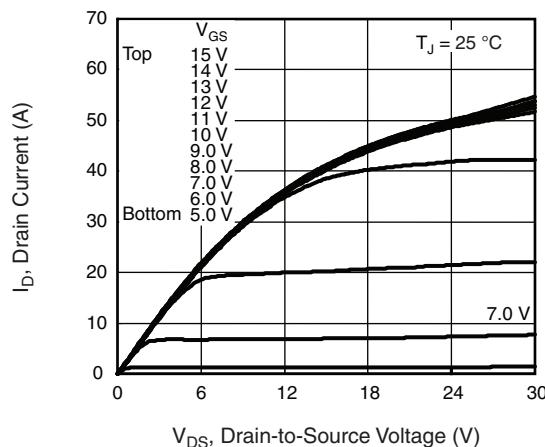
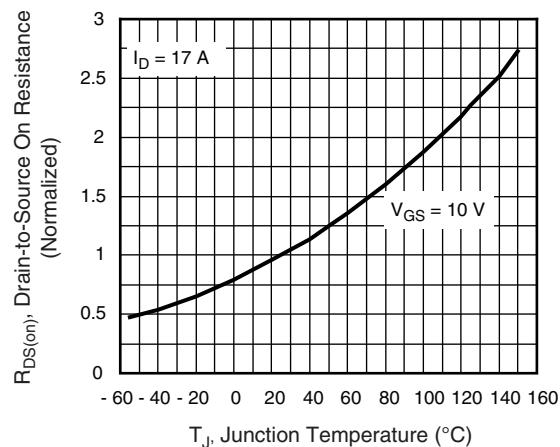
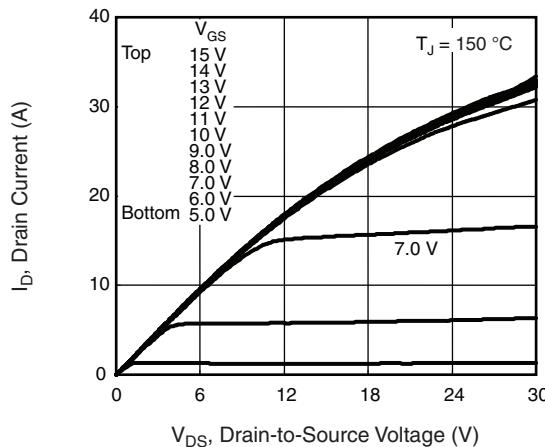
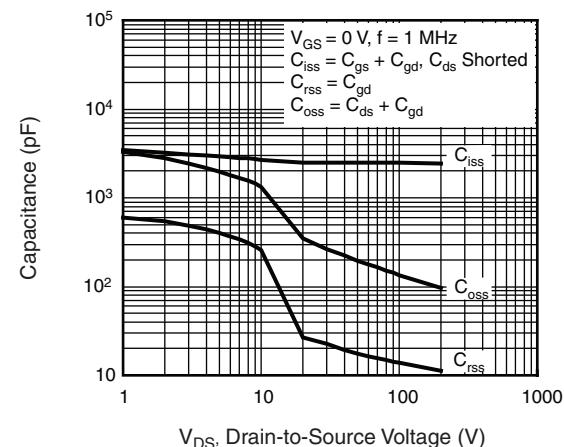
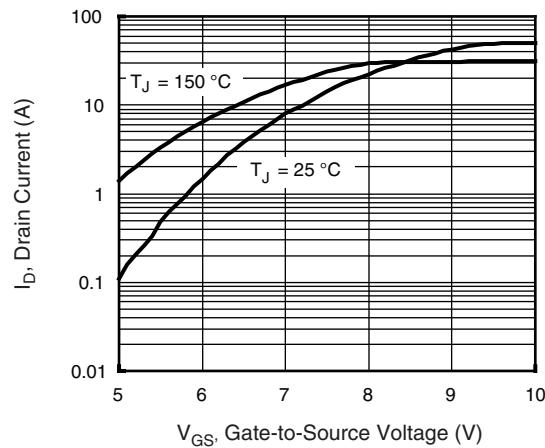
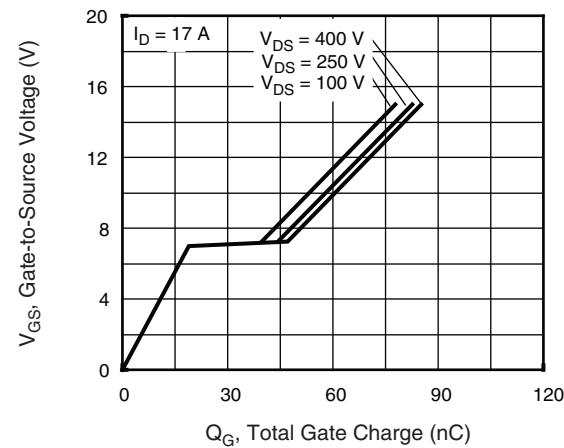
Notes

- Limited by maximum junction temperature
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.5$ mH, $R_g = 25$ Ω, $I_{AS} = 17$ A
- $I_{SD} \leq 18$ A, $di/dt \leq 380$ A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.5	

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		500	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1\text{ mA}$		-	0.7	-	$\text{V}/^\circ\text{C}$	
Gate-source threshold voltage (N)	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V	
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA	
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$		-	-	250		
Drain-source on-state resistance	$R_{DS(\text{on})}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$	-	0.225	0.270	Ω	
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 10\text{ A}$		-	6.4	-	S	
Dynamic								
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$		-	2451	2942	pF	
Output capacitance	C_{oss}			-	300	360		
Reverse transfer capacitance	C_{rss}			-	26	32		
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 18\text{ A}$, $V_{DS} = 400\text{ V}$	-	65	76	nC	
Gate-source charge	Q_{gs}			-	21	-		
Gate-drain charge	Q_{gd}			-	29	-		
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 250\text{ V}$, $I_D = 18\text{ A}$, $R_g = 9.1\text{ }\Omega$		-	80	-	ns	
Rise time	t_r			-	27	-		
Turn-off delay time	$t_{d(\text{off})}$			-	32	-		
Fall time	t_f			-	44	-		
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain		-	1.1	-	Ω	
Drain-Source Body Diode Characteristics								
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	A	
Pulsed diode forward current	I_{SM}			-	-	80		
Diode forward voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = 18\text{ A}$, $V_{GS} = 0\text{ V}$		-	-	1.5	V	
Reverse recovery time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = I_S$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 35\text{ V}$		-	503	-	ns	
Reverse recovery charge	Q_{rr}			-	6.7	-		
Reverse recovery current	I_{RRM}			-	30	-		

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25 \text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics, $T_C = 150 \text{ }^\circ\text{C}$

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

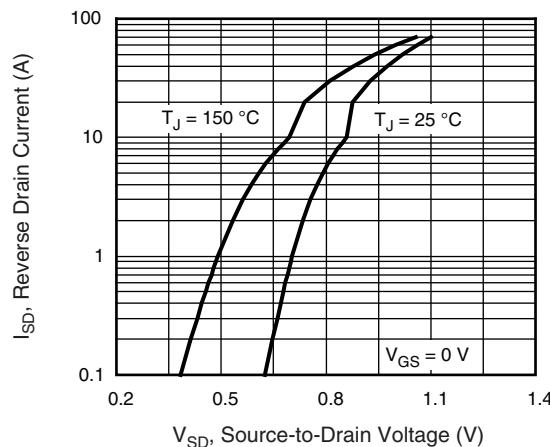


Fig. 7 - Typical Source-Drain Diode Forward Voltage

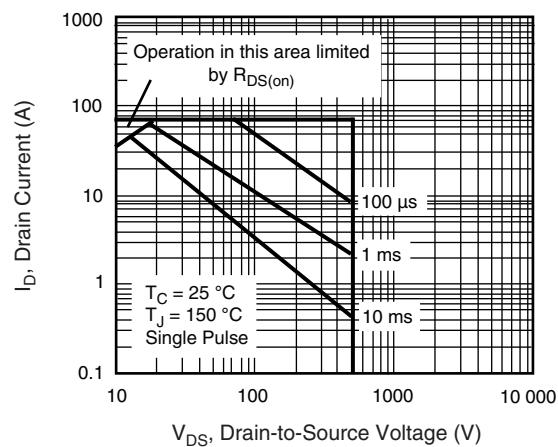


Fig. 8 - Maximum Safe Operating Area

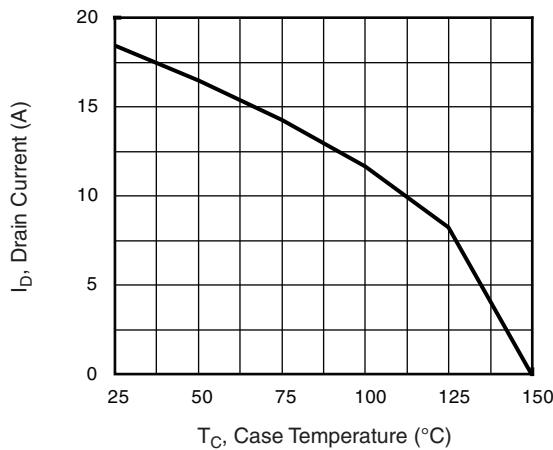


Fig. 9 - Maximum Drain Current vs. Case Temperature

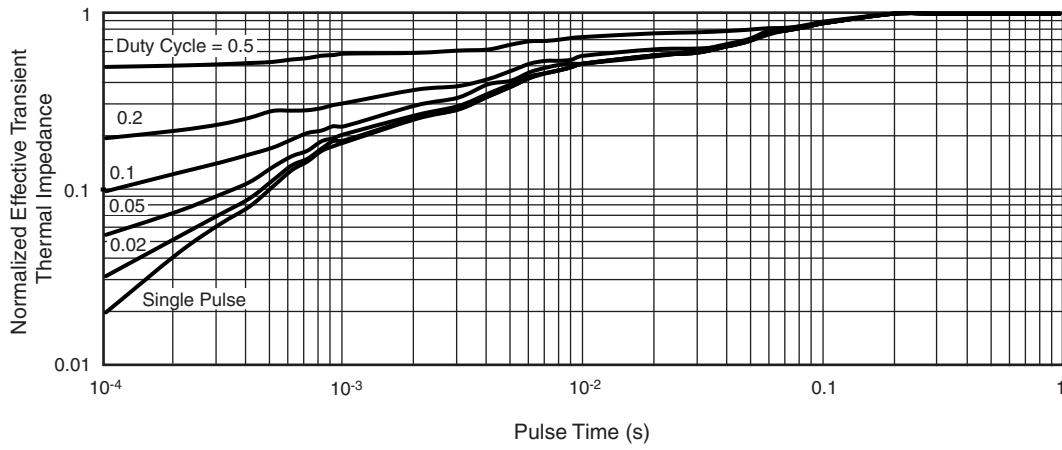


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case (Super-247)

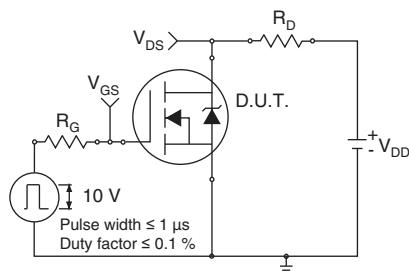


Fig. 11 - Switching Time Test Circuit

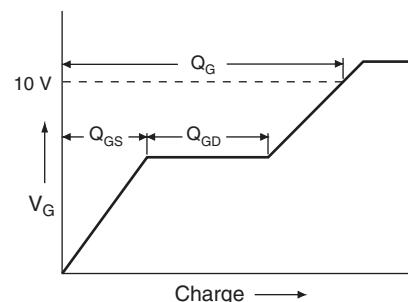


Fig. 15 - Basic Gate Charge Waveform

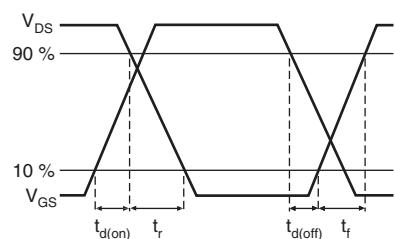


Fig. 12 - Switching Time Waveforms

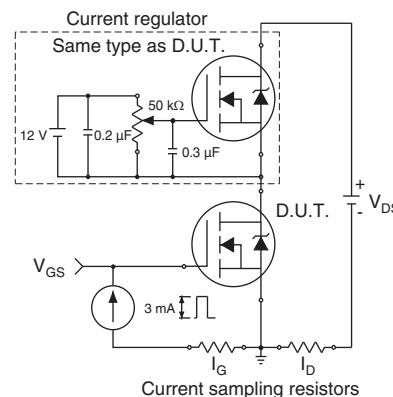


Fig. 16 - Gate Charge Test Circuit

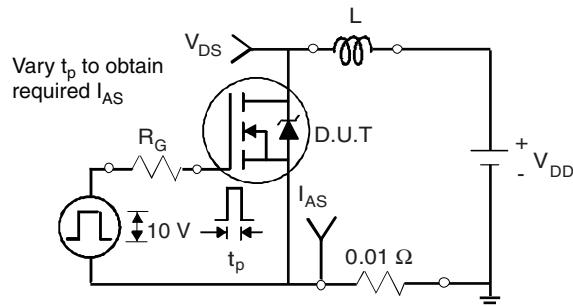


Fig. 13 - Unclamped Inductive Test Circuit

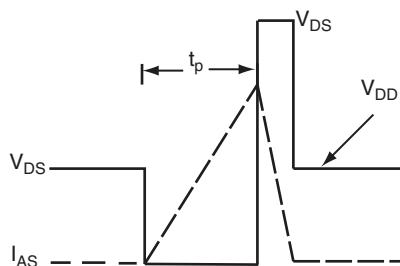
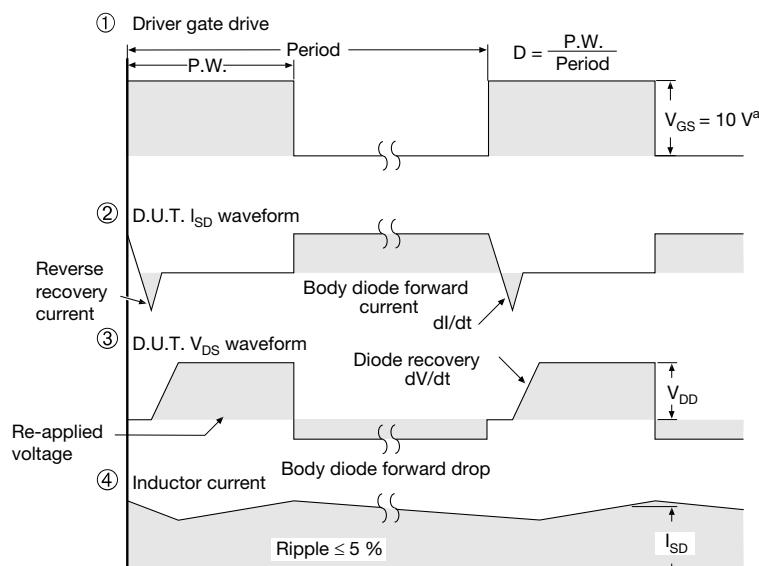
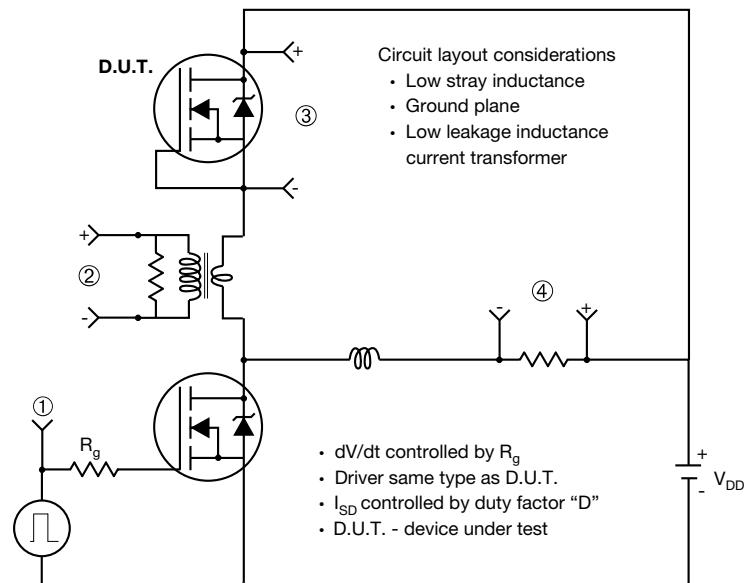


Fig. 14 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 17 - For N-Channel

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