

# GTL2002

## 2-bit bidirectional low voltage translator

Rev. 8 — 19 August 2013

Product data sheet

### 1. General description

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The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2002 provides 2 NMOS pass transistors (Sn and Dn) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bidirectional voltage translations between 1.0 V and 5.0 V without use of a direction pin.

When the Sn or Dn port is LOW the clamp is in the ON-state and a low resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH, the voltage on the Sn port is limited to the voltage set by the reference transistor (SREF). When the Sn port is HIGH, the Dn port is pulled to  $V_{CC}$  by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other two matched Sn/Dn transistors, allowing for easier board layout. The translator's transistors provide excellent ESD protection to lower voltage devices and at the same time protect less ESD-resistant devices.

### 2. Features and benefits

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- 2-bit bidirectional low voltage translator
- Allows voltage level translation between 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5 V buses, which allows direct interface with GTL, GTL+, LVTTTL/TTL and 5 V CMOS levels
- Provides bidirectional voltage translation with no direction pin
- Low 6.5  $\Omega$  ON-state resistance ( $R_{on}$ ) between input and output pins (Sn/Dn)
- Supports hot insertion
- No power supply required; will not latch up
- 5 V tolerant inputs
- Low standby current
- Flow-through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Packages offered: SO8, TSSOP8 (MSOP8), VSSOP8, XQFN8



### 3. Applications

- Any application that requires bidirectional or unidirectional voltage level translation from any voltage between 1.0 V and 5.0 V to any voltage between 1.0 V and 5.0 V
- The open-drain construction with no direction pin is ideal for bidirectional low voltage (e.g., 1.0 V, 1.2 V, 1.5 V, or 1.8 V) processor I<sup>2</sup>C-bus port translation to the normal 3.3 V or 5.0 V I<sup>2</sup>C-bus signal levels or GTL/GTL+ translation to LVTTTL/TTL signal levels.

### 4. Ordering information

**Table 1. Ordering information**

| Type number | Topside marking    | Package               |                                                                                          |          |
|-------------|--------------------|-----------------------|------------------------------------------------------------------------------------------|----------|
|             |                    | Name                  | Description                                                                              | Version  |
| GTL2002D    | GTL2002            | SO8                   | plastic small outline package; 8 leads; body width 3.9 mm                                | SOT96-1  |
| GTL2002DP   | 2002               | TSSOP8 <sup>[1]</sup> | plastic thin shrink small outline package; 8 leads; body width 3 mm                      | SOT505-1 |
| GTL2002DC   | 2002               | VSSOP8                | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm               | SOT765-1 |
| GTL2002GM   | G2X <sup>[2]</sup> | XQFN8                 | plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm | SOT902-2 |

[1] Also known as MSOP8.

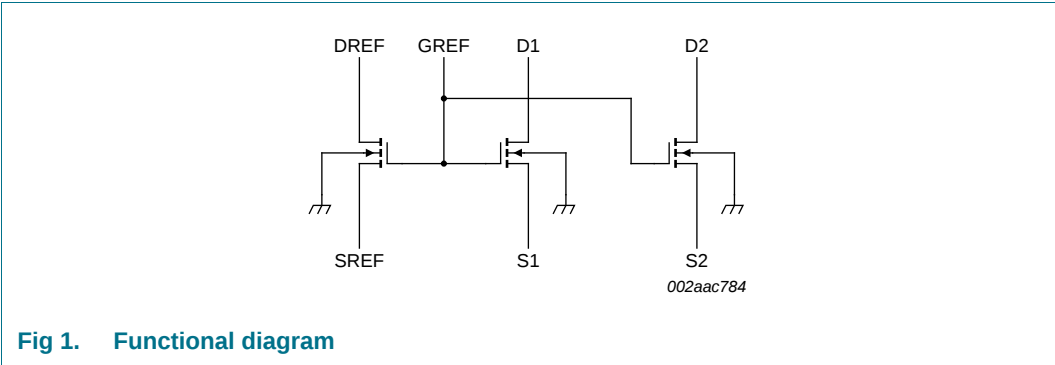
[2] 'X' will change based on date code.

#### 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method                                  | Minimum order quantity | Temperature                         |
|-------------|-----------------------|---------|-------------------------------------------------|------------------------|-------------------------------------|
| GTL2002D    | GTL2002D,112          | SO8     | Standard marking<br>* IC's tube - DSC bulk pack | 2000                   | T <sub>amb</sub> = -40 °C to +85 °C |
| GTL2002D    | GTL2002D,118          | SO8     | Reel 13" Q1/T1<br>*Standard mark SMD            | 2500                   | T <sub>amb</sub> = -40 °C to +85 °C |
| GTL2002DP   | GTL2002DP,118         | TSSOP8  | Reel 13" Q1/T1<br>*Standard mark SMD            | 2500                   | T <sub>amb</sub> = -40 °C to +85 °C |
| GTL2002DC   | GTL2002DC,125         | VSSOP8  | Reel 7" Q3/T4<br>*Standard mark                 | 3000                   | T <sub>amb</sub> = -40 °C to +85 °C |
| GTL2002GM   | GTL2002GM,125         | XQFN8   | Reel 7" Q3/T4<br>*Standard mark                 | 4000                   | T <sub>amb</sub> = -40 °C to +85 °C |

5. Functional diagram



6. Pinning information

6.1 Pinning

Pin configuration for SO8 package. The chip is labeled GTL2002D. The pins are numbered 1 to 8. The connections are: 1 GND, 2 SREF, 3 S1, 4 S2, 5 D2, 6 D1, 7 DREF, 8 GREF. The diagram is labeled 002aac777.

**Fig 2. Pin configuration for SO8**

Pin configuration for TSSOP8 (MSOP8) package. The chip is labeled GTL2002DP. The pins are numbered 1 to 8. The connections are: 1 GND, 2 SREF, 3 S1, 4 S2, 5 D2, 6 D1, 7 DREF, 8 GREF. The diagram is labeled 002aac778.

**Fig 3. Pin configuration for TSSOP8 (MSOP8)**

Pin configuration for VSSOP8 package. The chip is labeled GTL2002DC. The pins are numbered 1 to 8. The connections are: 1 SREF, 2 S1, 3 S2, 4 GND, 5 D2, 6 D1, 7 DREF, 8 GREF. The diagram is labeled 002aac779.

**Fig 4. Pin configuration for VSSOP8**

Pin configuration for XQFN8 package. The chip is labeled GTL2002GM. The pins are numbered 1 to 8. The connections are: 1 GND, 2 SREF, 3 S1, 4 S2, 5 D2, 6 D1, 7 DREF, 8 GREF. The diagram is labeled 002aac780. A terminal 1 index area is indicated.

**Fig 5. Pin configuration for XQFN8**

## 6.2 Pin description

Table 3. Pin description

| Symbol | Pin                 |        | Description                    |
|--------|---------------------|--------|--------------------------------|
|        | SO8, TSSOP8, XQFN8U | VSSOP8 |                                |
| GND    | 1                   | 4      | ground (0 V)                   |
| SREF   | 2                   | 1      | source of reference transistor |
| S1     | 3                   | 2      | port S1                        |
| S2     | 4                   | 3      | port S2                        |
| D2     | 5                   | 5      | port D2                        |
| D1     | 6                   | 6      | port D1                        |
| DREF   | 7                   | 7      | drain of reference transistor  |
| GREF   | 8                   | 8      | gate of reference transistor   |

## 7. Functional description

Refer to [Figure 1 “Functional diagram”](#).

### 7.1 Function selection

Table 4. Function selection, HIGH to LOW translation

Assuming  $D_n$  is at the higher voltage level.

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

| GREF <sup>[1]</sup> | DREF | SREF                                 | Input $D_n$ | Output $S_n$               | Transistor |
|---------------------|------|--------------------------------------|-------------|----------------------------|------------|
| H                   | H    | 0 V                                  | X           | X                          | off        |
| H                   | H    | $V_{TT}$ <sup>[4]</sup>              | H           | $V_{TT}$ <sup>[2][4]</sup> | on         |
| H                   | H    | $V_{TT}$ <sup>[4]</sup>              | L           | L <sup>[3]</sup>           | on         |
| L                   | L    | $0\text{ V} - V_{TT}$ <sup>[4]</sup> | X           | X                          | off        |

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2]  $S_n$  is not pulled up or pulled down.

[3]  $S_n$  follows the  $D_n$  input LOW.

[4]  $V_{TT}$  is equal to the SREF voltage.

Table 5. Function selection, LOW to HIGH translation

Assuming  $D_n$  is at the higher voltage level.

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

| GREF <sup>[1]</sup> | DREF | SREF                                 | Input $S_n$             | Output $D_n$     | Transistor |
|---------------------|------|--------------------------------------|-------------------------|------------------|------------|
| H                   | H    | 0 V                                  | X                       | X                | off        |
| H                   | H    | $V_{TT}$ <sup>[4]</sup>              | $V_{TT}$ <sup>[4]</sup> | H <sup>[2]</sup> | nearly off |
| H                   | H    | $V_{TT}$ <sup>[4]</sup>              | L                       | L <sup>[3]</sup> | on         |
| L                   | L    | $0\text{ V} - V_{TT}$ <sup>[4]</sup> | X                       | X                | off        |

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2]  $D_n$  is pulled up to  $V_{CC}$  through an external resistor.

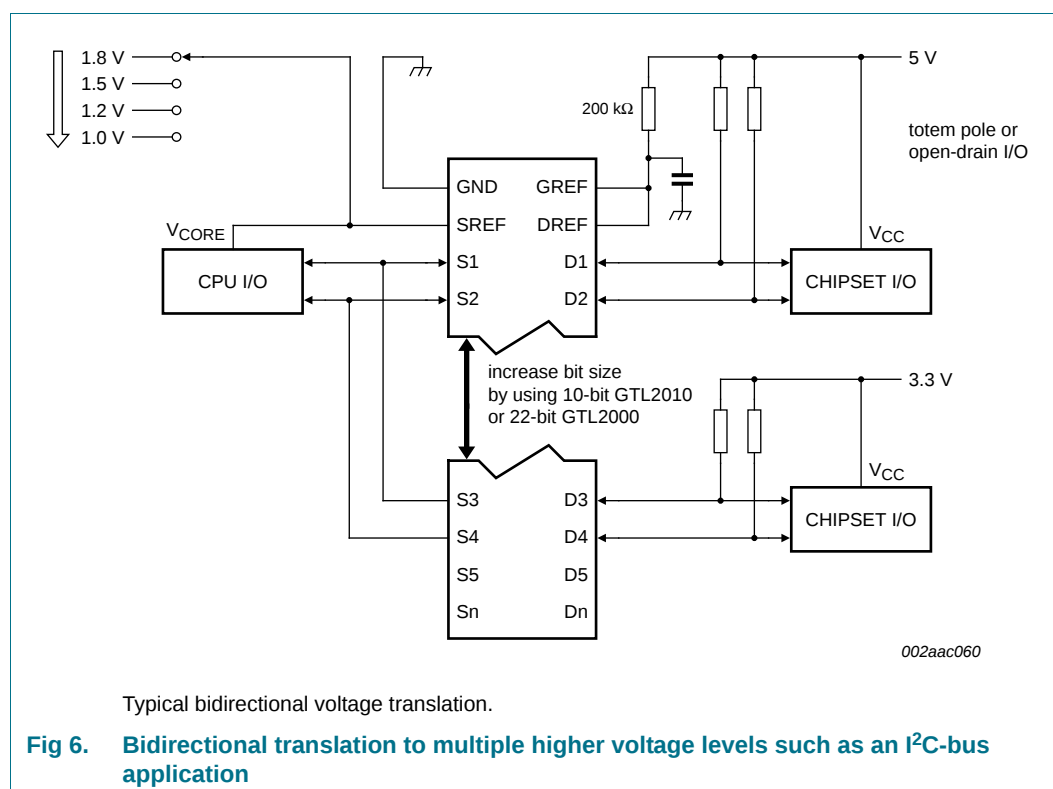
[3]  $D_n$  follows the  $S_n$  input LOW.

[4]  $V_{TT}$  is equal to the SREF voltage.

## 8. Application design-in information

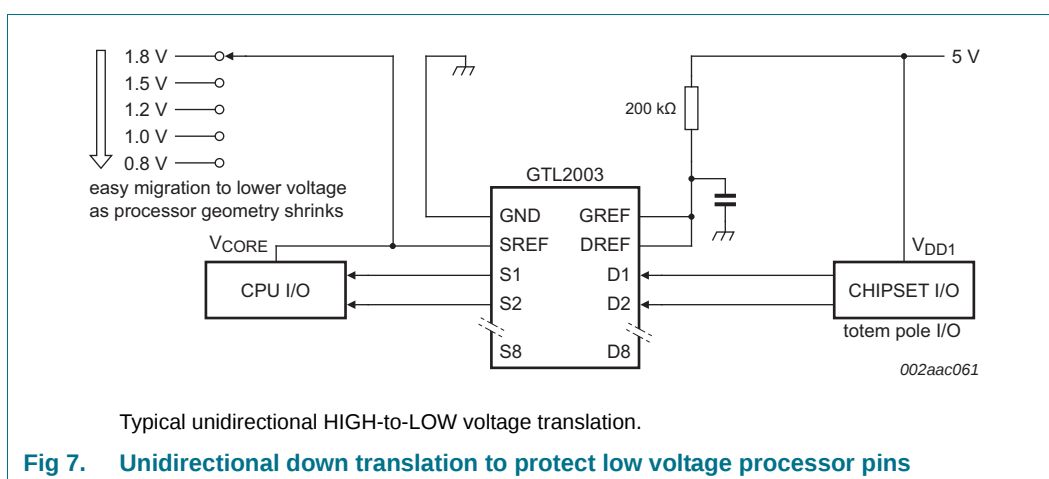
### 8.1 Bidirectional translation

For the bidirectional clamping configuration, higher voltage to lower voltage or lower voltage to higher voltage, the GREF input must be connected to DREF and both pins pulled to HIGH side  $V_{CC}$  through a pull-up resistor (typically 200 k $\Omega$ ). A filter capacitor on DREF is recommended. The processor output can be totem pole or open-drain (pull-up resistors may be required) and the chip set output can be totem pole or open-drain (pull-up resistors are required to pull the Dn outputs to  $V_{CC}$ ). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and the outputs must be controlled by some direction control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed. The opposite side of the reference transistor (SREF) is connected to the processor core power supply voltage. When DREF is connected through a 200 k $\Omega$  resistor to a 3.3 V to 5.5 V  $V_{CC}$  supply and SREF is set between 1.0 V to ( $V_{CC} - 1.5$  V), the output of each Sn has a maximum output voltage equal to SREF and the output of each Dn has a maximum output voltage equal to  $V_{CC}$ .



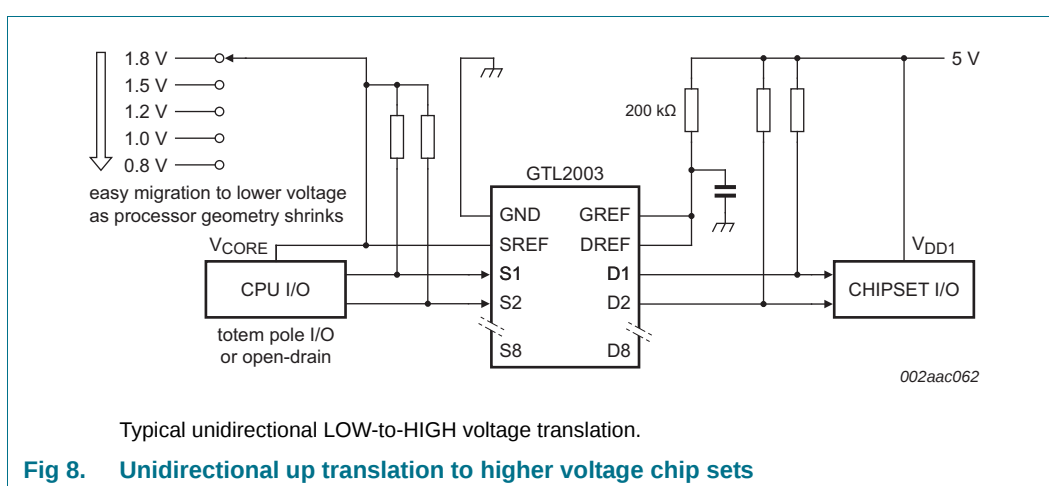
## 8.2 Unidirectional down translation

For unidirectional clamping, higher voltage to lower voltage, the GREF input must be connected to DREF and both pins pulled to the higher side  $V_{CC}$  through a pull-up resistor (typically 200 k $\Omega$ ). A filter capacitor on DREF is recommended. Pull-up resistors are required if the chip set I/O are open-drain. The opposite side of the reference transistor (SREF) is connected to the processor core supply voltage. When DREF is connected through a 200 k $\Omega$  resistor to a 3.3 V to 5.5 V  $V_{CC}$  supply and SREF is set between 1.0 V to ( $V_{CC} - 1.5$  V), the output of each  $S_n$  has a maximum output voltage equal to SREF.



## 8.3 Unidirectional up translation

For unidirectional up translation, lower voltage to higher voltage, the reference transistor is connected the same as for a down translation. A pull-up resistor is required on the higher voltage side ( $D_n$  or  $S_n$ ) to get the full HIGH level, since the GTL-TVC device will only pass the reference source (SREF) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pull-up resistors if it is open-drain.



## 8.4 Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This will guarantee a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage will also be higher in the ON state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as shown in [Equation 1](#):

$$\text{resistor value } (\Omega) = \frac{\text{pull-up voltage (V)} - 0.35 \text{ V}}{0.015 \text{ A}} \quad (1)$$

[Table 6](#) summarizes resistor values for various reference voltages and currents at 15 mA and also at 10 mA and 3 mA. The resistor value shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL-TVC device at 0.175 V, although the 15 mA only applies to current flowing through the GTL-TVC device. See application note AN10145, "Bidirectional low voltage translators" for more information.

**Table 6. Pull-up resistor values**

| Voltage | Pull-up resistor value ( $\Omega$ ) <sup>[1]</sup> |                       |                      |                       |                     |                       |
|---------|----------------------------------------------------|-----------------------|----------------------|-----------------------|---------------------|-----------------------|
|         | 15 mA <sup>[2]</sup>                               |                       | 10 mA <sup>[2]</sup> |                       | 3 mA <sup>[2]</sup> |                       |
|         | Nominal                                            | + 10 % <sup>[3]</sup> | Nominal              | + 10 % <sup>[3]</sup> | Nominal             | + 10 % <sup>[3]</sup> |
| 5.0 V   | 310                                                | 341                   | 465                  | 512                   | 1550                | 1705                  |
| 3.3 V   | 197                                                | 217                   | 295                  | 325                   | 983                 | 1082                  |
| 2.5 V   | 143                                                | 158                   | 215                  | 237                   | 717                 | 788                   |
| 1.8 V   | 97                                                 | 106                   | 145                  | 160                   | 483                 | 532                   |
| 1.5 V   | 77                                                 | 85                    | 115                  | 127                   | 383                 | 422                   |
| 1.2 V   | 57                                                 | 63                    | 85                   | 94                    | 283                 | 312                   |

[1] Calculated for  $V_{OL} = 0.35 \text{ V}$ .

[2] Assumes output driver  $V_{OL} = 0.175 \text{ V}$  at stated current.

[3] + 10 % to compensate for  $V_{DD}$  range and resistor tolerance.

## 9. Limiting values

**Table 7. Limiting values<sup>[1]</sup>**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol            | Parameter                       | Conditions           | Min                 | Max  | Unit |
|-------------------|---------------------------------|----------------------|---------------------|------|------|
| V <sub>SREF</sub> | voltage on pin SREF             |                      | <sup>[2]</sup> -0.5 | +7.0 | V    |
| V <sub>DREF</sub> | voltage on pin DREF             |                      | <sup>[2]</sup> -0.5 | +7.0 | V    |
| V <sub>GREF</sub> | voltage on pin GREF             |                      | <sup>[2]</sup> -0.5 | +7.0 | V    |
| V <sub>Sn</sub>   | voltage on port Sn              |                      | <sup>[2]</sup> -0.5 | +7.0 | V    |
| V <sub>Dn</sub>   | voltage on port Dn              |                      | <sup>[2]</sup> -0.5 | +7.0 | V    |
| I <sub>REFK</sub> | diode current on reference pins | V <sub>I</sub> < 0 V | -                   | -50  | mA   |
| I <sub>SK</sub>   | diode current port Sn           | V <sub>I</sub> < 0 V | -                   | -50  | mA   |
| I <sub>DK</sub>   | diode current port Dn           | V <sub>I</sub> < 0 V | -                   | -50  | mA   |
| I <sub>max</sub>  | clamp current per channel       | channel in ON state  | -                   | ±128 | mA   |
| T <sub>stg</sub>  | storage temperature             |                      | -65                 | +150 | °C   |

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperature which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## 10. Recommended operating conditions

**Table 8. Recommended operating conditions**

| Symbol            | Parameter                      | Conditions            | Min              | Max | Unit |
|-------------------|--------------------------------|-----------------------|------------------|-----|------|
| V <sub>I/O</sub>  | voltage on an input/output pin | Sn, Dn                | 0                | 5.5 | V    |
| V <sub>SREF</sub> | voltage on pin SREF            |                       | <sup>[1]</sup> 0 | 5.5 | V    |
| V <sub>DREF</sub> | voltage on pin DREF            |                       | 0                | 5.5 | V    |
| V <sub>GREF</sub> | voltage on pin GREF            |                       | 0                | 5.5 | V    |
| I <sub>PASS</sub> | pass transistor current        |                       | -                | 64  | mA   |
| T <sub>amb</sub>  | ambient temperature            | operating in free air | -40              | +85 | °C   |

[1] V<sub>SREF</sub> ≤ V<sub>DREF</sub> - 1.5 V for best results in level shifting applications.

## 11. Static characteristics

**Table 9. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol         | Parameter                          | Conditions                                                                                                                         | Min              | Typ <sup>[1]</sup> | Max  | Unit          |
|----------------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------------|------|---------------|
| $V_{OL}$       | LOW-level output voltage           | $V_{DD} = 3.0\text{ V}$ ; $V_{SREF} = 1.365\text{ V}$ ;<br>$V_{Sn}$ or $V_{Dn} = 0.175\text{ V}$ ;<br>$I_{clamp} = 15.2\text{ mA}$ | -                | 260                | 350  | mV            |
| $V_{IK}$       | input clamping voltage             | $I_I = -18\text{ mA}$ ; $V_{GREF} = 0\text{ V}$                                                                                    | -                | -                  | -1.2 | V             |
| $I_{LI(gate)}$ | gate input leakage current         | $V_I = 5\text{ V}$ ; $V_{GREF} = 0\text{ V}$                                                                                       | -                | -                  | 5    | $\mu\text{A}$ |
| $C_{ig}$       | input capacitance at gate          | pin GREF; $V_I = 3\text{ V}$ or $0\text{ V}$                                                                                       | -                | 19.4               | -    | pF            |
| $C_{io(off)}$  | off-state input/output capacitance | $V_O = 3\text{ V}$ or $0\text{ V}$ ; $V_{GREF} = 0\text{ V}$                                                                       | <sup>[2]</sup> - | 7.4                | -    | pF            |
| $C_{io(on)}$   | on-state input/output capacitance  | $V_O = 3\text{ V}$ or $0\text{ V}$ ; $V_{GREF} = 3\text{ V}$                                                                       | <sup>[2]</sup> - | 18.6               | -    | pF            |
| $R_{on}$       | ON-state resistance                | $V_I = 0\text{ V}$ ; $I_O = 64\text{ mA}$                                                                                          | <sup>[3]</sup>   |                    |      |               |
|                |                                    | $V_{GREF} = 4.5\text{ V}$                                                                                                          | -                | 3.5                | 5    | $\Omega$      |
|                |                                    | $V_{GREF} = 3\text{ V}$                                                                                                            | -                | 4.4                | 7    | $\Omega$      |
|                |                                    | $V_{GREF} = 2.3\text{ V}$                                                                                                          | -                | 5.5                | 9    | $\Omega$      |
|                |                                    | $V_{GREF} = 1.5\text{ V}$                                                                                                          | -                | 67                 | 105  | $\Omega$      |
|                |                                    | $V_I = 0\text{ V}$ ; $I_O = 30\text{ mA}$ ;<br>$V_{GREF} = 1.5\text{ V}$                                                           | <sup>[3]</sup> - | 9                  | 15   | $\Omega$      |
|                |                                    | $V_I = 2.4\text{ V}$ ; $I_O = 15\text{ mA}$ ;<br>$V_{GREF} = 4.5\text{ V}$                                                         | <sup>[3]</sup> - | 7                  | 10   | $\Omega$      |
|                |                                    | $V_I = 2.4\text{ V}$ ; $I_O = 15\text{ mA}$ ;<br>$V_{GREF} = 3\text{ V}$                                                           | <sup>[3]</sup> - | 58                 | 80   | $\Omega$      |
|                |                                    | $V_I = 1.7\text{ V}$ ; $I_O = 15\text{ mA}$ ;<br>$V_{GREF} = 2.3\text{ V}$                                                         | <sup>[3]</sup> - | 50                 | 70   | $\Omega$      |

[1] All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2]  $C_{io(on)}$  maximum of 30 pF and  $C_{io(off)}$  maximum of 15 pF is guaranteed by design.

[3] Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

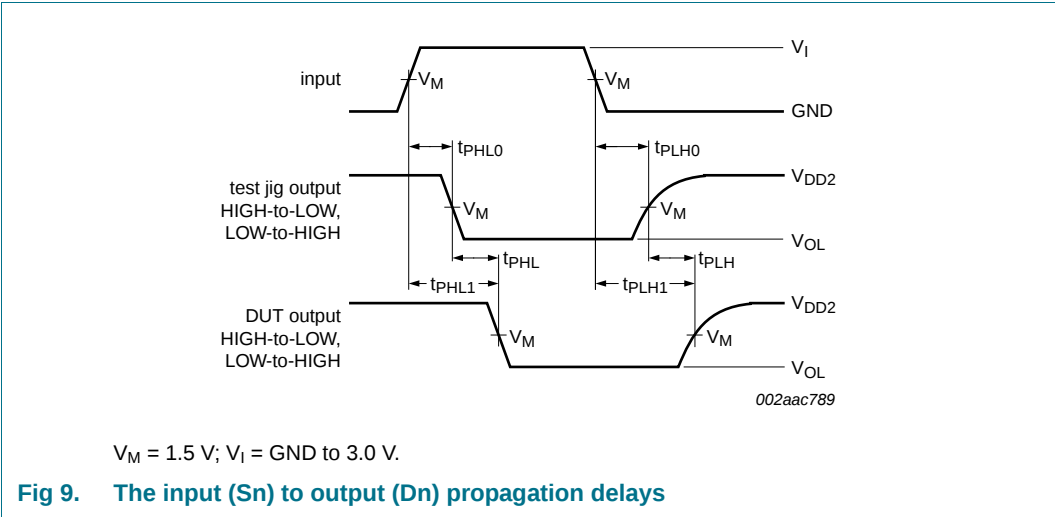
12. Dynamic characteristics

12.1 Dynamic characteristics for translator-type application

Table 10. Dynamic characteristics for translator-type application
T\_amb = -40 °C to +85 °C; V\_ref = 1.365 V to 1.635 V; V\_DD1 = 3.0 V to 3.6 V; V\_DD2 = 2.36 V to 2.64 V; GND = 0 V; t\_r = t\_f ≤ 3.0 ns. Refer to Figure 11.

Table with 7 columns: Symbol, Parameter, Conditions, Min, Typ, Max, Unit. It lists propagation delays t\_PLH and t\_PHL for LOW to HIGH and HIGH to LOW transitions under specific conditions.

[1] All typical values are measured at V\_DD1 = 3.3 V, V\_DD2 = 2.5 V; V\_ref = 1.5 V and T\_amb = 25 °C.
[2] Propagation delay guaranteed by characterization.

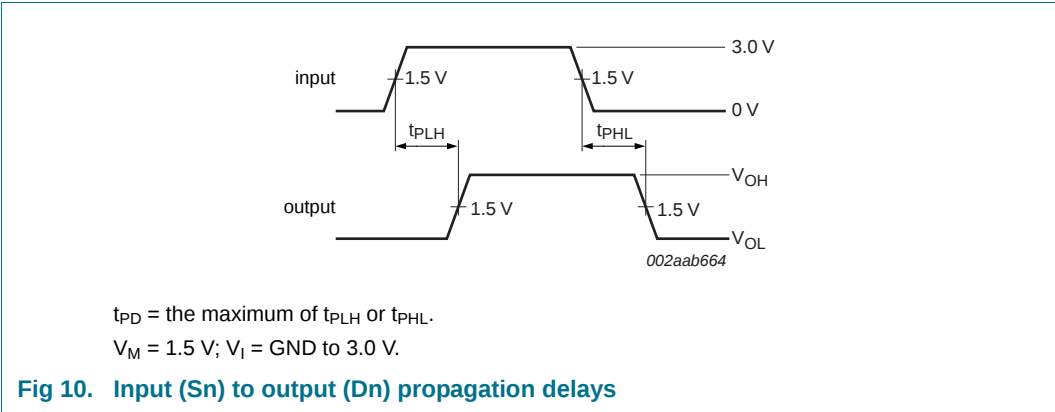


12.2 Dynamic characteristics for CBT-type application

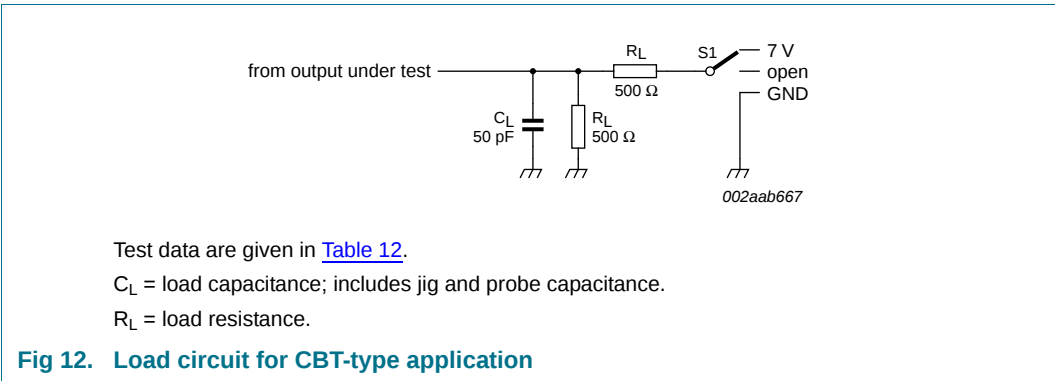
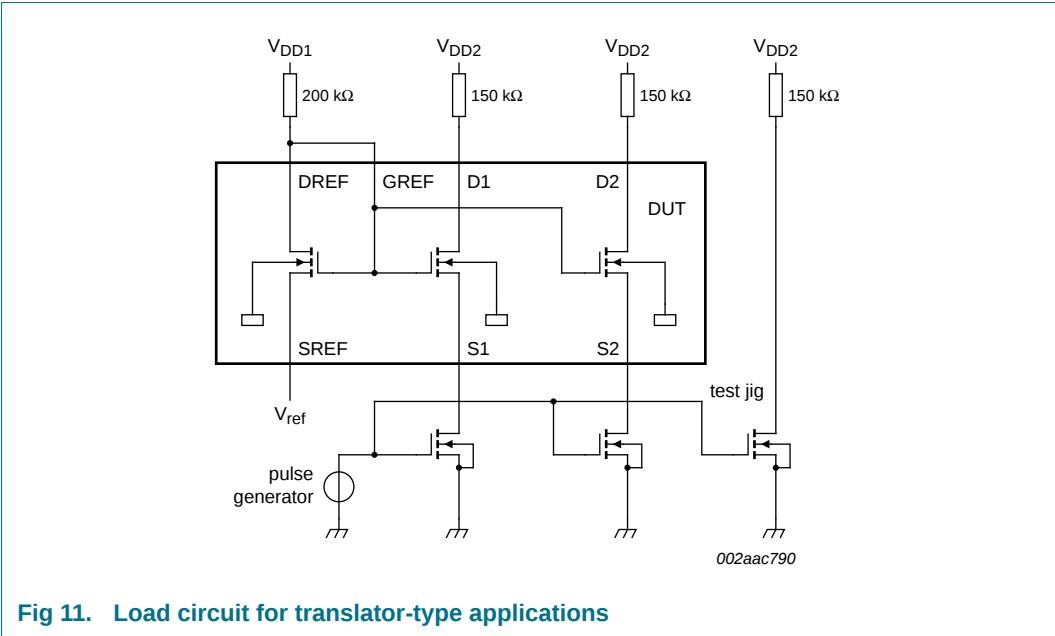
Table 11. Dynamic characteristics for CBT-type application  
 $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ;  $V_{GREF} = 5\text{ V} \pm 0.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ ;  $C_L = 50\text{ pF}$ .

| Symbol   | Parameter         | Conditions | Min | Typ | Max | Unit |
|----------|-------------------|------------|-----|-----|-----|------|
| $t_{PD}$ | propagation delay | [1]        | -   | -   | 250 | ps   |

[1] This parameter is warranted by the ON-state resistance at  $GREF = 4.5\text{ V}$ , but is not directly production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



13. Test information



| Test     | Load  |       | Switch |
|----------|-------|-------|--------|
|          | $C_L$ | $R_L$ |        |
| $t_{PD}$ | 50 pF | 500 Ω | open   |

14. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

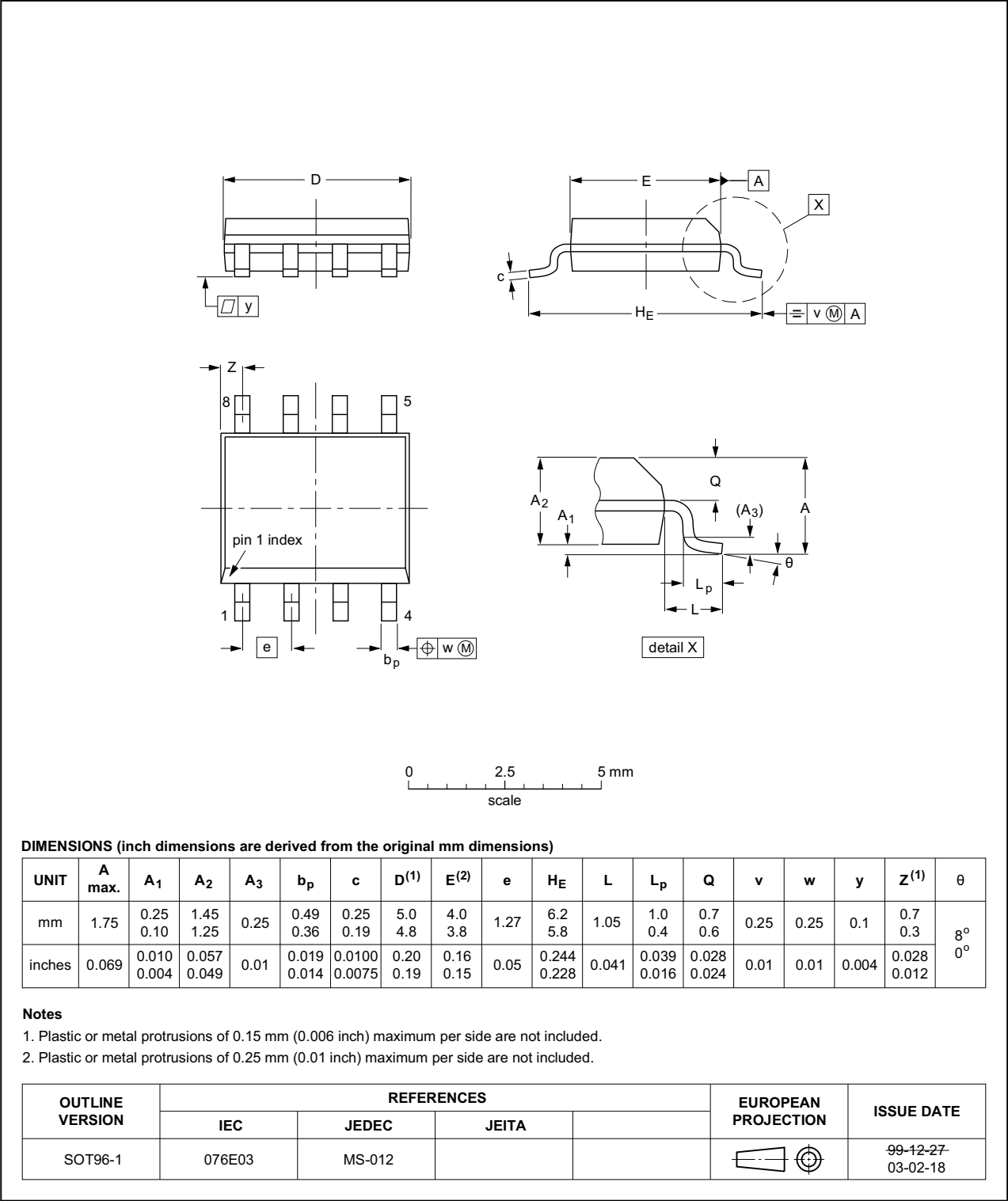


Fig 13. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

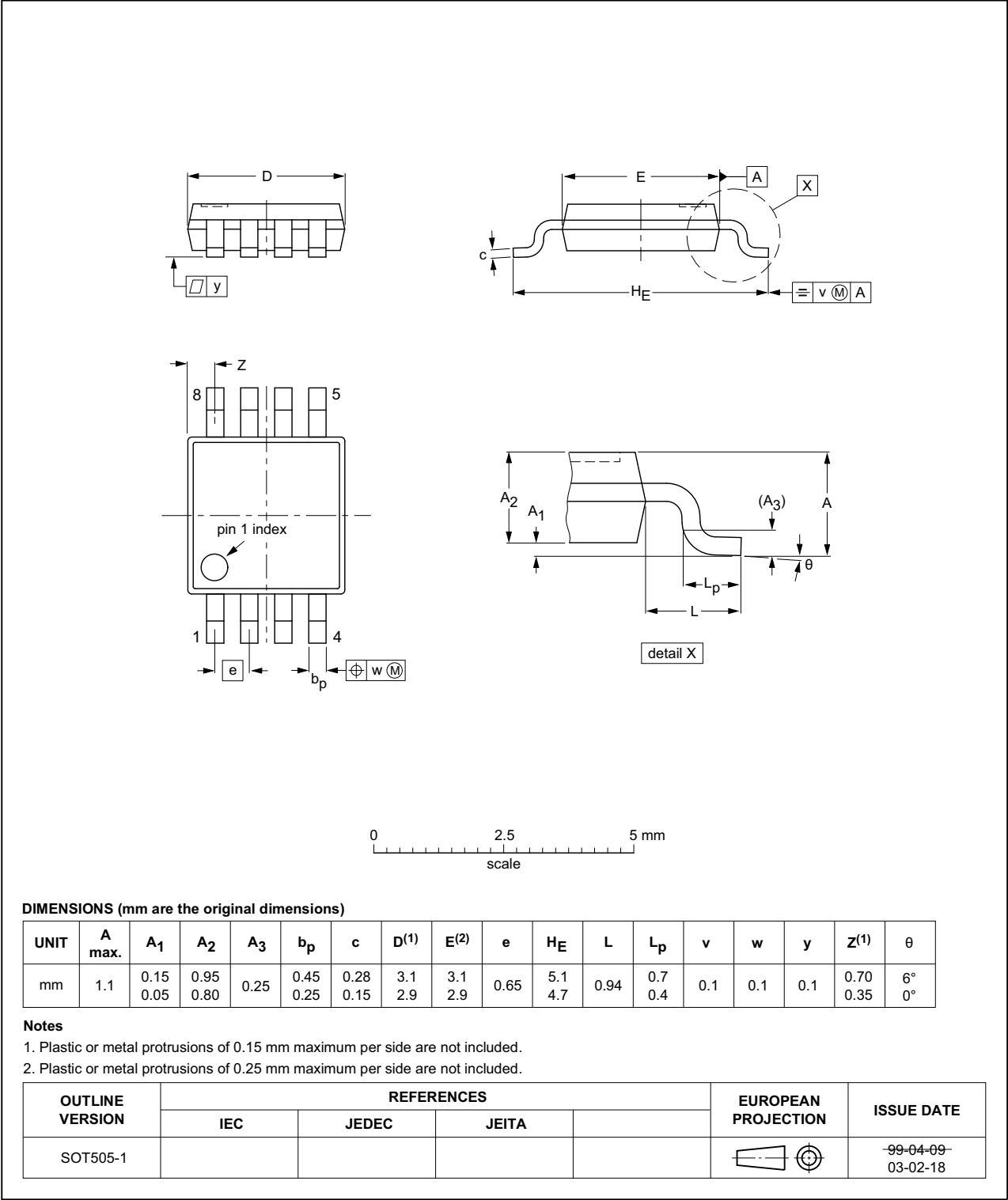


Fig 14. Package outline SOT505-1 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

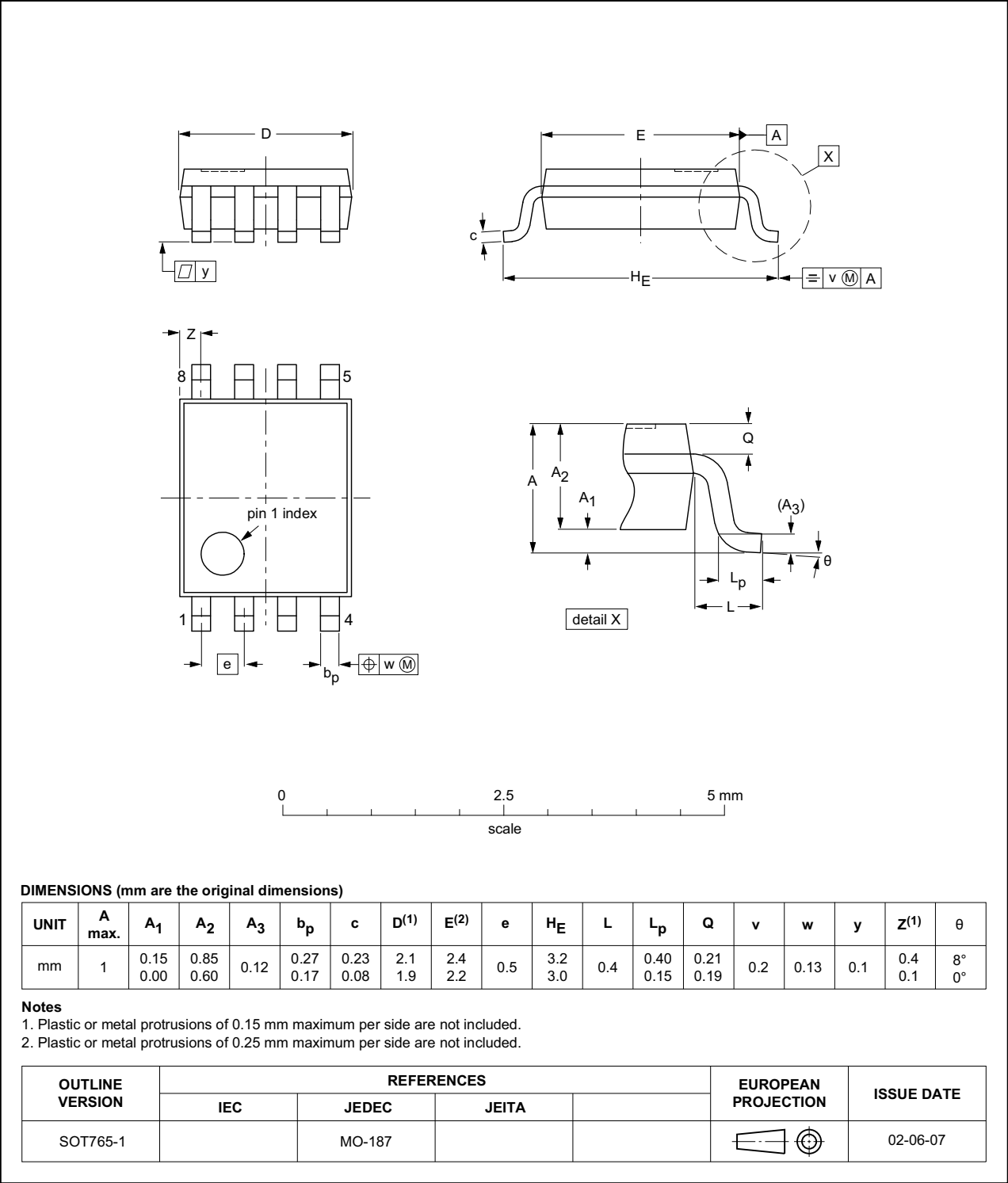


Fig 15. Package outline SOT765-1 (VSSOP8)

XQFN8: plastic, extremely thin quad flat package; no leads;  
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

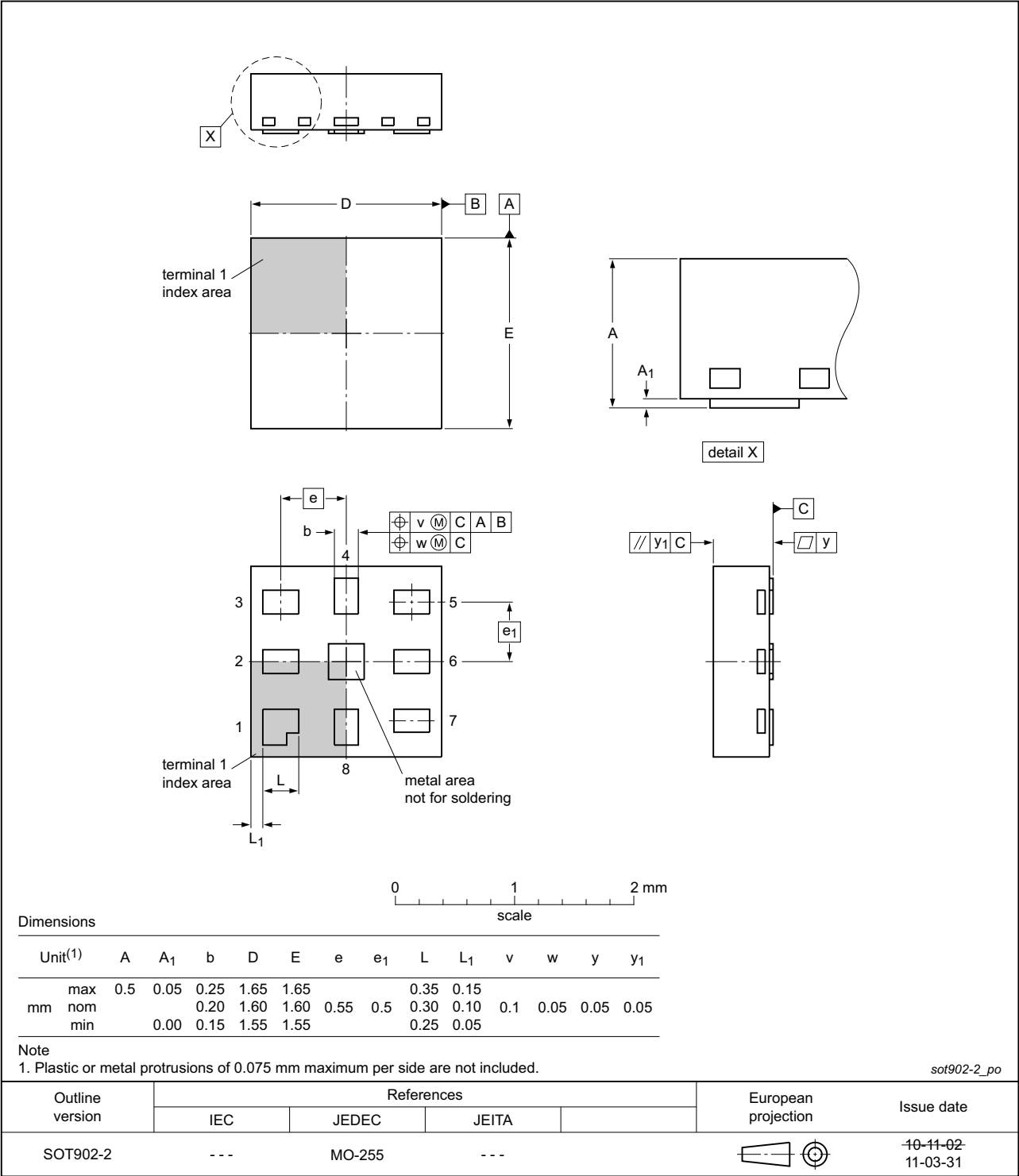


Fig 16. Package outline SOT902-2 (XQFN8)

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 17](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 13](#) and [14](#)

**Table 13. SnPb eutectic process (from J-STD-020D)**

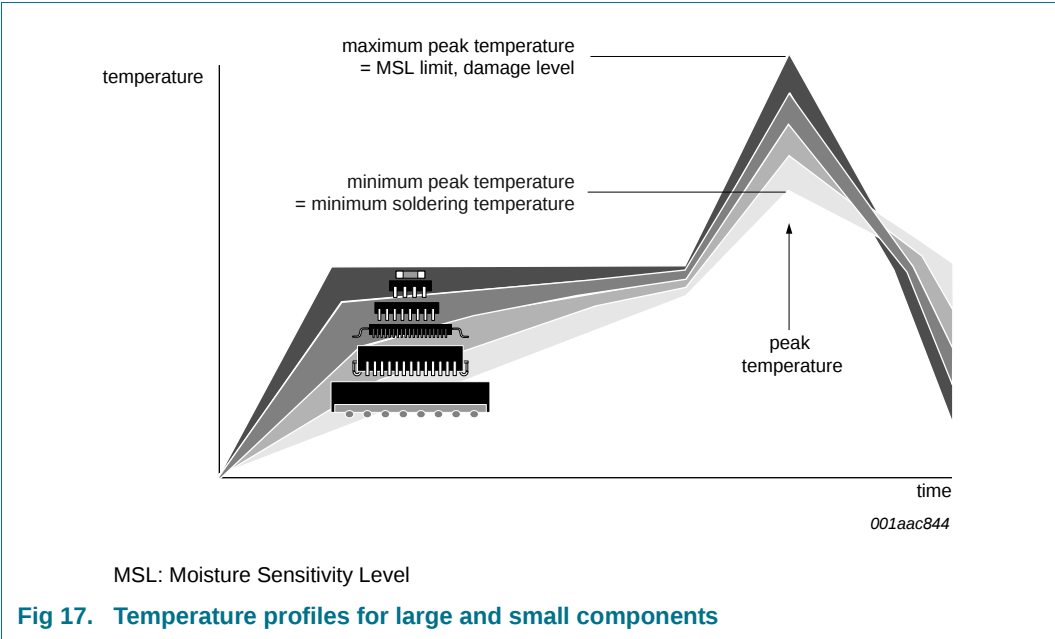
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 14. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

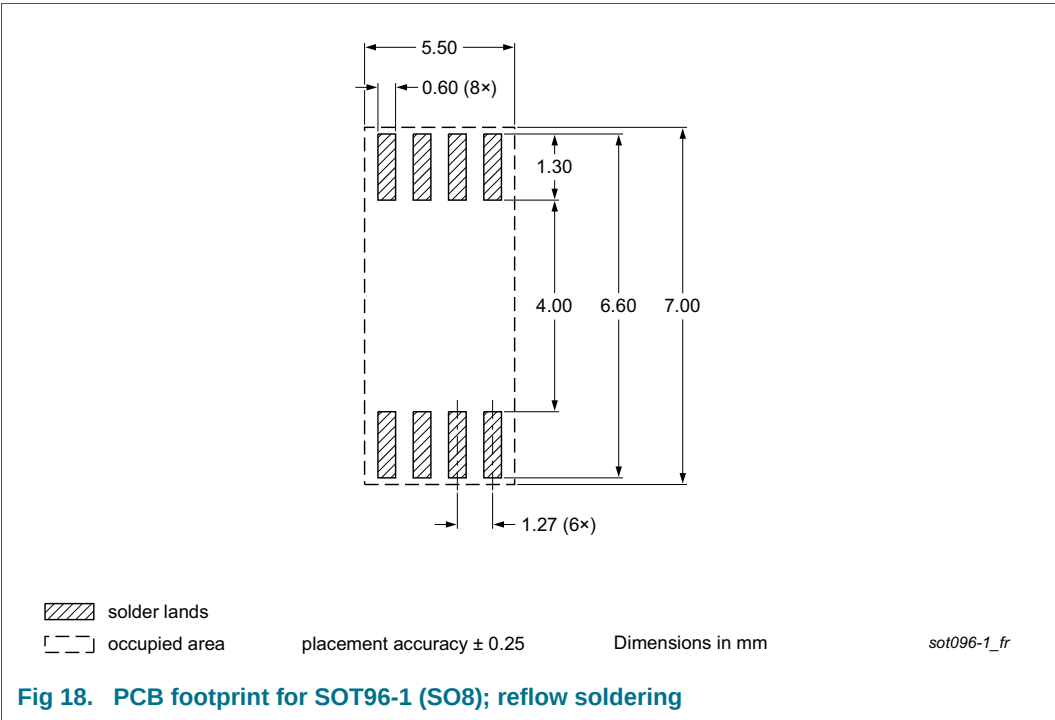
Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

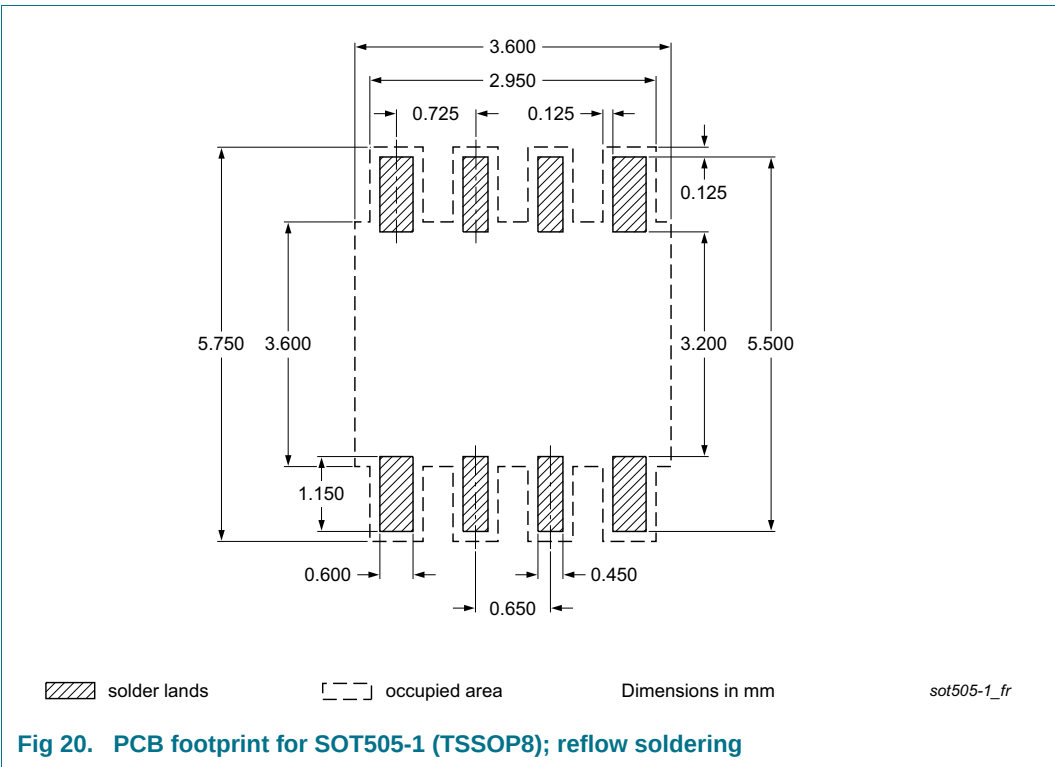
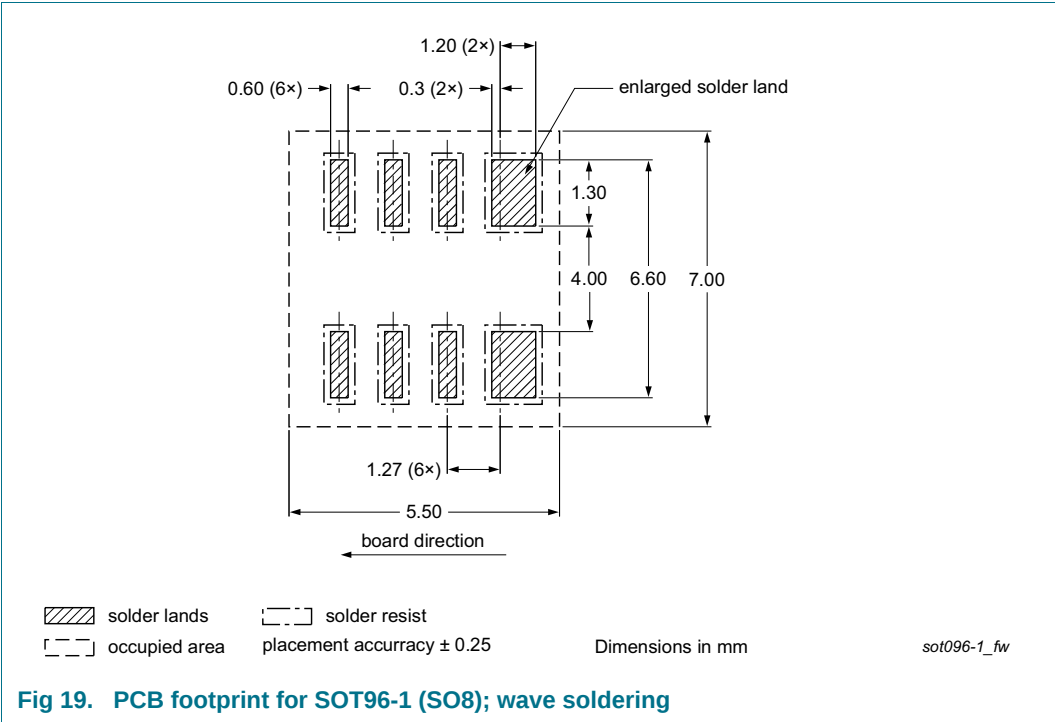
Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 17](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 16. Soldering: PCB footprints





Footprint information for reflow soldering of VSSOP8 package

SOT765-1

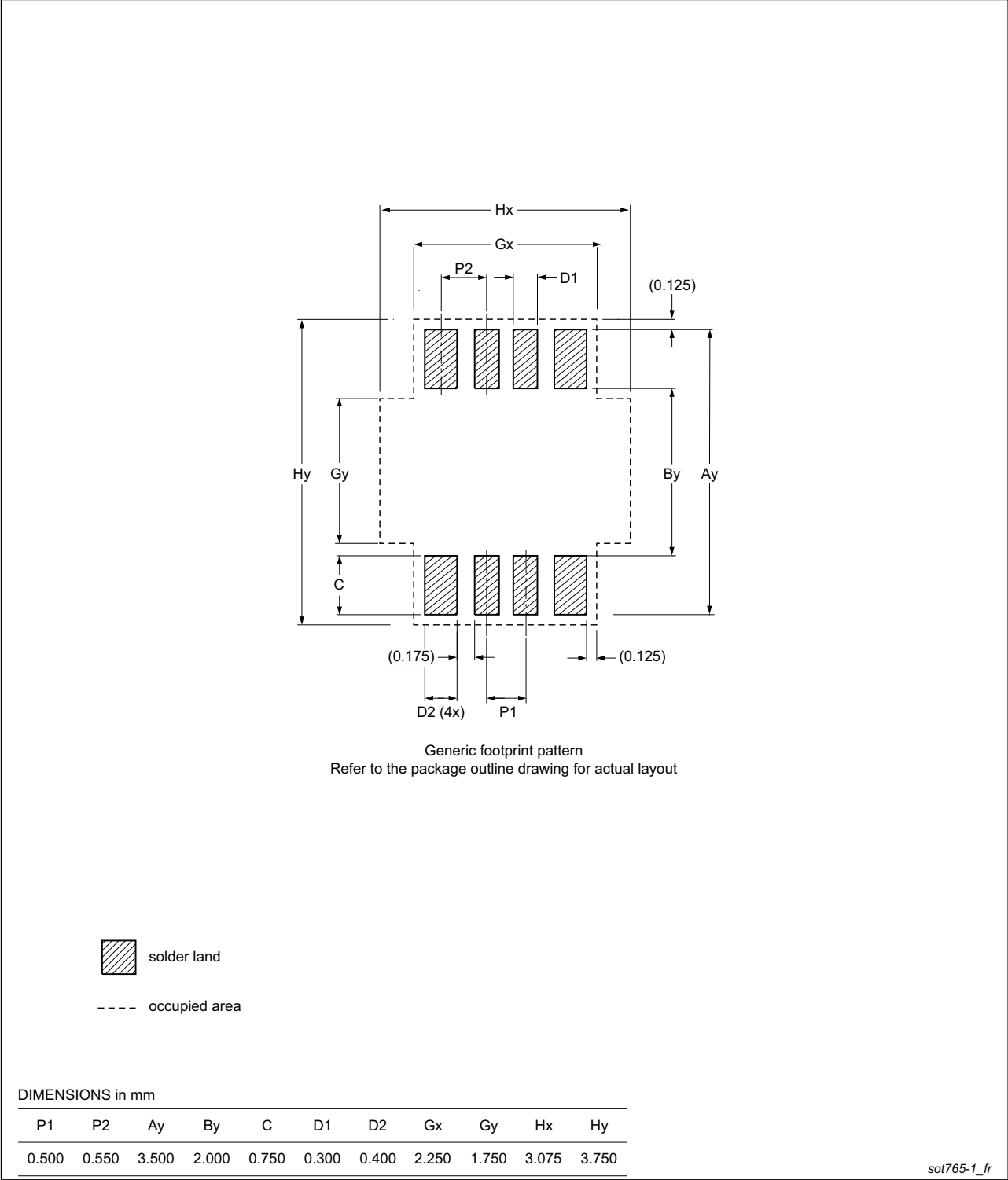


Fig 21. PCB footprint for SOT765-1 (VSSOP8); reflow soldering

Footprint information for reflow soldering of XQFN8 package

SOT902-2

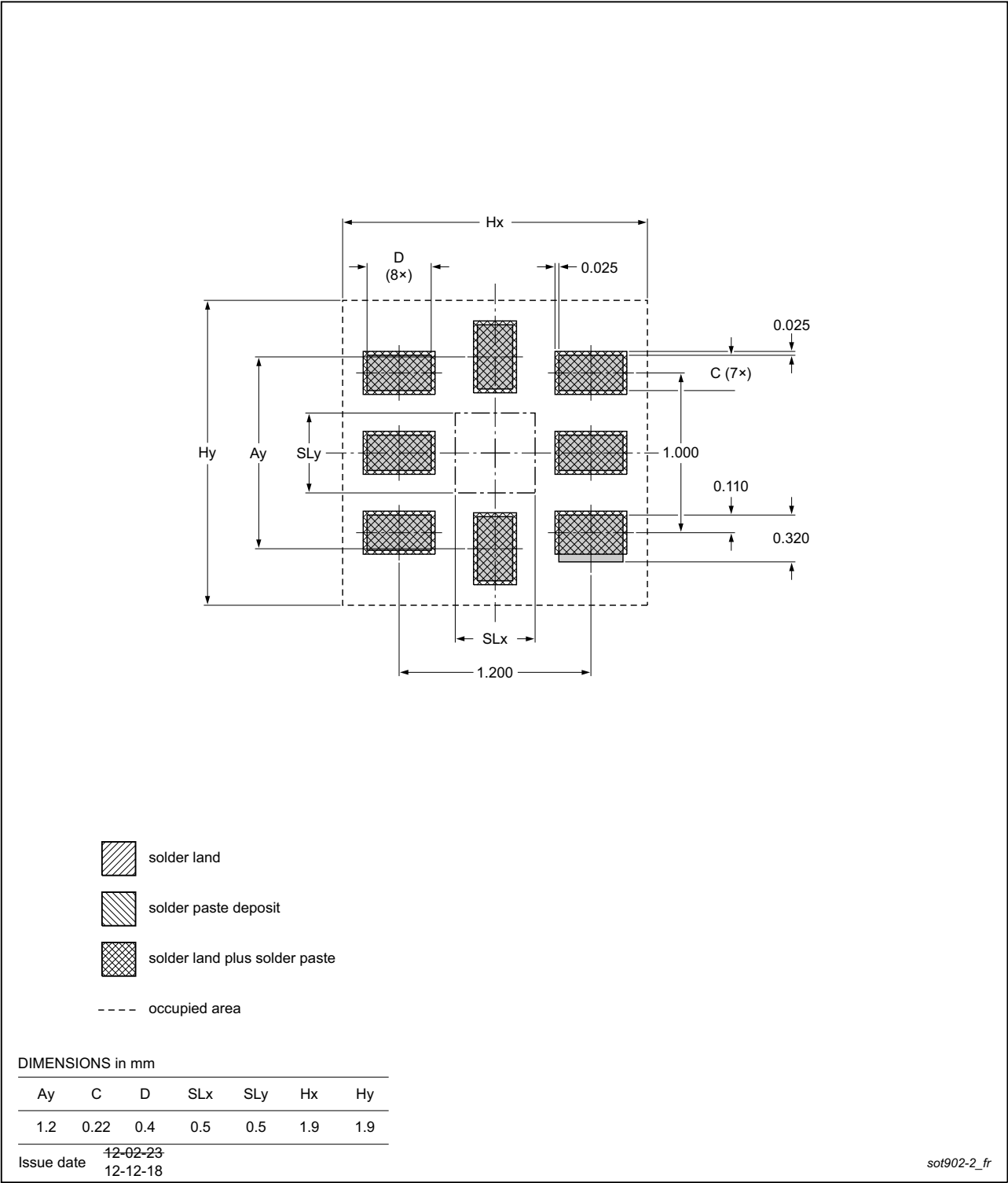


Fig 22. PCB footprint for SOT902-2 (XQFN8); reflow soldering

## 17. Abbreviations

Table 15. Abbreviations

| Acronym              | Description                                |
|----------------------|--------------------------------------------|
| CBT                  | Cross Bar Technology                       |
| CDM                  | Charged-Device Model                       |
| CMOS                 | Complementary Metal-Oxide Semiconductor    |
| CPU                  | Central Processing Unit                    |
| ESD                  | ElectroStatic Discharge                    |
| GTL                  | Gunning Transceiver Logic                  |
| HBM                  | Human Body Model                           |
| I/O                  | Input/Output                               |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus               |
| LVTTL                | Low Voltage Transistor-Transistor Logic    |
| NMOS                 | Negative-channel Metal-Oxide Semiconductor |
| RC                   | Resistor Capacitor network                 |
| TTL                  | Transistor-Transistor Logic                |
| TVC                  | Transceiver Voltage Clamps                 |

## 18. Revision history

Table 16. Revision history

| Document ID                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Release date | Data sheet status     | Change notice                           | Supersedes  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------------------|-----------------------------------------|-------------|
| GTL2002 v.8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 20130819     | Product data sheet    | -                                       | GTL2002 v.7 |
| Modifications: <ul style="list-style-type: none"> <li>• <a href="#">Section 2 “Features and benefits”</a>:               <ul style="list-style-type: none"> <li>– 10th bullet item: deleted phrase “150 V MM per JESD22-A115”</li> <li>– 11th bullet item changed from “XQFN8U” to “XQFN8”</li> </ul> </li> <li>• <a href="#">Table 1 “Ordering information”</a>:               <ul style="list-style-type: none"> <li>– removed type number “GTL2002DP/Q900”</li> <li>– added column “Topside marking”</li> <li>– GTL2002GM package name, description, and version changed per PCN #201108001F01: from “XQFN8U, plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm (SOT902-1)” to “XQFN8, plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm (SOT902-2)”</li> </ul> </li> <li>• <a href="#">Table 2 “Ordering options”</a>:               <ul style="list-style-type: none"> <li>– Added columns “Orderable part number”, “Package”, “Packing method”, and “Minimum order quantity”</li> <li>– Column “Topside mark” is moved to <a href="#">Table 1</a></li> </ul> </li> <li>• <a href="#">Figure 3 “Pin configuration for TSSOP8 (MSOP8)”</a> updated: removed type number “GTL2002DP/Q900”</li> <li>• <a href="#">Figure 5</a> changed from “XQFN8U” (SOT902-1) to “XQFN8” (SOT902-2), (per PCN #201108001F01)</li> <li>• <a href="#">Table 3 “Pin description”</a> modified: column heading changed from “XQFN8U” to “XQFN8”</li> <li>• <a href="#">Figure 16</a> changed from “SOT902-1 (XQFN8U)” to “SOT902-2 (XQFN8)”, per PCN #201108001F01</li> <li>• <a href="#">Section 15 “Soldering of SMD packages”</a> updated</li> <li>• Added <a href="#">Section 16 “Soldering: PCB footprints”</a></li> </ul> |              |                       |                                         |             |
| GTL2002 v.7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 20090702     | Product data sheet    | -                                       | GTL2002 v.6 |
| GTL2002 v.6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 20071221     | Product data sheet    | -                                       | GTL2002 v.5 |
| GTL2002 v.5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 20070813     | Product data sheet    | -                                       | GTL2002 v.4 |
| GTL2002 v.4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 20060829     | Product data sheet    | -                                       | GTL2002 v.3 |
| GTL2002 v.3<br>(9397 750 13058)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 20040929     | Product data sheet    | -                                       | GTL2002 v.2 |
| GTL2002 v.2<br>(9397 750 11349)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 20030401     | Product data          | ECN 853-2214 29603<br>dated 2003 Feb 28 | GTL2002 v.1 |
| GTL2002 v.1<br>(9397 750 07417)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 20000216     | Product specification | ECN 853-2214 24367<br>dated 2000 Aug 16 | -           |

## 19. Legal information

### 19.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

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