

SN54ALVTH16601, SN74ALVTH16601 2.5-V/3.3-V 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES143A – SEPTEMBER 1998 – REVISED JULY 1999

- **UBT™ (Universal Bus Transceiver)**
Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design** for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce)**
 $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **High-Drive** ($-24/24\text{ mA}$ at 2.5-V and $-32/64\text{ mA}$ at 3.3-V V_{CC})
- **I_{off} and Power-Up 3-State Support** Hot Insertion
- **Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors** to Prevent the Bus From Floating
- **Auto3-State Eliminates Bus Current Loading** When Output Exceeds $V_{CC} + 0.5\text{ V}$
- **Flow-Through Architecture Facilitates** Printed Circuit Board Layout
- **Distributed V_{CC} and GND Pin Configuration** Minimizes High-Speed Switching Noise
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

NOTE: For tape and reel order entry:
The DGGR package is abbreviated to GR and
the DGVR package is abbreviated to VR.

SN54ALVTH16601 . . . WD PACKAGE
SN74ALVTH16601 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

OEAB	1	56	CLKENAB
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	CLKENBA

description

The 'ALVTH16601 devices are 18-bit universal bus transceivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.



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2.5-V/3.3-V 18-BIT UNIVERSAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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description (continued)

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH16601 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH16601 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE[†]

INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	$B_0^{\ddagger}$
H	L	L	X	X	$B_0^{\ddagger}$
L	L	L	$\uparrow$	L	L
L	L	L	$\uparrow$	H	H
L	L	L	L or H	X	$B_0^{\ddagger}$

[†] A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

[‡] Output level before the indicated steady-state input conditions were established

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The diagram illustrates the logic for a 17-channel system. On the left, nine input signals are listed: OEAB (1), CLKENAB (56), CLKAB (55), LEAB (2), LEBA (28), CLKBA (30), CLKENBA (29), OEBA (27), and A1 (3). Each of these signals passes through an inverter. The outputs of these inverters are connected to two logic blocks. The first logic block (bottom) has inputs CE, 1D, C1, and CLK. The second logic block (top) has inputs CE, 1D, C1, and CLK. The outputs of these blocks are connected to two more inverters, which then lead to outputs B1 and 54. A bracket at the bottom indicates that the signals are connected to 17 other channels.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output current in the low state, I_O : SN54ALVTH16601	96 mA
SN74ALVTH16601	128 mA
Output current in the high state, I_O : SN54ALVTH16601	–48 mA
SN74ALVTH16601	–64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

		SN54ALVTH16601			SN74ALVTH16601			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage	1.7			1.7			V
V_{IL}	Low-level input voltage			0.7			0.7	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			–6			–8	mA
I_{OL}	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

			SN54ALVTH16601			SN74ALVTH16601			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		3		3.6	3		3.6	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current				–24			–32	mA
I_{OL}	Low-level output current				24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$				48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature		–55		125	–40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16601			SN74ALVTH16601			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 2.3 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}		V _{CC} = 2.3 V to 2.7 V, I _{OH} = −100 μA		V _{CC} −0.2			V _{CC} −0.2			V
		V _{CC} = 2.3 V		I _{OH} = −6 mA						
				I _{OH} = −8 mA			1.8			
V _{OL}		V _{CC} = 2.3 V to 2.7 V, I _{OL} = 100 μA		0.2			0.2			V
		V _{CC} = 2.3 V		I _{OL} = 6 mA			0.4			
				I _{OL} = 8 mA			0.4			
				I _{OL} = 18 mA			0.5			
				I _{OL} = 24 mA			0.5			
V _{RST} ‡		V _{CC} = 2.7 V, I _O = 1 mA, V _I = V _{CC} or GND		0.55			0.55			V
I _I	Control inputs	V _{CC} = 2.7 V, V _I = V _{CC} or GND		±1			±1			μA
		V _{CC} = 0 or 2.7 V, V _I = 5.5 V		10			10			
	A or B ports	V _{CC} = 2.7 V, V _I = 5.5 V		10			10			
		V _{CC} = 2.7 V, V _I = V _{CC}		1			1			
		V _{CC} = 2.7 V, V _I = 0		−5			−5			
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100			μA
I _{BHL} §		V _{CC} = 2.3 V, V _I = 0.7 V		115			115			μA
I _{BHH} ¶		V _{CC} = 2.3 V, V _I = 1.7 V		−10			−10			μA
I _{BHLO} #		V _{CC} = 2.7 V, V _I = 0 to V _{CC}		300			300			μA
I _{BHHO}		V _{CC} = 2.7 V, V _I = 0 to V _{CC}		−300			−300			μA
I _{EX} ☆		V _{CC} = 2.3 V, V _O = 5.5 V		125			125			μA
I _{OZ(PU/PD)} □		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , OE = don't care		±100			±100			μA
I _{CC}		V _{CC} = 2.7 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.04	0.1	0.04	0.1	mA
				Outputs low		2.5	4.5	2.5	4.5	
				Outputs disabled		0.04	0.1	0.04	0.1	
C _i		V _{CC} = 2.5 V, V _I = 2.5 V or 0		3			3			pF
C _{io}		V _{CC} = 2.5 V, V _O = 2.5 V or 0		7			7			pF

[†] All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Data must not be loaded into the flip-flops/latches after applying power.

[§] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[¶] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[#] An external driver must source at least I_{BHLO} to switch this node from low to high.

^{||} An external driver must sink at least I_{BHHO} to switch this node from high to low.

[☆] Current into an output in the high state when $V_O > V_{CC}$

[□] High-impedance state during power up or power down

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH16601		SN74ALVTH16601		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 3 V, I _I = −18 mA		−1.2		−1.2		V
V _{OH}		V _{CC} = 3 V to 3.6 V, I _{OH} = −100 μA		V _{CC} −0.2		V _{CC} −0.2		V
		V _{CC} = 3 V, I _{OH} = −24 mA		2				
		I _{OH} = −32 mA				2		
V _{OL}		V _{CC} = 3 V to 3.6 V, I _{OL} = 100 μA		0.2		0.2		V
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4		
				I _{OL} = 24 mA		0.5		
				I _{OL} = 32 mA		0.5		
				I _{OL} = 48 mA		0.55		
				I _{OL} = 64 mA		0.55		
V _{RST} ‡		V _{CC} = 3.6 V, I _O = 1 mA, V _I = V _{CC} or GND	0.55		0.55		V	
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1		μA
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10		10		
	A or B ports	V _I = 5.5 V		10		10		
		V _I = V _{CC}		1		1		
		V _I = 0		−5		−5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA
I _{BHL} §		V _{CC} = 3 V, V _I = 0.8 V		75		75		μA
I _{BHH} ¶		V _{CC} = 3 V, V _I = 2 V		−75		−75		μA
I _{BHLO} #		V _{CC} = 3.6 V, V _I = 0 to V _{CC}		500		500		μA
I _{BHHO}		V _{CC} = 3.6 V, V _I = 0 to V _{CC}		−500		−500		μA
I _{EX} ☆		V _{CC} = 3 V, V _O = 5.5 V		125		125		μA
I _{OZ} (PU/PD)□		V _{CC} ≤ 1.2 V, V _O = 0.5 V to V _{CC} , V _I = GND or V _{CC} , OE = don't care		±100		±100		μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		0.06		0.1		mA
		Outputs high		0.06		0.1		
		Outputs low		3.5		5		
		Outputs disabled		0.06		0.1		
ΔI _{CC} ◇		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.4		0.4		mA
C _i		V _{CC} = 3.3 V, V _I = 3.3 V or 0		3		3		pF
C _{i0}		V _{CC} = 3.3 V, V _O = 3.3 V or 0		7		7		pF

[†] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Data must not be loaded into the flip-flops/latches after applying power.

[§] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

^{\P} The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[#] An external driver must source at least I_{BHLO} to switch this node from low to high.

^{\parallel} An external driver must sink at least I_{BHHO} to switch this node from high to low.

^{\star} Current into an output in the high state when $V_O > V_{CC}$

^{\square} High-impedance state during power up or power down

^{\diamond} This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

				SN54ALVTH16601		SN74ALVTH16601		UNIT
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			150		150		MHz
t _w	Pulse duration		LE high	1.8		1.8		ns
			CLK high or low	2.3		2.3		
t _{su}	Setup time		A or B before CLK↑	Data high	4		ns	
				Data low	5.2			
			A or B before LE↓	CLK high	0.7			
				CLK low	0.9			
			$\overline{\text{CLKEN}}$ before CLK↑	Data high	1.7			
				Data low	2.3			
t _h	Hold time		A or B after CLK↑	Data high	0.5		ns	
				Data low	0.5			
			A or B after LE↓	CLK high	2.3			
				CLK low	2.4			
			$\overline{\text{CLKEN}}$ after CLK↑	Data high	0.5			
				Data low	0.5			

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)

				SN54ALVTH16601		SN74ALVTH16601		UNIT
				MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			150		150		MHz
t _w	Pulse duration		LE high	1.8		1.8		ns
			CLK high or low	2.3		2.3		
t _{su}	Setup time		A or B before CLK↑	Data high	2.4		ns	
				Data low	3.8			
			A or B before LE↓	CLK high	1			
				CLK low	0.6			
			$\overline{\text{CLKEN}}$ before CLK↑	Data high	1.4			
				Data low	1.9			
t _h	Hold time		A or B after CLK↑	Data high	0.5		ns	
				Data low	0.5			
			A or B after LE↓	CLK high	2			
				CLK low	2.3			
			$\overline{\text{CLKEN}}$ after CLK↑	Data high	0.6			
				Data low	0.5			

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switching characteristics over recommended operating free-air temperature range, $C_L = 30$ pF, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16601		SN74ALVTH16601		UNIT
			MIN	MAX	MIN	MAX	
$f_{\max}$			150		150		MHz
t_{PLH}	B or A	A or B	1.1	4.1	1.1	4.1	ns
t_{PHL}			1.6	4.8	1.6	4.8	
t_{PLH}	LEBA or LEAB	A or B	2.1	5	2.1	5	ns
t_{PHL}			2.4	5.4	2.4	5.4	
t_{PLH}	CLKBA or CLKAB	A or B	2	5	2	5	ns
t_{PHL}			2.5	5.9	2.5	5.9	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.2	4.8	1.2	4.8	ns
t_{PZL}			1	4.6	1	4.6	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	1.2	5.2	1.2	5.2	ns
t_{PLZ}			1	3.9	1	3.9	

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16601		SN74ALVTH16601		UNIT
			MIN	MAX	MIN	MAX	
$f_{\max}$			150		150		MHz
t_{PLH}	B or A	A or B	1.4	3.9	1.4	3.9	ns
t_{PHL}			1.1	3.9	1.1	3.9	
t_{PLH}	LEBA or LEAB	A or B	2	4.6	2	4.6	ns
t_{PHL}			2.1	4.6	2.1	4.6	
t_{PLH}	CLKBA or CLKAB	A or B	1.9	4.5	1.9	4.5	ns
t_{PHL}			2.2	4.6	2.2	4.6	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1	4.2	1	4.2	ns
t_{PZL}			1	4.4	1	4.4	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	1.8	5.3	1.8	5.3	ns
t_{PLZ}			1.7	4.6	1.7	4.6	

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SN54ALVTH16601, SN74ALVTH16601

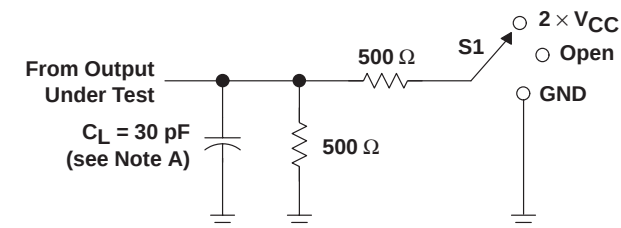
2.5-V/3.3-V 18-BIT UNIVERSAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES143A – SEPTEMBER 1998 – REVISED JULY 1999

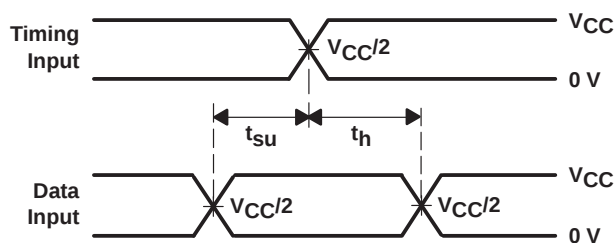
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

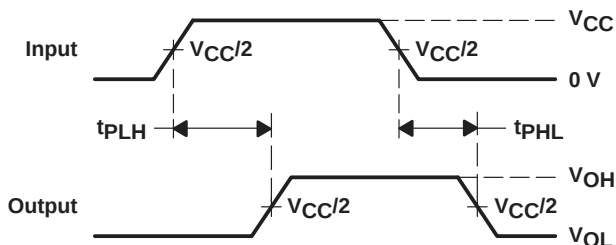


LOAD CIRCUIT

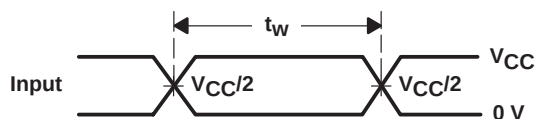
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



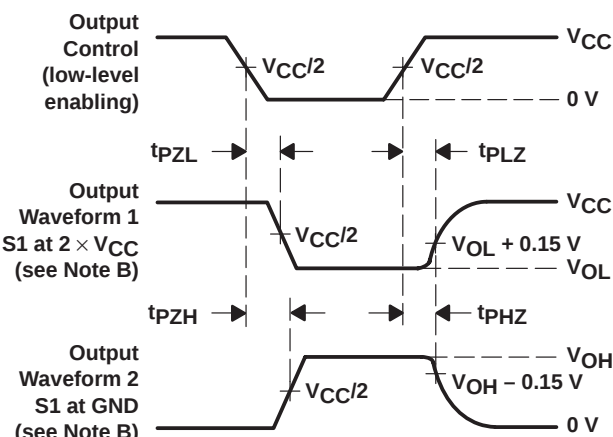
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

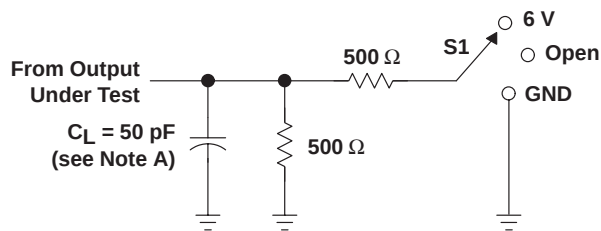
Figure 1. Load Circuit and Voltage Waveforms

SN54ALVTH16601, SN74ALVTH16601
2.5-V/3.3-V 18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES143A – SEPTEMBER 1998 – REVISED JULY 1999

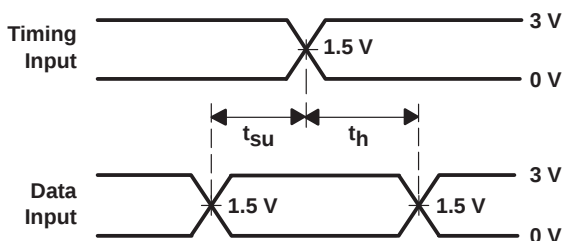
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

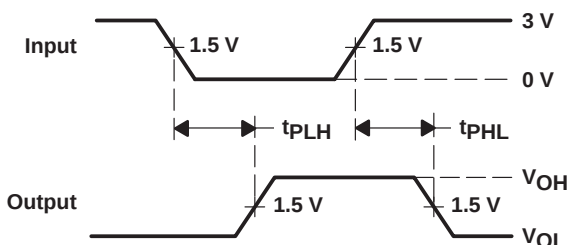


LOAD CIRCUIT

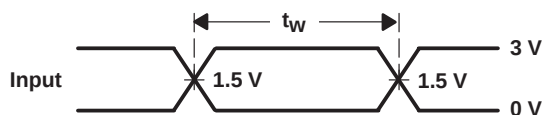
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



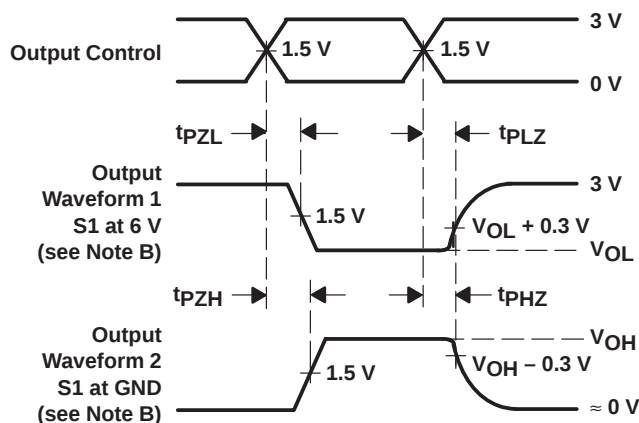
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVTH16601DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16601DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16601GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16601GRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16601VRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16601VRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16601DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16601DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16601GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16601VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVTH16601DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74ALVTH16601GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVTH16601VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



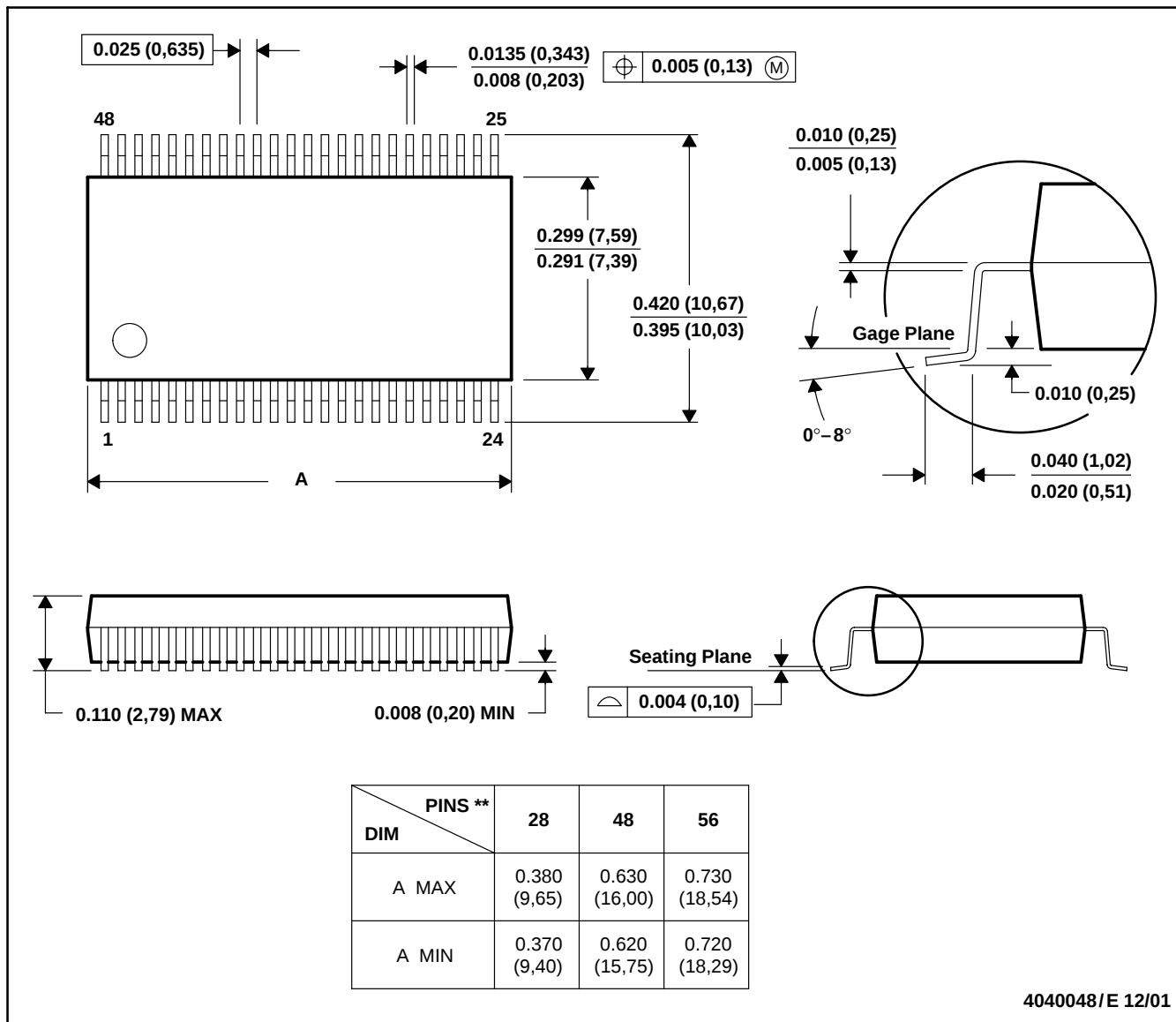
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVTH16601DLR	SSOP	DL	56	1000	346.0	346.0	49.0
SN74ALVTH16601GR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVTH16601VR	TVSOP	DGV	56	2000	346.0	346.0	41.0

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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