

**Document Title**

8Mb SyncBurst Flow through SRAM

**Revision History**

| <u>Revision No</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|--------------------|----------------|-------------------|---------------|
| 0A                 | Initial Draft  | September 3,2002  |               |

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## 256K x 32, 256K x 36, 512K x 18 8Mb SYNCBURST Flow throughSRAMs

### FEATURES

- Flowthrough Mode operation.
- User-selectable Output Drive Strength with XQ Mode.
- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Single +3.3V, +10%, -5% core power supply
- Power-down snooze mode
- 2.5V or 3.3V I/O Supply
- Snooze MODE for reduced-power standby
- T version (three chip selects)
- D version (two chip selects)

### DESCRIPTION

ICSI's 8Mb SyncBurst Flowthrough SRAMs integrate a 512k x 18, 256k x 32, or 256k x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter.

### Applications

The ICSI SyncBurst Flowthrough SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process to provide Level 2 Cache applications supporting Pentium and PowerPC microprocessors originally, the device now finds application ranging from DSP main store to networking chip set support.

### Controls

All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input. Bursts can be initiated with either  $\overline{\text{ADSP}}$  (Address Status Processor) or  $\overline{\text{ADSC}}$  (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the  $\overline{\text{ADV}}$  (burst address advance) input pin. The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

### Byte Write and Global Write

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs. Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ( $\overline{\text{BWE}}$ ) input combined with one or more individual byte write signals ( $\overline{\text{BWx}}$ ). In addition, Global Write ( $\overline{\text{GW}}$ ) is available for writing all bytes at one time, regardless of the byte write controls.

### IOL/IOH Drive strength Options

The XQ pin allows selection between high drive strength (XQ low) for multi-drop bus applications and normal drive strength (XQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

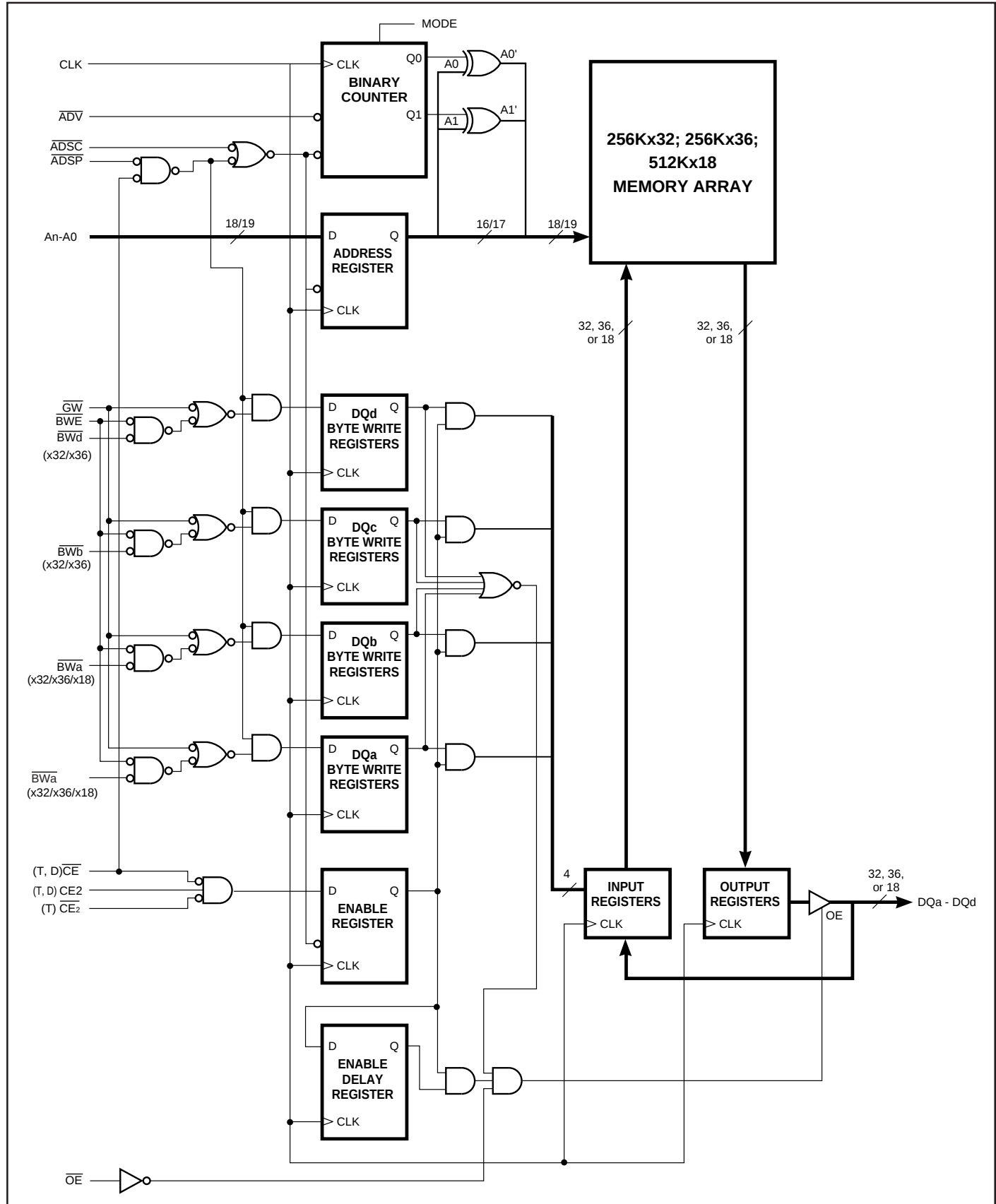
### Snooze Mode

Low power (Snooze mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Snooze mode.

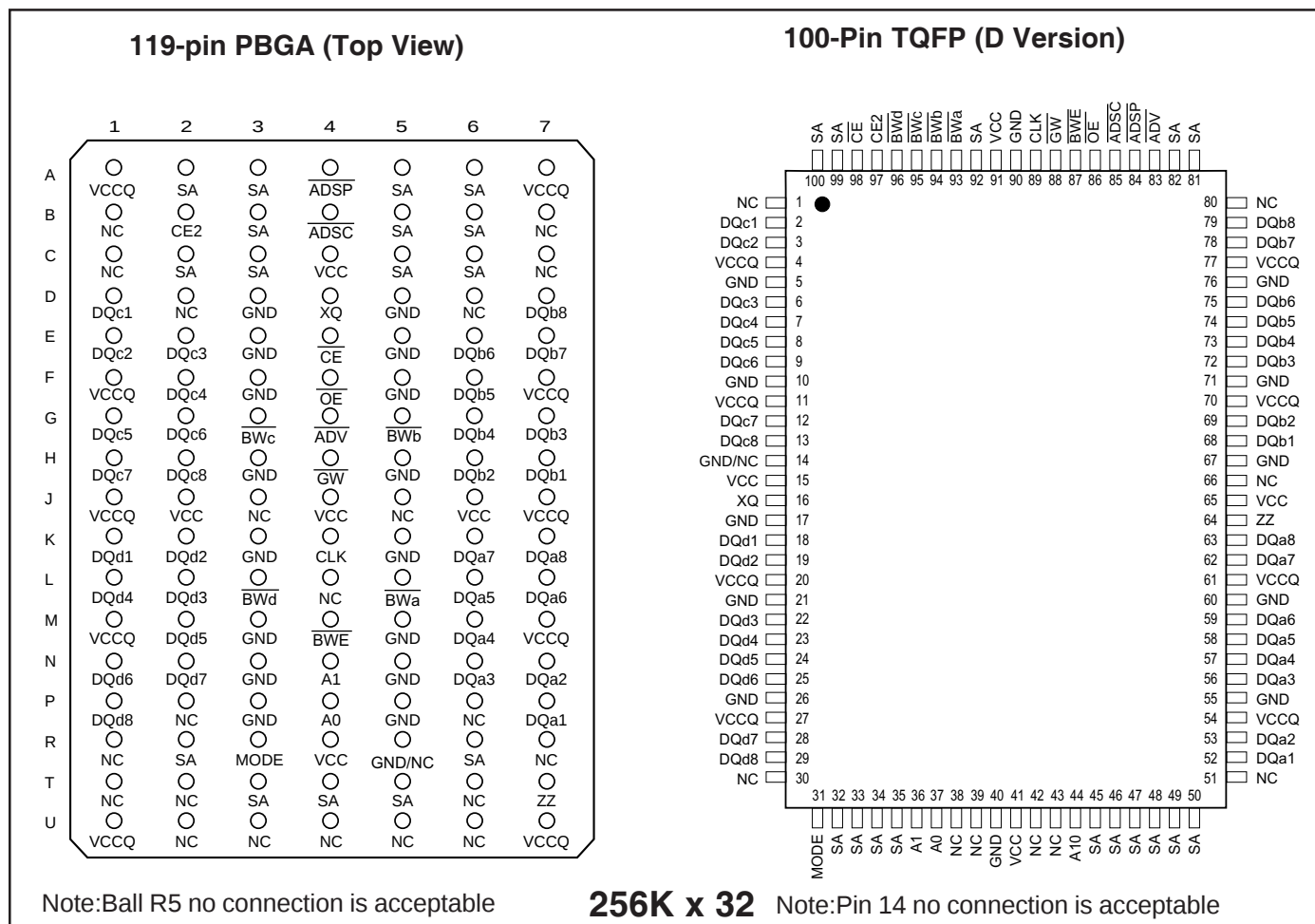
### FAST ACCESS TIME

|         | Symbol | -6.5 | -7.5 | -8.5 | -9.5 | Units |
|---------|--------|------|------|------|------|-------|
| Flow    | tkq    | 6.5  | 7.5  | 8.5  | 9.5  | ns    |
| Through | tkc    | 7.5  | 8.5  | 10   | 11   | ns    |
| 2-1-1-1 | lcc1   | 270  | 260  | 240  | 230  | mA    |

## BLOCK DIAGRAM



## PIN CONFIGURATION

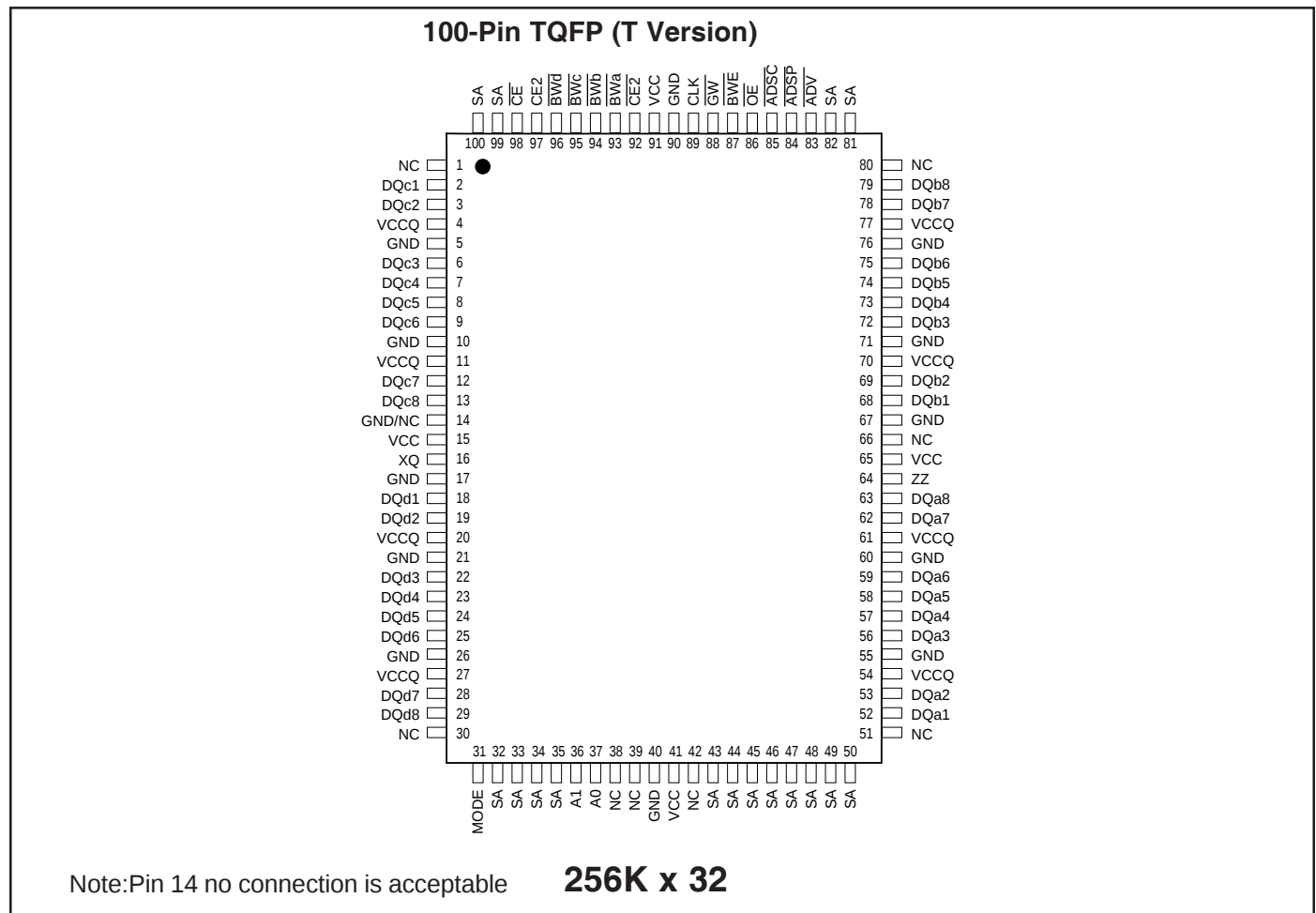


## PIN DESCRIPTIONS

|          |                                                                                      |
|----------|--------------------------------------------------------------------------------------|
| A0, A1   | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A17   | Synchronous Address Inputs                                                           |
| CLK      | Synchronous Clock                                                                    |
| ADSP     | Synchronous Processor Address Status                                                 |
| ADSC     | Synchronous Controller Address Status                                                |
| ADV      | Synchronous Burst Address Advance                                                    |
| BWa -BWd | Synchronous Byte Write Enable                                                        |
| BWE      | Synchronous Byte Write Enable                                                        |
| GW       | Synchronous Global Write Enable                                                      |
| CE , CE2 | Synchronous Chip Enable                                                              |
| OE       | Output Enable                                                                        |

|         |                                               |
|---------|-----------------------------------------------|
| DQa-DQd | Synchronous Data Input/Output                 |
| MODE    | Burst Sequence Mode Selection                 |
| XQ      | Output Drive Control                          |
| Vcc     | +3.3V Power Supply                            |
| GND     | Ground                                        |
| Vccq    | Isolated Output Buffer Supply : +3.3V or 2.5V |
| ZZ      | Snooze Enable                                 |

## PIN CONFIGURATION

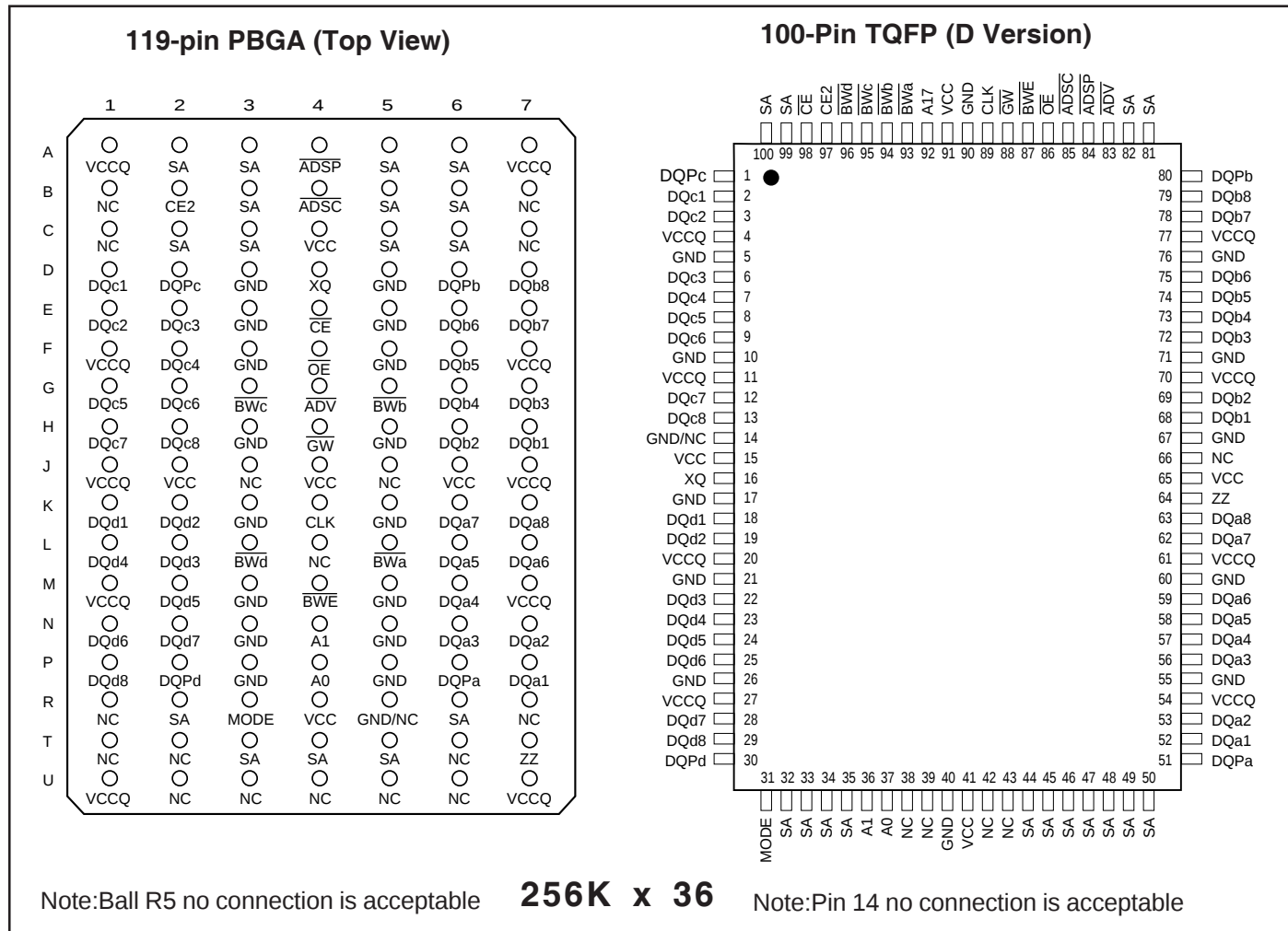


## PIN DESCRIPTIONS

|                                  |                                                                                      |
|----------------------------------|--------------------------------------------------------------------------------------|
| A0, A1                           | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A17                           | Synchronous Address Inputs                                                           |
| CLK                              | Synchronous Clock                                                                    |
| ADSP                             | Synchronous Processor Address Status                                                 |
| ADSC                             | Synchronous Controller Address Status                                                |
| ADV                              | Synchronous Burst Address Advance                                                    |
| BW <sub>a</sub> -BW <sub>d</sub> | Synchronous Byte Write Enable                                                        |
| BWE                              | Synchronous Byte Write Enable                                                        |
| GW                               | Synchronous Global Write Enable                                                      |
| CE, CE2, CE2                     | Synchronous Chip Enable                                                              |
| OE                               | Output Enable                                                                        |

|                                  |                                               |
|----------------------------------|-----------------------------------------------|
| DQ <sub>a</sub> -DQ <sub>d</sub> | Synchronous Data Input/Output                 |
| MODE                             | Burst Sequence Mode Selection                 |
| XQ                               | Output Drive Control                          |
| V <sub>cc</sub>                  | +3.3V Power Supply                            |
| GND                              | Ground                                        |
| V <sub>ccq</sub>                 | Isolated Output Buffer Supply : +3.3V or 2.5V |
| ZZ                               | Snooze Enable                                 |

## PIN CONFIGURATION

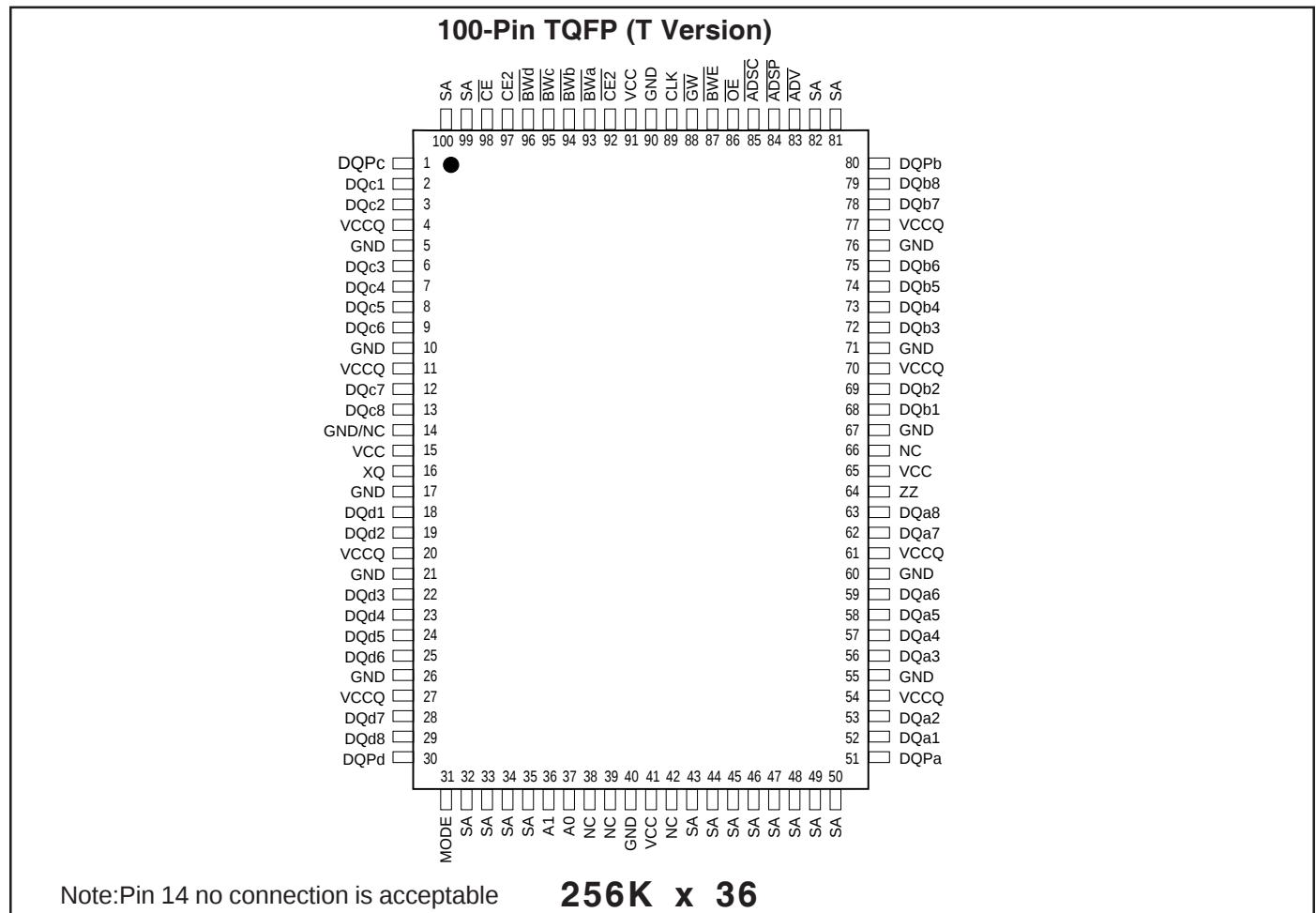


## PIN DESCRIPTIONS

|          |                                                                                      |
|----------|--------------------------------------------------------------------------------------|
| A0, A1   | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A17   | Synchronous Address Inputs                                                           |
| CLK      | Synchronous Clock                                                                    |
| ADSP     | Synchronous Processor Address Status                                                 |
| ADSC     | Synchronous Controller Address Status                                                |
| ADV      | Synchronous Burst Address Advance                                                    |
| BWa -BWd | Synchronous Byte Write Enable                                                        |
| BWE      | Synchronous Byte Write Enable                                                        |
| GW       | Synchronous Global Write Enable                                                      |
| CE , CE2 | Synchronous Chip Enable                                                              |
| OE       | Output Enable                                                                        |

|           |                                               |
|-----------|-----------------------------------------------|
| DQa-DQd   | Synchronous Data Input/Output                 |
| MODE      | Burst Sequence Mode Selection                 |
| XQ        | Output Drive Control                          |
| Vcc       | +3.3V Power Supply                            |
| GND       | Ground                                        |
| Vccq      | Isolated Output Buffer Supply : +3.3V or 2.5V |
| ZZ        | Snooze Enable                                 |
| DQPa-DQPd | Parity Data I/O                               |

## PIN CONFIGURATION

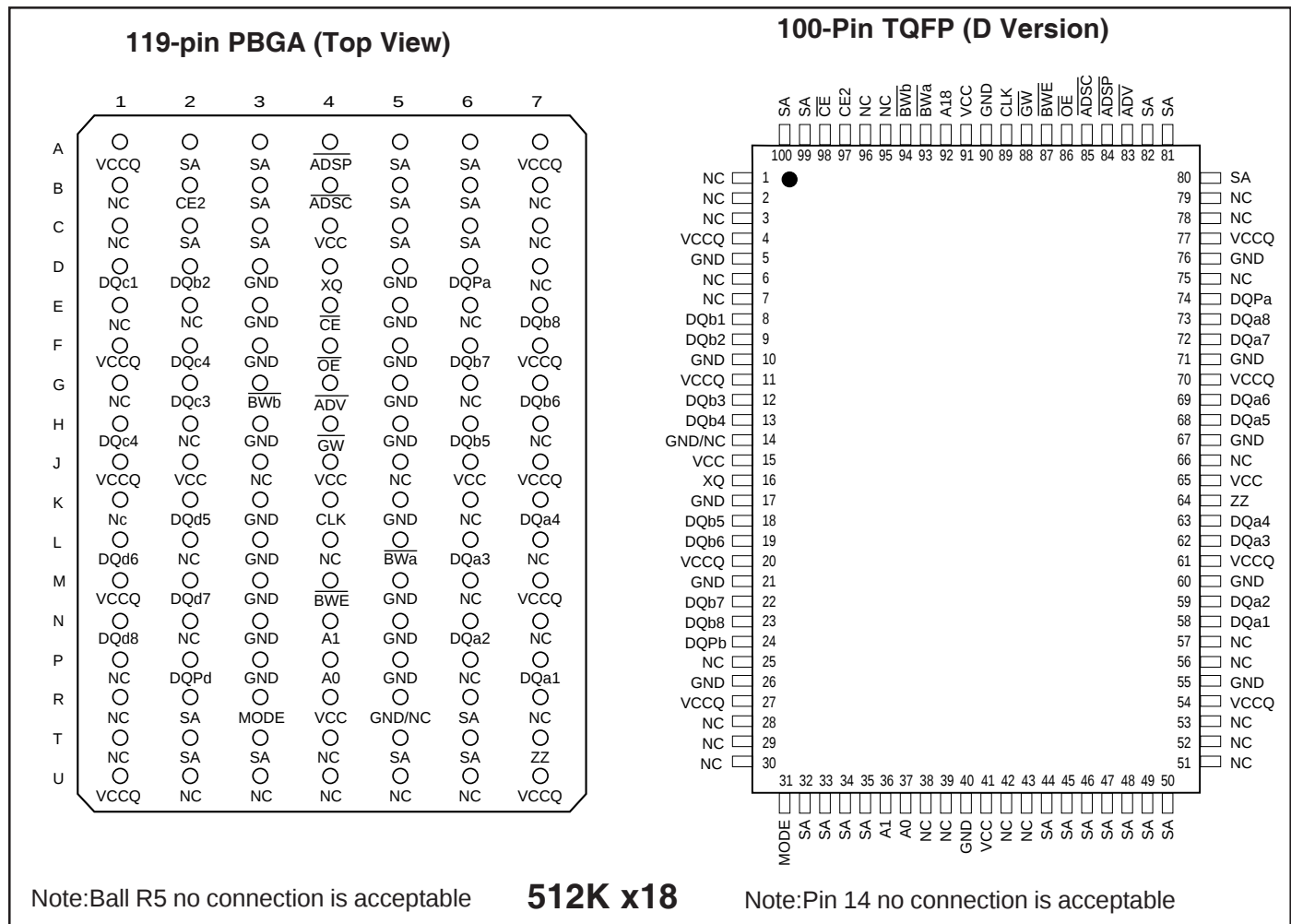


## PIN DESCRIPTIONS

|            |                                                                                      |
|------------|--------------------------------------------------------------------------------------|
| A0, A1     | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A17     | Synchronous Address Inputs                                                           |
| CLK        | Synchronous Clock                                                                    |
| ADSP       | Synchronous Processor Address Status                                                 |
| ADSC       | Synchronous Controller Address Status                                                |
| ADV        | Synchronous Burst Address Advance                                                    |
| BWa -BWd   | Synchronous Byte Write Enable                                                        |
| BWE        | Synchronous Byte Write Enable                                                        |
| GW         | Synchronous Global Write Enable                                                      |
| CE,CE2,CE2 | Synchronous Chip Enable                                                              |
| OE         | Output Enable                                                                        |

|           |                                               |
|-----------|-----------------------------------------------|
| DQa-DQd   | Synchronous Data Input/Output                 |
| MODE      | Burst Sequence Mode Selection                 |
| XQ        | Output Drive Control                          |
| Vcc       | +3.3V Power Supply                            |
| GND       | Ground                                        |
| Vccq      | Isolated Output Buffer Supply : +3.3V or 2.5V |
| ZZ        | Snooze Enable                                 |
| DQPa-DQPd | Parity Data I/O                               |

## PIN CONFIGURATION

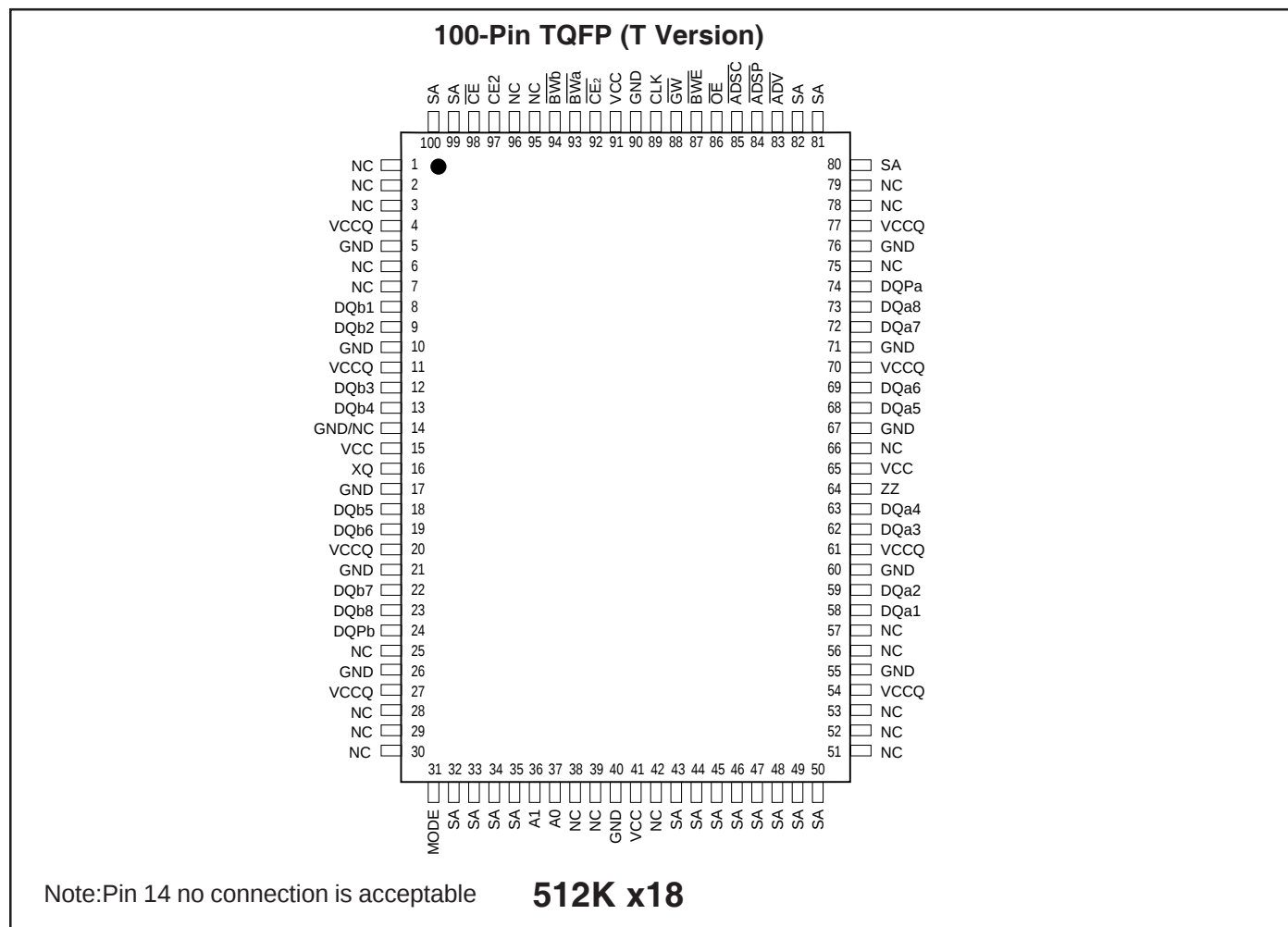


## PIN DESCRIPTIONS

|          |                                                                                      |
|----------|--------------------------------------------------------------------------------------|
| A0, A1   | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A18   | Synchronous Address Inputs                                                           |
| CLK      | Synchronous Clock                                                                    |
| ADSP     | Synchronous Processor Address Status                                                 |
| ADSC     | Synchronous Controller Address Status                                                |
| ADV      | Synchronous Burst Address Advance                                                    |
| BWa -BWb | Synchronous Byte Write Enable                                                        |
| BWE      | Synchronous Byte Write Enable                                                        |
| GW       | Synchronous Global Write Enable                                                      |
| CE , CE2 | Synchronous Chip Enable                                                              |
| OE       | Output Enable                                                                        |

|            |                                                                      |
|------------|----------------------------------------------------------------------|
| DQa-DQb    | Synchronous Data Input/Output                                        |
| MODE       | Burst Sequence Mode Selection                                        |
| XQ         | Output Drive Control                                                 |
| Vcc        | +3.3V Power Supply                                                   |
| GND        | Ground                                                               |
| Vccq       | Isolated Output Buffer Supply : +3.3V or 2.5V                        |
| ZZ         | Snooze Enable                                                        |
| DQPa-DQ Pb | Parity Data I/O DQPa is parity for DQa1-8;DQ Pb is parity for DQb1-8 |

## PIN CONFIGURATION



## PIN DESCRIPTIONS

|              |                                                                                      |
|--------------|--------------------------------------------------------------------------------------|
| A0, A1       | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A18       | Synchronous Address Inputs                                                           |
| CLK          | Synchronous Clock                                                                    |
| ADSP         | Synchronous Processor Address Status                                                 |
| ADSC         | Synchronous Controller Address Status                                                |
| ADV          | Synchronous Burst Address Advance                                                    |
| BWa -BWb     | Synchronous Byte Write Enable                                                        |
| BWE          | Synchronous Byte Write Enable                                                        |
| GW           | Synchronous Global Write Enable                                                      |
| CE, CE2, CE2 | Synchronous Chip Enable                                                              |
| OE           | Output Enable                                                                        |

|           |                                                                      |
|-----------|----------------------------------------------------------------------|
| DQa-DQb   | Synchronous Data Input/Output                                        |
| MODE      | Burst Sequence Mode Selection                                        |
| XQ        | Output Drive Control                                                 |
| Vcc       | +3.3V Power Supply                                                   |
| GND       | Ground                                                               |
| Vccq      | Isolated Output Buffer Supply : +3.3V or 2.5V                        |
| ZZ        | Snooze Enable                                                        |
| DQPa-DQPb | Parity Data I/O DQPa is parity for DQa1-8; DQPb is parity for DQb1-8 |

## Mode Pin Functions

| Mode Name            | Pin Name | State   | Function                   |
|----------------------|----------|---------|----------------------------|
| Burst Order Control  | MODE     | L       | Linear Burst               |
|                      |          | H or NC | Interleaved Burst          |
| Power Down Control   | ZZ       | L or NC | Active                     |
|                      |          | H       | Standby                    |
| Output Drive Control | XQ       | L       | High Drive (Low Impedance) |
|                      |          | H       | Low Drive (High Impedance) |

Note:

There are pull-up devices on the MODE, XQ, SCD, and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

## TRUTH TABLE

| Operation                   | Address  |                 |     |                  |                   |                   |                  |                    |                 |        |
|-----------------------------|----------|-----------------|-----|------------------|-------------------|-------------------|------------------|--------------------|-----------------|--------|
|                             | Used     | $\overline{CE}$ | CE2 | $\overline{CE2}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | $\overline{OE}$ | DQ     |
| Deselected, Power-down      | None     | H               | X   | X                | X                 | L                 | X                | X                  | X               | High-Z |
| Deselected, Power-down      | None     | L               | X   | H                | L                 | X                 | X                | X                  | X               | High-Z |
| Deselected, Power-down      | None     | L               | L   | X                | L                 | X                 | X                | X                  | X               | High-Z |
| Deselected, Power-down      | None     | L               | X   | H                | H                 | L                 | X                | X                  | X               | High-Z |
| Deselected, Power-down      | None     | L               | L   | X                | H                 | L                 | X                | X                  | X               | High-Z |
| Read Cycle, Begin Burst     | External | L               | H   | L                | L                 | X                 | X                | X                  | X               | Q      |
| Read Cycle, Begin Burst     | External | L               | H   | L                | H                 | L                 | X                | Read               | X               | Q      |
| Write Cycle, Begin Burst    | External | L               | H   | L                | H                 | L                 | X                | Write              | X               | D      |
| Read Cycle, Continue Burst  | Next     | X               | X   | X                | H                 | H                 | L                | Read               | L               | Q      |
| Read Cycle, Continue Burst  | Next     | X               | X   | X                | H                 | H                 | L                | Read               | H               | High-Z |
| Read Cycle, Continue Burst  | Next     | H               | X   | X                | X                 | H                 | L                | Read               | L               | Q      |
| Read Cycle, Continue Burst  | Next     | H               | X   | X                | X                 | H                 | L                | Read               | H               | High-Z |
| Write Cycle, Continue Burst | Next     | X               | X   | X                | H                 | H                 | L                | Write              | X               | D      |
| Write Cycle, Continue Burst | Next     | H               | X   | X                | X                 | H                 | L                | Write              | X               | D      |
| Read Cycle, Suspend Burst   | Current  | X               | X   | X                | H                 | H                 | H                | Read               | L               | Q      |
| Read Cycle, Suspend Burst   | Current  | X               | X   | X                | H                 | H                 | H                | Read               | H               | High-Z |
| Read Cycle, Suspend Burst   | Current  | H               | X   | X                | X                 | H                 | H                | Read               | L               | Q      |
| Read Cycle, Suspend Burst   | Current  | H               | X   | X                | X                 | H                 | H                | Read               | H               | High-Z |
| Write Cycle, Suspend Burst  | Current  | X               | X   | X                | H                 | H                 | H                | Write              | X               | D      |
| Write Cycle, Suspend Burst  | Current  | H               | X   | X                | X                 | H                 | H                | Write              | X               | D      |

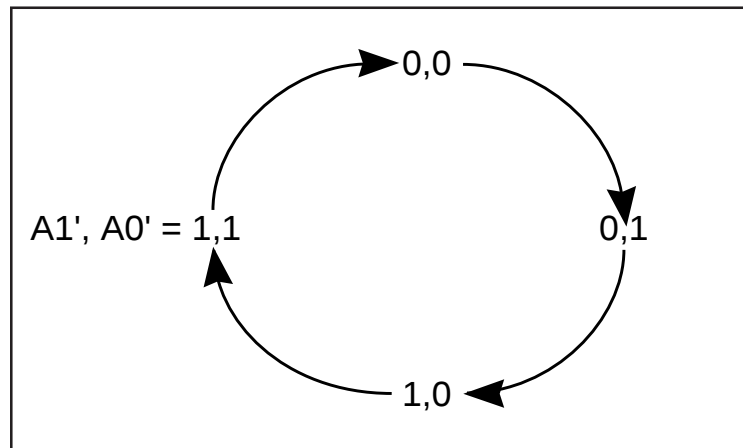
## PARTIAL TRUTH TABLE

| Function        | GW | BWE | BW <sub>a</sub> | BW <sub>b</sub> | BW <sub>c</sub> | BW <sub>d</sub> |
|-----------------|----|-----|-----------------|-----------------|-----------------|-----------------|
| Read            | H  | H   | X               | X               | X               | X               |
| Read            | H  | L   | H               | H               | H               | H               |
| Write Byte 1    | H  | L   | L               | H               | H               | H               |
| Write All Bytes | H  | L   | L               | L               | L               | L               |
| Write All Bytes | L  | X   | X               | X               | X               | X               |

## INTERLEAVED BURST ADDRESS TABLE (MODE = VCC or No Connect)

| External Address | 1st Burst Address | 2nd Burst Address | 3rd Burst Address |
|------------------|-------------------|-------------------|-------------------|
| A1 A0            | A1 A0             | A1 A0             | A1 A0             |
| 00               | 01                | 10                | 11                |
| 01               | 00                | 11                | 10                |
| 10               | 11                | 00                | 01                |
| 11               | 10                | 01                | 00                |

## LINEAR BURST ADDRESS TABLE (MODE = GND)



## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

| Symbol                             | Parameter                                                     | Value                          | Unit |
|------------------------------------|---------------------------------------------------------------|--------------------------------|------|
| T <sub>BIAS</sub>                  | Temperature Under Bias                                        | −40 to +85                     | °C   |
| T <sub>STG</sub>                   | Storage Temperature                                           | −55 to +150                    | °C   |
| P <sub>D</sub>                     | Power Dissipation                                             | 1.6                            | W    |
| I <sub>OUT</sub>                   | Output Current (per I/O)                                      | 100                            | mA   |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage Relative to GND for I/O Pins                          | −0.5 to V <sub>CCQ</sub> + 0.5 | V    |
| V <sub>IN</sub>                    | Voltage Relative to GND for<br>for Address and Control Inputs | −0.5 to V <sub>CC</sub> + 0.5  | V    |
| V <sub>CC</sub>                    | Voltage on V <sub>CC</sub> Supply Relative to GND             | −0.5 to 4.6                    | V    |

### Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

## OPERATING RANGE

| Range      | Ambient Temperature | V <sub>CC</sub> | V <sub>CCQ</sub> |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C        | 3.3V, +10%, -5% | 2.375–3.6V       |
| Industrial | -40°C to +85°C      | 3.3V, +10%, -5% | 2.375–3.6V       |

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol          | Parameter              | Test Conditions                                                  | Min. | Max.                   | Unit |
|-----------------|------------------------|------------------------------------------------------------------|------|------------------------|------|
| V <sub>OH</sub> | Output HIGH Voltage    | I <sub>OH</sub> = -2.0 mA, V <sub>CCQ</sub> = 2.5V               | 1.7  | —                      | V    |
|                 |                        | I <sub>OH</sub> = -4.0 mA, V <sub>CCQ</sub> = 3.3V               | 2.4  | —                      | V    |
| V <sub>OL</sub> | Output LOW Voltage     | I <sub>OL</sub> = 2.0 mA, V <sub>CCQ</sub> = 2.5V                | —    | 0.7                    | V    |
|                 |                        | I <sub>OL</sub> = 8.0 mA, V <sub>CCQ</sub> = 3.3V                | —    | 0.4                    | V    |
| V <sub>IH</sub> | Input HIGH Voltage     | V <sub>CCQ</sub> = 2.5V                                          | 1.7  | V <sub>CCQ</sub> + 0.3 | V    |
|                 |                        | V <sub>CCQ</sub> = 3.3V                                          | 2.0  | V <sub>CCQ</sub> + 0.3 | V    |
| V <sub>IL</sub> | Input LOW Voltage      | V <sub>CCQ</sub> = 2.5V                                          | -0.3 | 0.7                    | V    |
|                 |                        | V <sub>CCQ</sub> = 3.3V                                          | -0.3 | 0.8                    | V    |
| I <sub>LI</sub> | Input Leakage Current  | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> (1)                      | -2   | 2                      | μA   |
| I <sub>LO</sub> | Output Leakage Current | GND ≤ V <sub>OUT</sub> ≤ V <sub>CCQ</sub> , OE = V <sub>IH</sub> | -2   | 2                      | μA   |

Notes:

1. The MODE, ZZ, XQ, pin14 pin has an internal pullup. and input leakage = ±10 μA .

## POWER SUPPLY CHARACTERISTICS (Over Operating Range)

| Parameter                      | Test Conditions                                                                                                            | Symbol           |      | -6.5<br>Max. | -7.5<br>Max. | -8.5<br>Max. | -9.5<br>Max. | Unit |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------|------------------|------|--------------|--------------|--------------|--------------|------|
| AC Operating<br>Supply Current | Device Selected,                                                                                                           | I <sub>CC1</sub> | Com. | 300          | 290          | 280          | 370          | mA   |
|                                | All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub><br>OE = V <sub>IH</sub> , V <sub>CC</sub> = Max<br>f = 1/t <sub>KC</sub> |                  | Ind. | 320          | 310          | 300          | 290          | mA   |
| Clock Running                  | Device Deselected,                                                                                                         | I <sub>CC2</sub> | Com. | 110          | 100          | 90           | 90           | mA   |
|                                | V <sub>CC</sub> = Max.,<br>All Inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub><br>f = 1/t <sub>KC</sub>                      |                  | Ind. | 120          | 110          | 100          | 100          | mA   |
| COMS Standby                   | Device Deselected,                                                                                                         | I <sub>SB</sub>  | Com. | 90           | 90           | 90           | 90           | mA   |
|                                | V <sub>CC</sub> = Max.,<br>All Inputs ≤ 0.2V or<br>≥ V <sub>CC</sub> - 0.2V; f = 0                                         |                  | Ind. | 100          | 100          | 100          | 100          | mA   |
| Power Down Mode                | V <sub>CC</sub> = Max                                                                                                      | I <sub>ZZ</sub>  | Com. | 80           | 80           | 80           | 80           | mA   |
|                                | ZZ ≥ V <sub>CC</sub> - 0.2V<br>f = 0,<br>All input ≤ 0.2V or ≥ V <sub>CC</sub> - 0.2V                                      |                  | Ind. | 90           | 90           | 90           | 90           | mA   |

## CAPACITANCE <sup>(1,2)</sup>

| Symbol           | Parameter Conditions     | Max.                  | Unit |
|------------------|--------------------------|-----------------------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 6 pF |
| C <sub>OUT</sub> | Input/Output Capacitance | V <sub>OUT</sub> = 0V | 8 pF |

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.3V.

## AC TEST CONDITIONS

| Parameter                                   | Unit                                                   |
|---------------------------------------------|--------------------------------------------------------|
| Input Pulse Level                           | 0V to 3.0V                                             |
| Input Rise and Fall Times                   | 1.5 ns                                                 |
| Input and Output Timing and Reference Level | 1.5V for 3.3V I/O<br>V <sub>CCQ</sub> /2V for 2.5V I/O |
| Output Load                                 | See Figures 1 and 2                                    |

## AC TEST LOADS

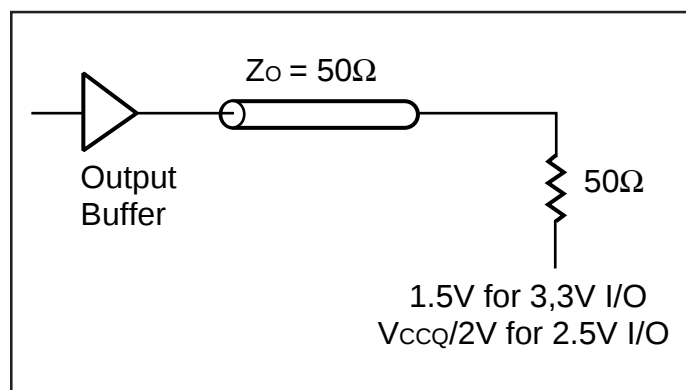


Figure 1

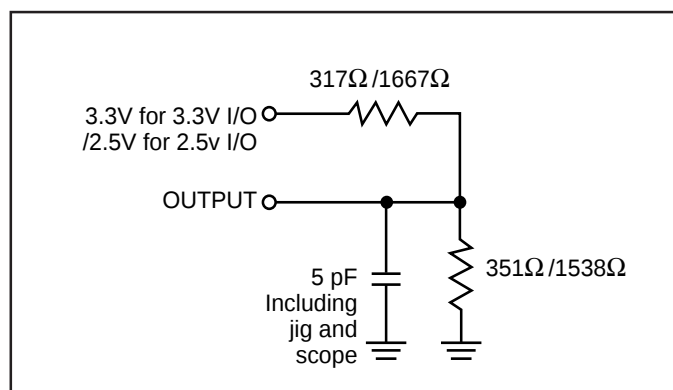


Figure 2

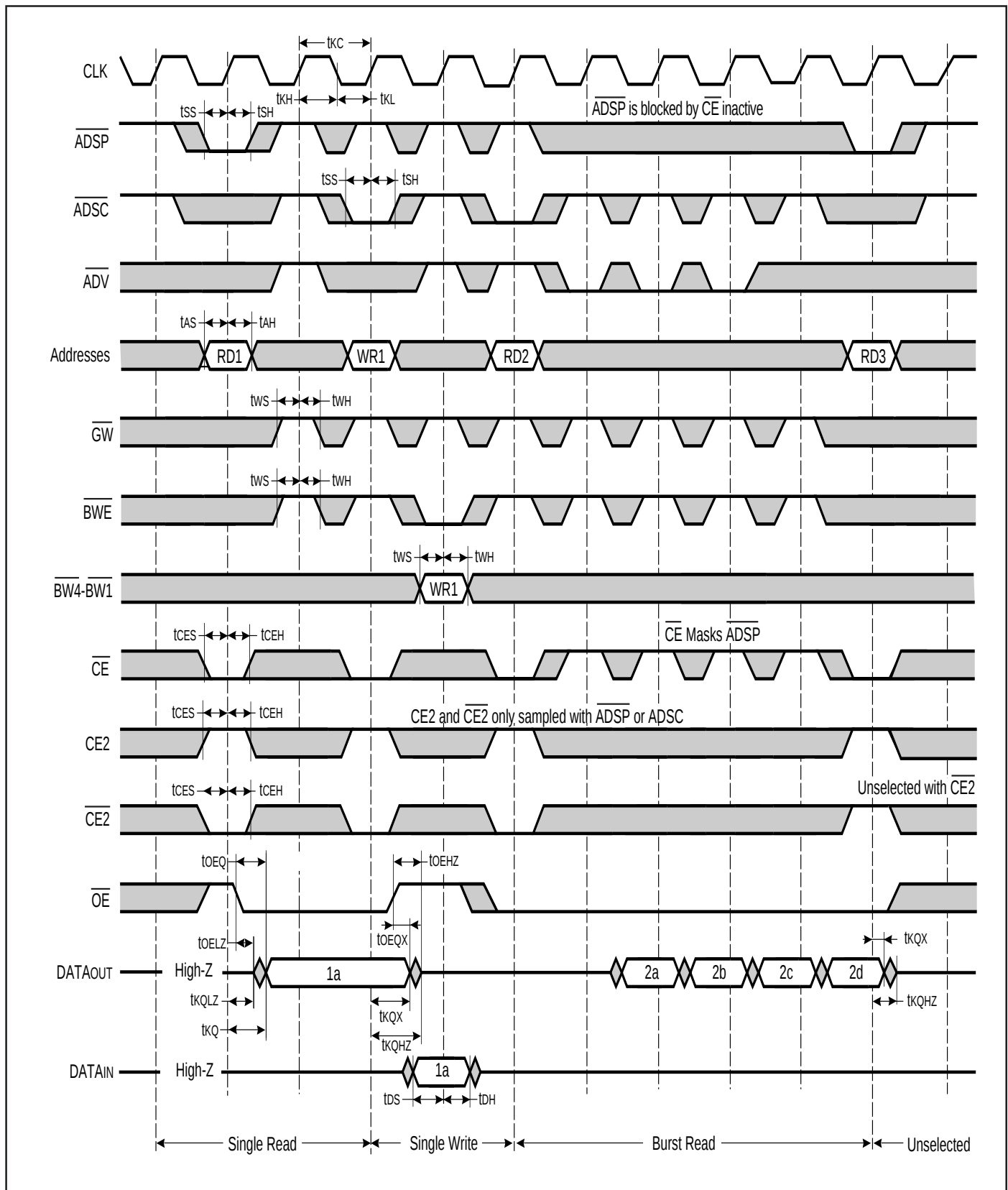
## READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol                             | Parameter                      | -6.5 |      | -7.5 |      | -8.5 |      | -9.5 |      | Unit |
|------------------------------------|--------------------------------|------|------|------|------|------|------|------|------|------|
|                                    |                                | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |      |
| t <sub>KC</sub>                    | Cycle Time                     | 7.5  | —    | 8.5  | —    | 10   | —    | 11   | —    | ns   |
| t <sub>KQ</sub>                    | Clock Access Time              | —    | 6.5  | —    | 7.5  | —    | 8.5  | —    | 9.5  | ns   |
| t <sub>KQX</sub> <sup>(1)</sup>    | Clock High to Output Invalid   | 2.5  | —    | 2.5  | —    | 3.0  | —    | 3.0  | —    | ns   |
| t <sub>KQLZ</sub> <sup>(1,2)</sup> | Clock High to Output Low-Z     | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   |
| t <sub>KH</sub>                    | Clock High Pulse Width         | 1.6  | —    | 2    | —    | 2.3  | —    | 2.8  | —    | ns   |
| t <sub>KL</sub>                    | Clock Low Pulse Width          | 1.6  | —    | 2    | —    | 2.3  | —    | 2.8  | —    | ns   |
| t <sub>KQHZ</sub> <sup>(1,2)</sup> | Clock High to Output High-Z    | —    | 3.1  | —    | 3.1  | —    | 3.5  | —    | 4    | ns   |
| t <sub>OEQ</sub>                   | Output Enable to Output Valid  | —    | 3.1  | —    | 3.1  | —    | 3.5  | —    | 4    | ns   |
| t <sub>ELZ</sub> <sup>(1,2)</sup>  | Output Enable to Output Low-Z  | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   |
| t <sub>EHZ</sub> <sup>(1,2)</sup>  | Output Enable to Output High-Z | —    | 3.0  | —    | 3.0  | —    | 3.5  | —    | 4    | ns   |
| t <sub>AS</sub>                    | Address Setup Time             | 1.5  | —    | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
| t <sub>SS</sub>                    | Address Status Setup Time      | 1.5  | —    | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
| t <sub>WS</sub>                    | Write Setup Time               | 1.5  | —    | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
| t <sub>CES</sub>                   | Chip Enable Setup Time         | 1.5  | —    | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
| t <sub>AVS</sub>                   | Address Advance Setup Time     | 1.5  | —    | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
| t <sub>DS</sub>                    | Data Setup time                |      |      | 1.5  | —    | 1.5  | —    | 1.5  | —    | ns   |
| t <sub>DH</sub>                    | Data Hold time                 |      |      | 0.5  | —    | 0.5  | —    | 0.5  | —    | ns   |
| t <sub>AH</sub>                    | Address Hold Time              | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    | ns   |
| t <sub>SH</sub>                    | Address Status Hold Time       | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    | ns   |
| t <sub>WH</sub>                    | Write Hold Time                | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    | ns   |
| t <sub>CEH</sub>                   | Chip Enable Hold Time          | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    | ns   |
| t <sub>AVH</sub>                   | Address Advance Hold Time      | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    | ns   |
| t <sub>ZZS</sub>                   | ZZ Setup Time                  | 2    | —    | 2    | —    | 2    | —    | 2    | —    | cyc  |
| t <sub>ZZREC</sub>                 | ZZ Recovery Time               | 2    | —    | 2    | —    | 2    | —    | 2    | —    | cyc  |

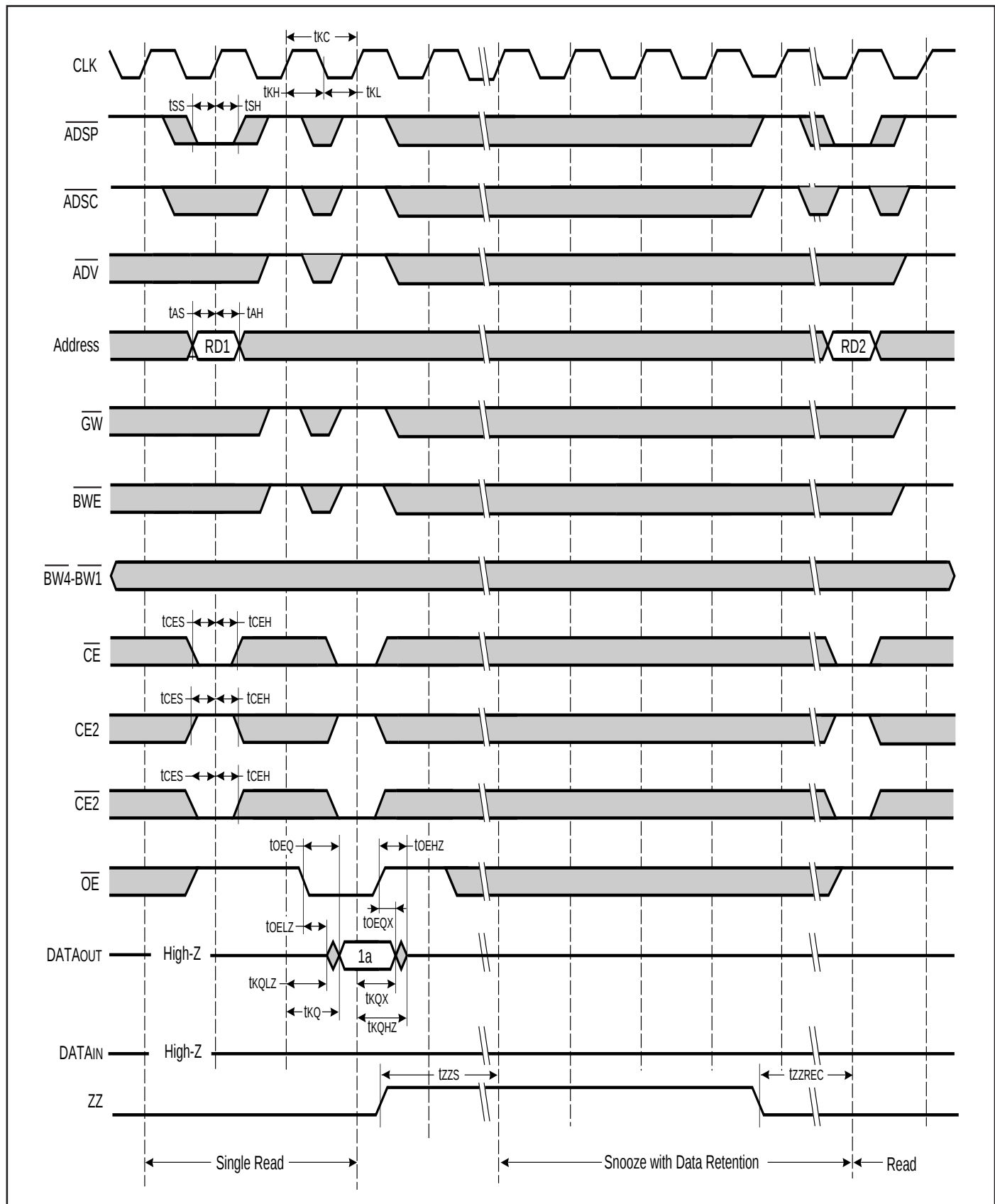
### Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

## READ/WRITE CYCLE TIMING: FLOW THROUGH



## SNOOZE AND RECOVERY CYCLE TIMING



## ORDERING INFORMATION

### Commercial Range: 0°C to +70°C

| Speed | Order Part Number  | Package          |
|-------|--------------------|------------------|
| -6.5  | IC61SF25632T-6.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF25632D-6.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF25632D-6.5B  | 14*22mm PBGA     |
| -7.5  | IC61SF25632T-7.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF25632D-7.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF25632D-7.5B  | 14*22mm PBGA     |
| -8.5  | IC61SF25632T-8.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25632D-8.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25632D-8.5B  | 14*22mm PBGA     |
| -9.5  | IC61SF25632T-9.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25632D-9.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25632D-9.5B  | 14*22mm PBGA     |

| Speed | Order Part Number  | Package          |
|-------|--------------------|------------------|
| -6.5  | IC61SF25636T-6.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF25636D-6.5Q  | 14*20*1.4mm LQFP |
|       | IC61SF25636D-6.5B  | 14*22mm PBGA     |
| -7.5  | IC61SF25636T-7.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF25636D-7.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF25636D-7.5B  | 14*22mm PBGA     |
| -8.5  | IC61SF25636T-8.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25636D-8.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25636D-8.5B  | 14*22mm PBGA     |
| -9.5  | IC61SF25636T-9.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25636D-9.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF25636D-9.5B  | 14*22mm PBGA     |

| Speed | Order Part Number  | Package          |
|-------|--------------------|------------------|
| -6.5  | IC61SF51218T-6.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF51218D-6.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF51218D-6.5B  | 14*22mm PBGA     |
| -7.5  | IC61SF51218T-7.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF51218D-7.5TQ | 14*20*1.4mm LQFP |
|       | IC61SF51218D-7.5B  | 14*22mm PBGA     |
| -8.5  | IC61SF51218T-8.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF51218D-8.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF51218D-8.5B  | 14*22mm PBGA     |
| -9.5  | IC61SF51218T-9.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF51218D-9.5TQ | 14*20*1.4mm TQFP |
|       | IC61SF51218D-9.5B  | 14*22mm PBGA     |

### Industrial Range: -40°C to 85°C

| Speed | Order Part Number   | Package          |
|-------|---------------------|------------------|
| -6.5  | IC61SF25632T-6.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF25632D-6.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF25632D-6.5BI  | 14*22mm PBGA     |
| -7.5  | IC61SF25632T-7.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF25632D-7.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF25632D-7.5BI  | 14*22mm PBGA     |
| -8.5  | IC61SF25632T-8.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25632D-8.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25632D-8.5BI  | 14*22mm PBGA     |
| -9.5  | IC61SF25632T-9.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25632D-9.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25632D-9.5BI  | 14*22mm PBGA     |

| Speed | Order Part Number   | Package          |
|-------|---------------------|------------------|
| -6.5  | IC61SF25636T-6.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF25636D-6.5QI  | 14*20*1.4mm LQFP |
|       | IC61SF25636D-6.5BI  | 14*22mm PBGA     |
| -7.5  | IC61SF25636T-7.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF25636D-7.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF25636D-7.5BI  | 14*22mm PBGA     |
| -8.5  | IC61SF25636T-8.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25636D-8.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25636D-8.5BI  | 14*22mm PBGA     |
| -9.5  | IC61SF25636T-9.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25636D-9.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF25636D-9.5BI  | 14*22mm PBGA     |

| Speed | Order Part Number   | Package          |
|-------|---------------------|------------------|
| -6.5  | IC61SF51218T-6.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF51218D-6.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF51218D-6.5BI  | 14*22mm PBGA     |
| -7.5  | IC61SF51218T-7.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF51218D-7.5TQI | 14*20*1.4mm LQFP |
|       | IC61SF51218D-7.5BI  | 14*22mm PBGA     |
| -8.5  | IC61SF51218T-8.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF51218D-8.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF51218D-8.5BI  | 14*22mm PBGA     |
| -9.5  | IC61SF51218T-9.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF51218D-9.5TQI | 14*20*1.4mm TQFP |
|       | IC61SF51218D-9.5BI  | 14*22mm PBGA     |



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