

Non Compensated Single Operational Amplifiers

LM301A, LM201A, LM201AV

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/ μ s can be obtained.

Features

- Low Input Offset Current: 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics
- Pb-Free Packages are Available

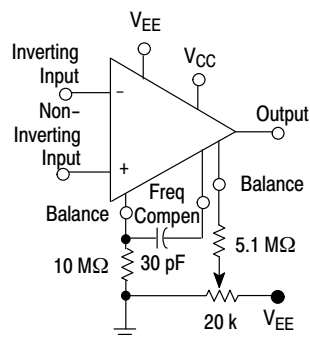


Figure 1. Standard Compensation and Offset Balancing Circuit

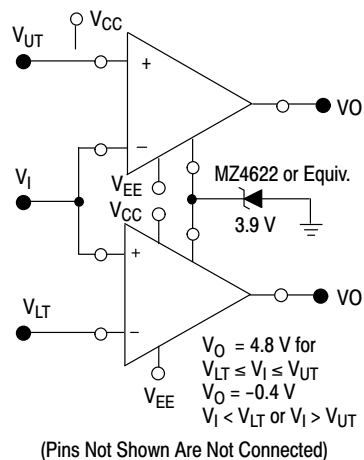
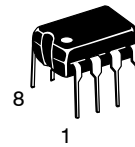
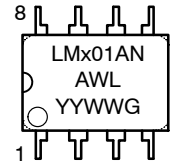


Figure 2. Double-Ended Limit Detector

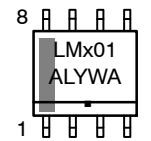
MARKING DIAGRAMS



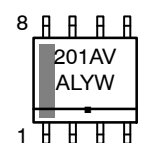
PDIP-8
N SUFFIX
CASE 626



SOIC-8
D SUFFIX
CASE 751

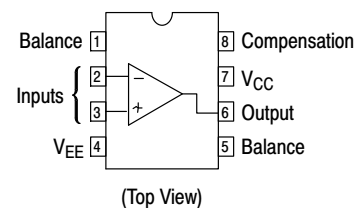


LM201AV/DR2G



x = 2 or 3
 A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G = Pb-Free Package
 ■ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

LM301A, LM201A, LM201AV

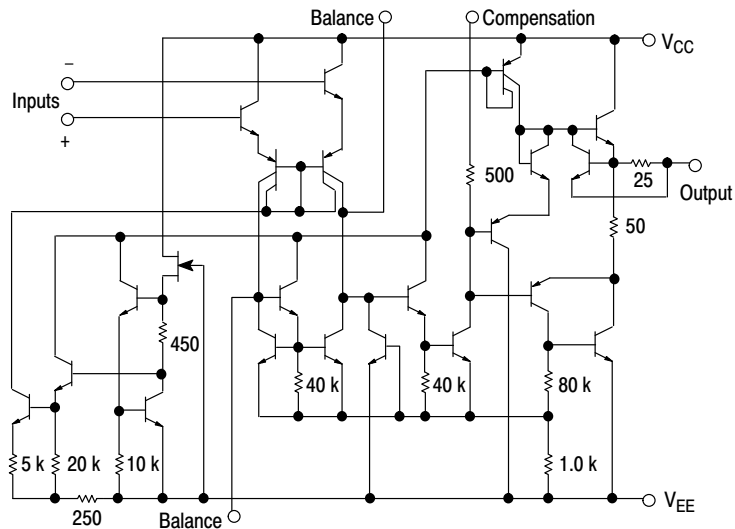


Figure 3. Representative Circuit Schematic

ORDERING INFORMATION

Device	Package	Shipping [†]
LM301ADR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
LM201ADR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
LM201AVDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 1)

LM301ADG	SOIC-8 (Pb-Free)	98 Units / Rail
LM301AN	PDIP-8	50 Units / Rail
LM301ANG	PDIP-8 (Pb-Free)	50 Units / Rail
LM201ADG	SOIC-8 (Pb-Free)	98 Units / Rail
LM201AN	PDIP-8	50 Units / Rail
LM201ANG	PDIP-8 (Pb-Free)	50 Units / Rail

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

LM301A, LM201A, LM201AV

MAXIMUM RATINGS

Rating	Symbol	Value			Unit
		LM201A	LM201AV	LM301A	
Power Supply Voltage	V_{CC}, V_{EE}	± 22	± 22	± 18	Vdc
Input Differential Voltage	V_{ID}	± 30			V
Input Common Mode Range (Note 1)	V_{ICR}	± 15			V
Output Short Circuit Duration	t_{SC}	Continuous			
Power Dissipation (Package Limitation)	P_D				
Plastic Dual-In-Line Package		625	625	625	mW
Derate above $T_A = +25^\circ\text{C}$		5.0	5.0	5.0	mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	-25 to $+85$	-40 to $+105$	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$			$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

LM301A, LM201A, LM201AV

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from $\pm 5.0\text{ V}$ to $\pm 20\text{ V}$ for the LM201A and LM201AV, and from $\pm 5.0\text{ V}$ to $\pm 15\text{ V}$ for the LM301A.

Characteristic	Symbol	LM201A / LM201AV			LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 50\text{ k}\Omega$)	V_{IO}	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_{IB}	–	30	75	–	70	250	nA
Input Resistance	r_i	1.5	4.0	–	0.5	2.0	–	$M\Omega$
Supply Current	I_{CC}, I_{EE}							mA
$V_{CC}/V_{EE} = \pm 20\text{ V}$		–	1.8	3.0	–	–	–	
$V_{CC}/V_{EE} = \pm 15\text{ V}$		–	–	–	–	1.8	3.0	
Large Signal Voltage Gain ($V_{CC}/V_{EE} = \pm 15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L > 2.0\text{ k}\Omega$)	A_V	50	160	–	25	160	–	V/mV

The following specifications apply over the operating temperature range.

Input Offset Voltage ($R_S \leq 50\text{ k}\Omega$)	V_{IO}	–	–	3.0	–	–	10	mV
Input Offset Current	I_{IO}	–	–	20	–	–	70	nA
Avg Temperature Coefficient of Input Offset Voltage (Note 2) $T_A(\text{min}) \leq T_A \leq T_A(\text{max})$	$\Delta V_{IO}/\Delta T$	–	3.0	15	–	6.0	30	$\mu\text{V}/^\circ\text{C}$
Avg Temperature Coefficient of Input Offset Current (Note 2) $+25^\circ\text{C} \leq T_A \leq T_A(\text{max})$ $T_A(\text{min}) \leq T_A \leq 25^\circ\text{C}$	$\Delta I_{IO}/\Delta T$	–	0.01 0.02	0.1 0.2	–	0.01 0.02	0.3 0.6	nA/ $^\circ\text{C}$
Input Bias Current	I_{IB}	–	–	100	–	–	300	nA
Large Signal Voltage Gain ($V_{CC}/V_{EE} = \pm 15\text{ V}$, $V_O = \pm 10\text{ V}$, $R_L > 2.0\text{ k}\Omega$)	A_{VOL}	25	–	–	15	–	–	V/mV
Input Voltage Range $V_{CC}/V_{EE} = \pm 20\text{ V}$ $V_{CC}/V_{EE} = \pm 15\text{ V}$	V_{ICR}	–15 –	– –	+15 –	– –12	– –	– +12	V
Common Mode Rejection ($R_S \leq 50\text{ k}\Omega$)	CMR	80	96	–	70	90	–	dB
Supply Voltage Rejection ($R_S \leq 50\text{ k}\Omega$)	PSR	80	96	–	70	96	–	dB
Output Voltage Swing ($V_{CC}/V_{EE} = \pm 15\text{ V}$, $R_L = \pm 10\text{ k}\Omega$, $R_L > 2.0\text{ k}\Omega$)	V_O	± 12 ± 10	± 14 ± 13	– –	± 12 ± 10	± 14 ± 13	– –	V
Supply Currents ($T_A = T_A(\text{max})$, $V_{CC}/V_{EE} = \pm 20\text{ V}$)	I_{CC}, I_{EE}	–	1.2	2.5	–	–	–	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For supply voltages less than $\pm 15\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
2. Guaranteed by design.

LM301A, LM201A, LM201AV

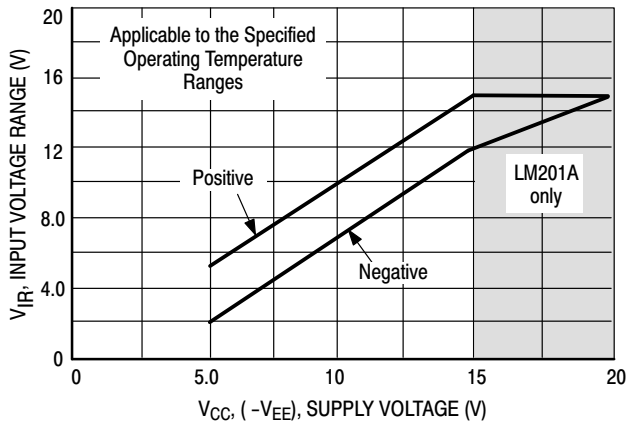


Figure 4. Minimum Input Voltage Range

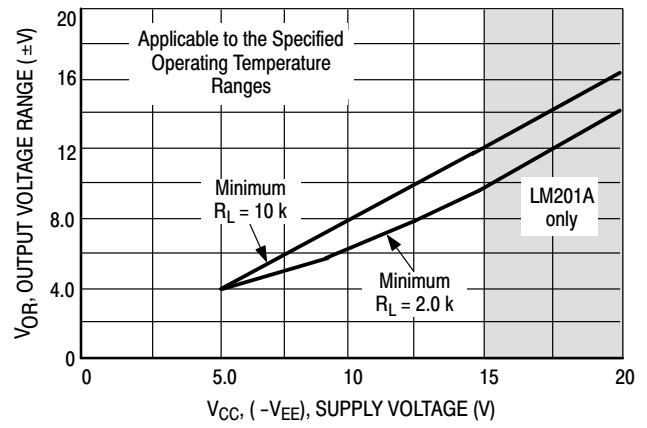


Figure 5. Minimum Output Voltage Swing

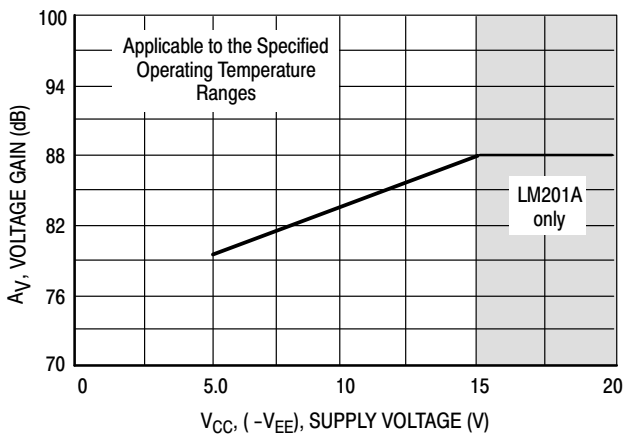


Figure 6. Minimum Voltage Gain

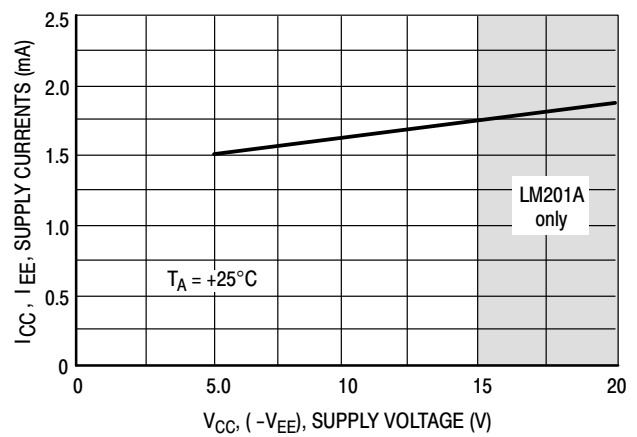


Figure 7. Typical Supply Currents

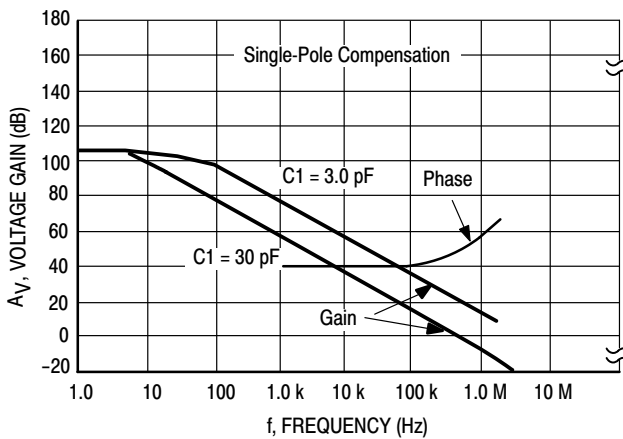


Figure 8. Open Loop Frequency Response

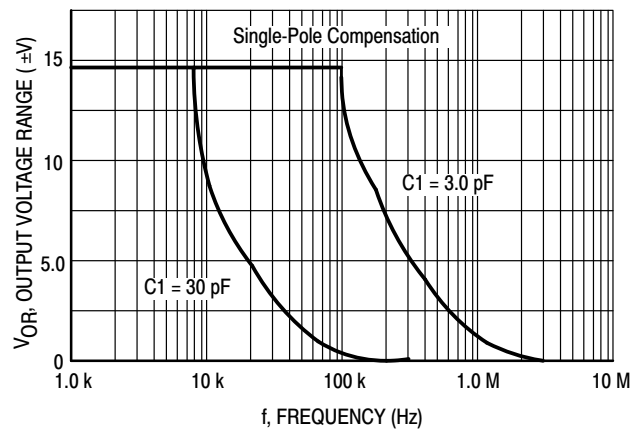


Figure 9. Large Signal Frequency Response

LM301A, LM201A, LM201AV

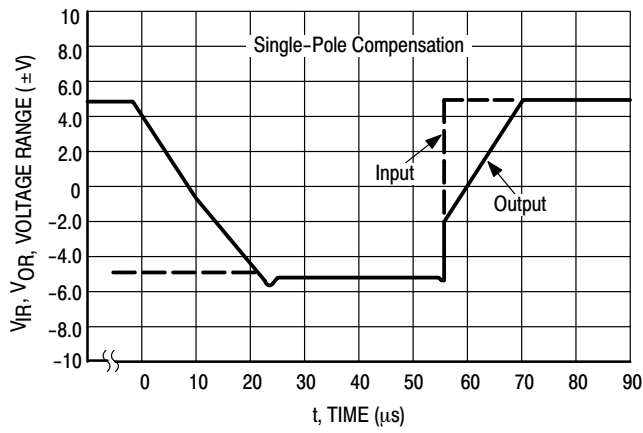


Figure 10. Voltage Follower Pulse Response

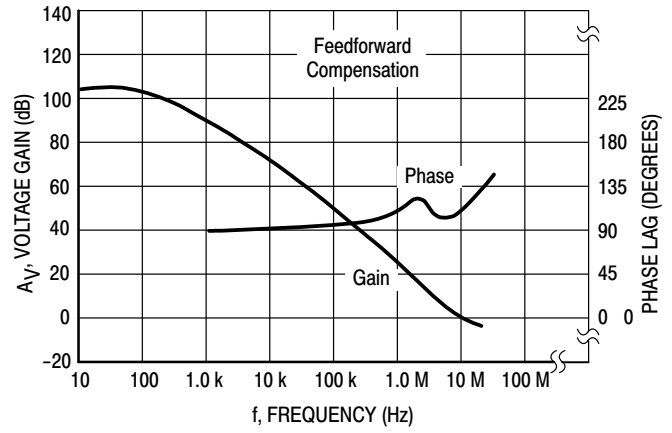


Figure 11. Open Loop Frequency Response

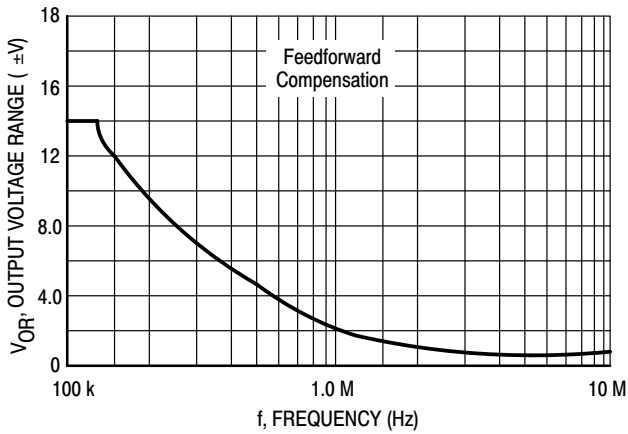


Figure 12. Large Signal Frequency Response

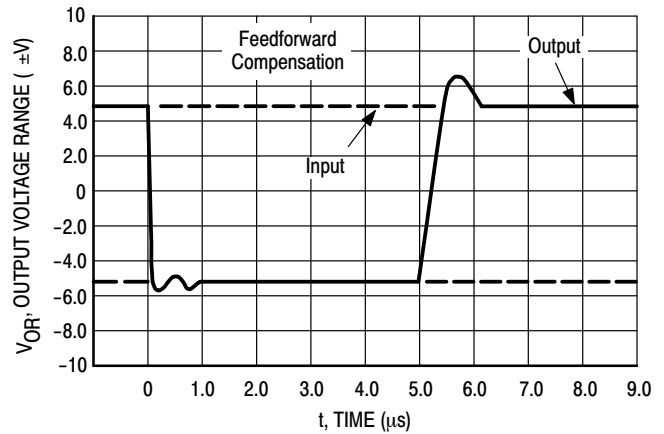


Figure 13. Inverter Pulse Response

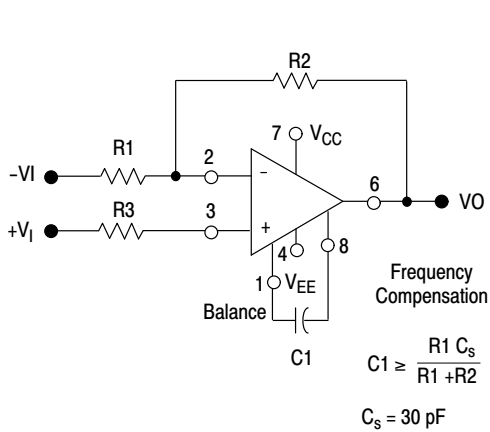


Figure 14. Single-Pole Compensation

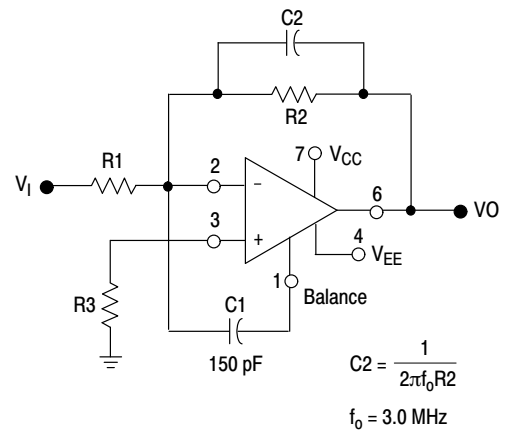


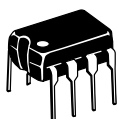
Figure 15. Feedforward Compensation

LM301A, LM201A, LM201AV

REVISION HISTORY

Revision	Description of Changes	Date
12	Rebranded the Data Sheet to onsemi format. LM301ADG, LM301AN, LM301ANG, LM201ADG, LM201AN, LM201ANG OPNs Marked as Discontinued.	07/03/2025

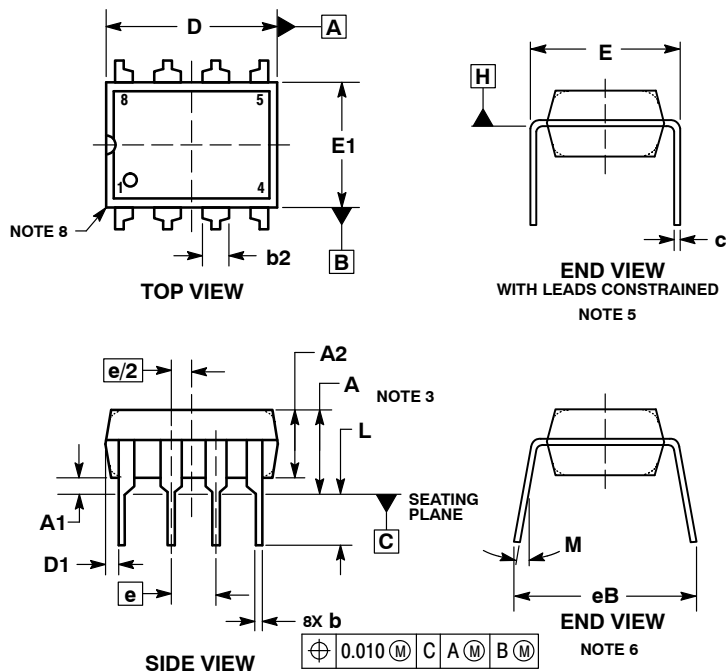
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 1:1

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015



STYLE 1:

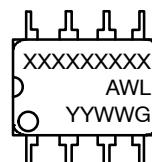
- PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.015	0.210	0.38	5.33
A1	0.015		0.38	
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005		0.13	
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB		0.430		10.92
L	0.115	0.150	2.92	3.81
M		10 ⁻³		10 ⁻³

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

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SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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