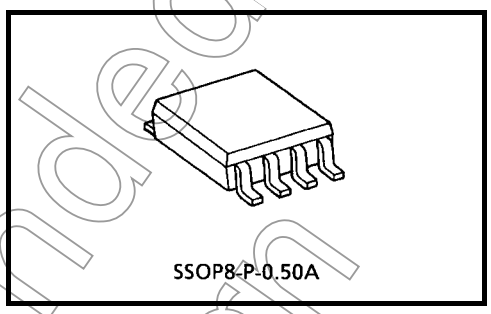
TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

TC9WMB1FK,TC9WMB2FK

TC9WMB1FK: 1024-Bit (128 × 8 Bit) 2-Wire Serial EEPROM

TC9WMB2FK: 2048-Bit (256 × 8 Bit) 2-Wire Serial EEPROM

The TC9WMB1FK and TC9WMB2FK are electrically erasable/programmable nonvolatile memory (EEPROM).

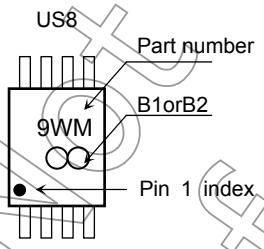


Weight: 0.01 g (typ.)

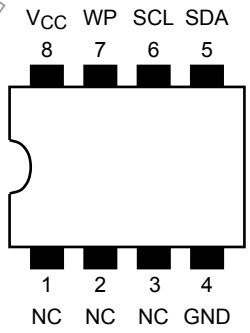
Features

- 2-wire serial interface (I^2C BUS)
- Single power supply
  Read: V_{CC} = 1.8 to 5.5 V
  Write: V_{CC} = 2.3 to 5.5 V
- Low power consumption: 5 μA (in standby state)
  : 0.5 mA (in read state)
- Operating frequency: 400 kHz (V_{CC} = 2.3 to 5.5 V)
- Byte write and page (8-byte) write
- Write protection
- Sequential read
- Write time: 10 ms (V_{CC} = 3.0 to 5.5 V)
  12 ms (V_{CC} = 2.3 to 2.7 V)
- Write endurance: 10^5 times
- Data retention: 10 years
- Wide operating temperature range: −40 to 85°C
- Package: US8

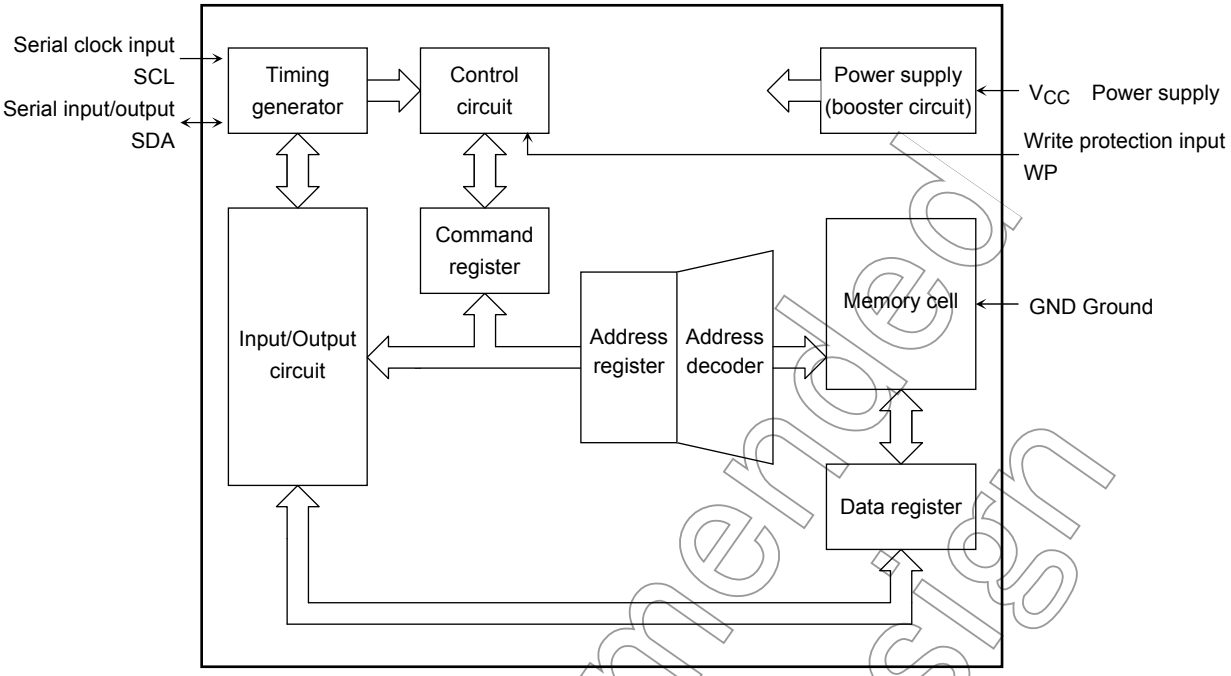
Product Marking



Pin Assignment (top view)



Block Diagram



Pin Function

Pin Name	Input/Output	Description
SCL	Input	Serial clock input Data is fetched on a rising edge of SCL. Data is output on a falling edge of SCL.
SDA	Input/output	Serial input/output This pin must be pulled up with a resistor because it is configured as an N-ch open-drain pin for output.
WP	Input	Write protection input A high on this input disables writing. A low on this input enables writing.
NC	—	No connection (not connected internally)
V_{CC}	Power supply	1.8 to 5.5 V (for reading) 2.3 to 5.5 V (for writing)
GND		0 V (GND)

Functional Description

1. Start and Stop Conditions

When SCL is high, pulling SDA low produces a start condition and pulling SDA high produces a stop condition. Every instruction is started when a start condition occurs and terminated when a stop condition occurs.

During a read, a stop condition causes the read to terminate and the chip to enter the standby state. During a write, a stop condition causes the fetching of write data to terminate, after which writing starts automatically. Upon the completion of writing, the chip enters the standby state.

Start conditions of five times or more cannot be generated from stop condition to the next stop condition.

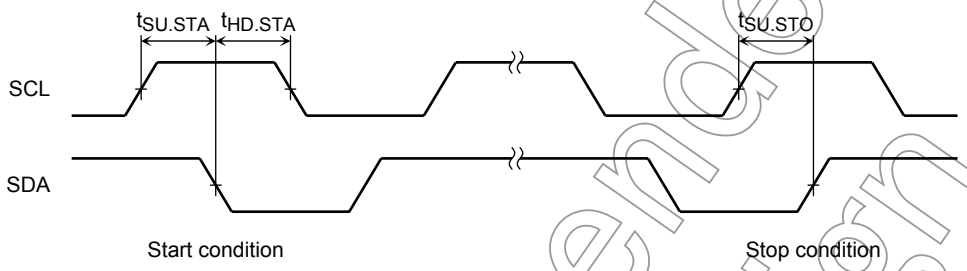


Figure 1

2. Modifying Data

Data on the SDA input can be modified while SCL is low. When SCL is high, modifying the SDA input means a start or stop condition.

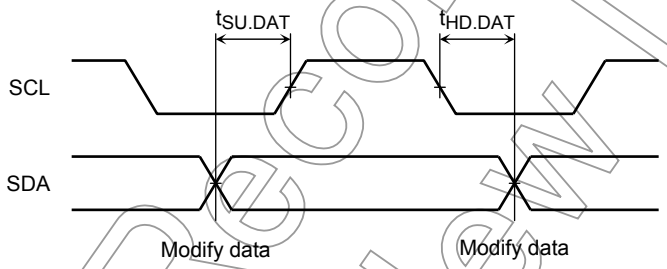


Figure 2

3. Acknowledge

Data is transmitted and received in 8-bit units. The receiver sends an acknowledge signal by outputting a low on SDA in the 9th clock cycle, indicating that it has received data normally. The transmitter releases the bus in the 9th clock cycle to receive an acknowledge signal.

During a write, the chip is always the receiver so that it outputs an acknowledge signal each time it has received eight bits of data.

During a read, the chip outputs an acknowledge signal after it receives an address following a start condition. Then, it outputs read data and releases the bus to wait for an acknowledge signal from the master. When it detects an acknowledge signal, it outputs data at the next address if it does not detect a stop condition. If the chip does not detect an acknowledge signal, it stops read operation, and enters the standby state when a stop condition occurs subsequently.

If the chip does not detect an acknowledge signal nor a stop condition, it keeps the bus released.

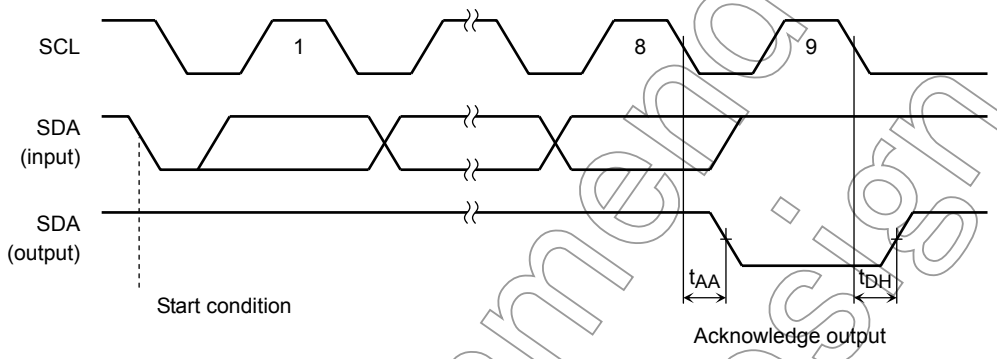


Figure 3

4. Device Addressing

After a start condition occurs, a 7-bit device address and a 1-bit read/write instruction code are input to the chip.

The upper four bits are called device code, which must always be “1010”. The next three bits are used to select a device on the bus. These three bits are not specified for this IC and can be set to any value.

The least significant bit (R/$\overline{W}$: READ/$\overline{WRITE}$) indicates a read instruction when set to 1 and a write instruction when set to 0.

An instruction is not executed if the device address does not match the specified value.

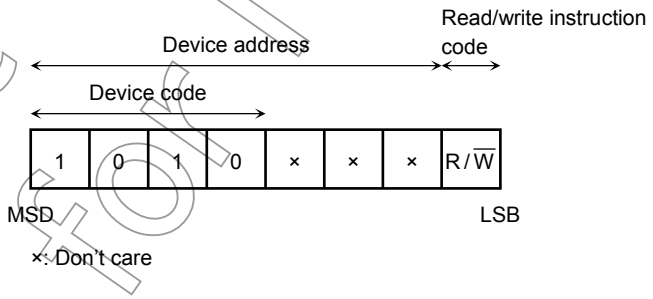


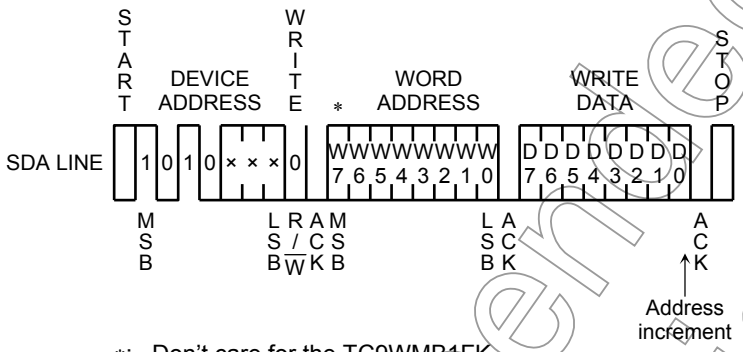
Figure 4

5. Write Operation

(1) Byte write

A byte write writes data to a specified address. After a start condition, input a device address, R/$\overline{W}$ (= 0), a word address, and write data.

When a stop condition is entered subsequently, write operation starts automatically, rewriting the data at the specified address with the input data. A next instruction cannot be accepted while write operation is in progress. Therefore, no acknowledge signal is returned. After writing the data, the chip automatically enters the standby state.



*: Don't care for the TC9WMB1FK

Figure 5

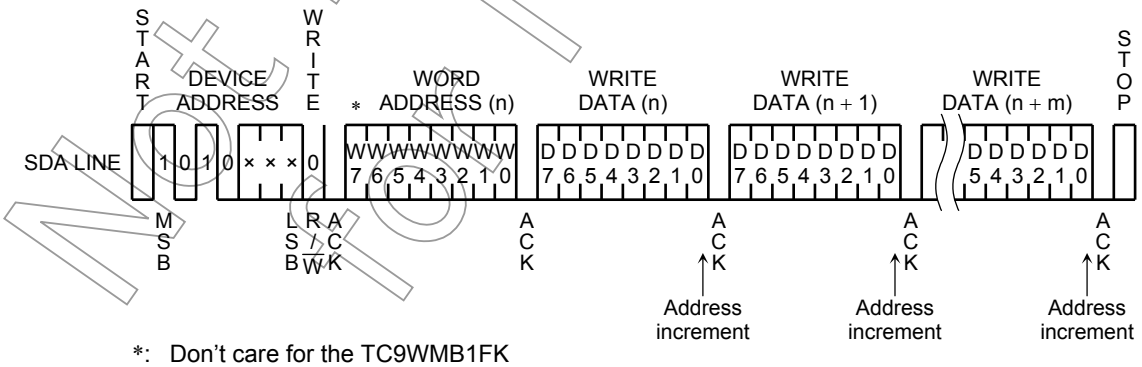
(2) Page write

A page write writes up to eight bytes of data collectively to a specified page. After a start condition, input a device address, R/$\overline{W}$ (= 0), a word address (n), and write data (n), in the same way as for a byte write. Then, input write data (n + 1) immediately without entering a stop condition, while checking that an acknowledge signal is asserted (0).

The upper four bits (W3 to W6) of the word address are fixed and the lower three bits (W0 to W2) are automatically incremented so that up to eight bytes of data can be input.

When the last address within the page is reached, the lower three bits (W0 to W2) of the word address are rolled over to the first address of the page. If more than eight bytes of write data are input, the last eight bytes are valid.

When a stop condition is entered subsequently, write operation starts automatically, rewriting the data at the specified addresses with the input data.



*: Don't care for the TC9WMB1FK

Figure 6

(3) Acknowledge polling

Acknowledge polling is a feature for determining whether rewrite operation is in progress. During rewrite operation, input a start condition, a device address, and $R/\overline{W}$ (= 0 or 1). The acknowledge feature does not output an acknowledge signal while rewrite operation is in progress. It outputs a low acknowledge signal if rewriting has already completed.

If the next instruction is a write, input a word address and write data subsequently. If the next instruction is a read, supply a stop condition and then start read operation.

(4) Write protection

Driving the write protection (WR) pin high causes the TC9WMB1FK to protect the entire memory area from being written and the TC9WMB2FK to protect the bottom half (80h to FFh) of the memory area from being written. Rewriting is allowed when the write protection pin is low. While a write is in progress, driving the WP pin high does not stop write operation.

Reading is always enabled regardless of whether the WP pin is high or low.

6. Read Operation

Read operation is performed in one of three modes: current address read, random read, and sequential read.

For reading, enter a device address and R/W (= 1) after a start condition. After read data is output, terminate read operation by inputting a high acknowledge signal (or releasing the bus without supplying an acknowledge signal) and then supplying a stop condition.

(1) Current address read

The internal address counter maintains the address that is next to the last accessed (read or written) word address (n). In current address read mode, data is read from address n + 1, as indicated by the address counter.

In current address read mode, entering a device address and R/W (= 1) after a start condition causes the chip to output a low acknowledge signal and then data at the address indicated by the internal address counter.

The address counter is incremented on a falling edge of the SCL pulse where the eighth bit is output. If the previous operation was reading data from the last address, the current address is rolled over to address 0. If the previous operation was writing data to the last address of the page, the address is rolled over to the first address of the page.

The current address is maintained in an internal register so that it is lost when the power is turned off. For the first read after power-up, specify an address by performing a random read.

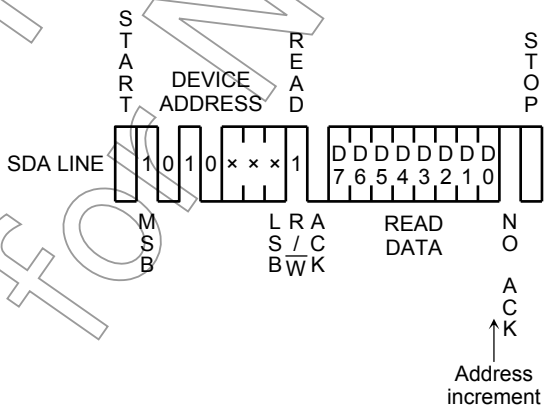


Figure 7

(2) Random read

A random read reads data at a specified address. A dummy write is necessary to specify an address.

In random read mode, enter a device address, R/W (= 0), and a word address after a start condition. Unlike a byte or page write, where write data is entered immediately, a dummy write only specifies a word address. Then, supply a start condition and enter a device address and R/W (= 1) in the same way as for a current address read, to read data from the specified address.

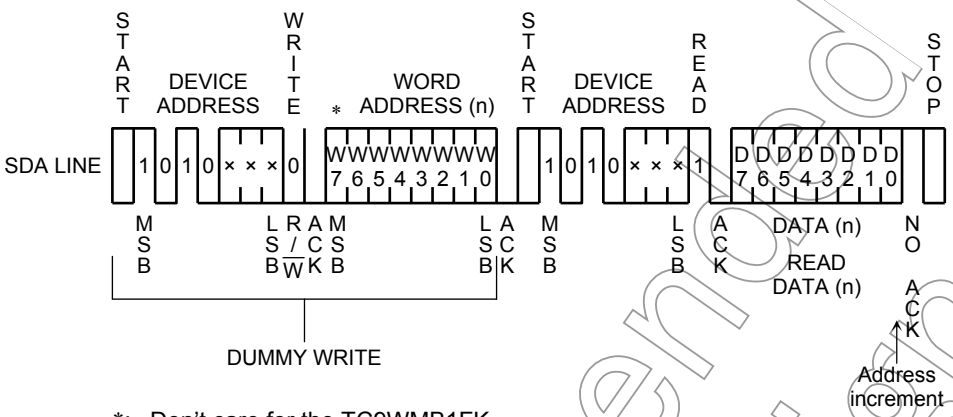


Figure 8

(3) Sequential read

A sequential read reads data sequentially from successive word addresses.

For either current address read or random read, upon receiving a start condition, a device address and R/W (= 1), an acknowledge (low) is placed on the SDA line, followed by the data at the address pointed to by the internal address counter. When an acknowledge (low) is then received, the word address is automatically incremented so that the next data is driven out.

After the last address is reached, the word address is rolled over to address 0.

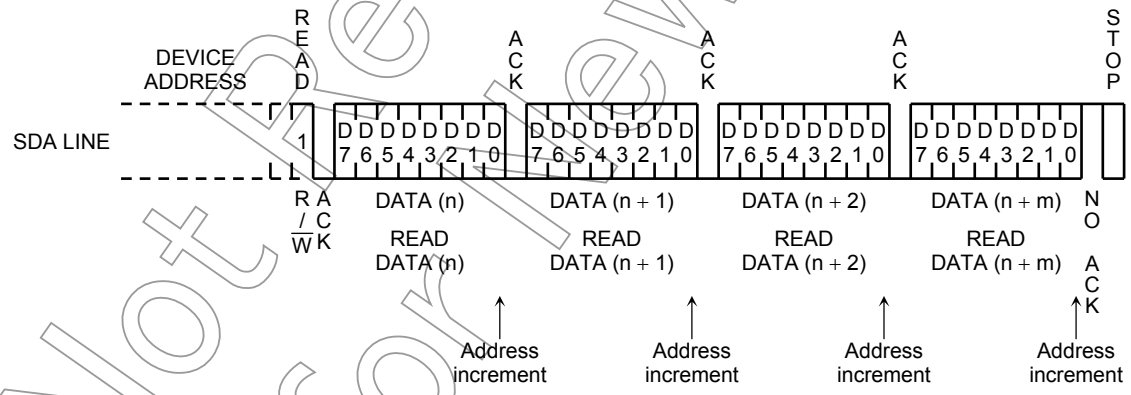


Figure 9

7. Notes on Use

(1) Powering up the chip

This IC contains a power-on clear circuit, which initializes the internal circuit of the IC when the power is turned on. If initialization fails, the chip may malfunction. When powering up the chip, observe the following precautions to assure that the clear circuit will operate normally:

(a) Pull SCL and SDA high.
(b) The power rising time (tR) must be 10 ms or less.
(c) After turning off the power, wait at least 100 ms (tOFF) before attempting to power up the chip again.
(d) The supply voltage must rise from a voltage lower than 0.1 V.
(e) After turning on the power, wait at least 10 ms before attempting to send an instruction to the chip.

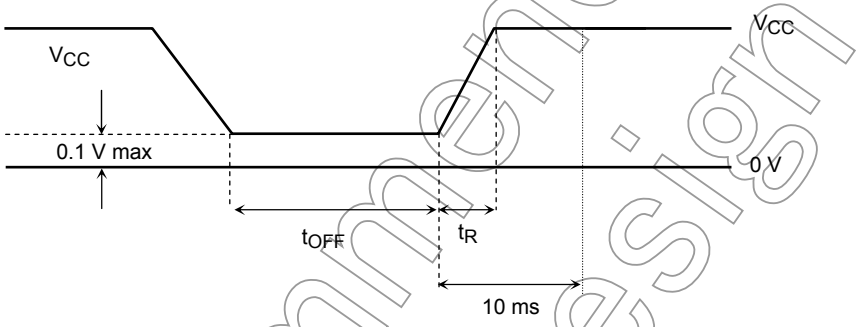


Figure 10

(2) Pulling up the SDA and SCL pins

This IC requires the SDA and SCL pins to be pulled up with an external resistor. The recommended pull-up resistance range is 1 kΩ to 10 kΩ.

(3) Noise elimination time for the SDA and SCL pins

This IC contains a low-pass filter for eliminating noise on the SDA and SCL pins. Its guaranteed value corresponds to the noise suppression time Ti, given in the AC characteristics table.

Absolute Maximum Ratings (Note) (GND = 0 V)

Characteristics	Symbol	Rating	Units
Supply voltage	V_{CC}	−0.3~7.0	V
Input voltage	V_{IN}	−0.3~V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3~V_{CC} + 0.3	V
Power dissipation	P_D	200 (25°C)	mW
Storage temperature	T_{stg}	−55~125	°C
Operating temperature	T_{opr}	−40~85	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note) (GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Max	Unit
Supply voltage (for reading)	V_{CC}	—	1.8	5.5	V
Supply voltage (for writing)	V_{CC}	—	2.3	5.5	V
High-level input voltage	V_{IH}	2.3 V ≤ V_{CC} ≤ 5.5 V	0.7 × V_{CC}	V_{CC}	V
		1.8 V ≤ V_{CC} < 2.3 V	0.8 × V_{CC}	V_{CC}	
Low-level input voltage	V_{IL}	2.3 V ≤ V_{CC} ≤ 5.5 V	0	0.3 × V_{CC}	V
		1.8 V ≤ V_{CC} < 2.3 V	0	0.2 × V_{CC}	
Operating frequency	f_{SCL}	2.3 V ≤ V_{CC} ≤ 5.5 V	0	400	kHz
		1.8 V ≤ V_{CC} < 2.3 V	0	100	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics (GND = 0 V, T_{opr} = −40 to 85°C)

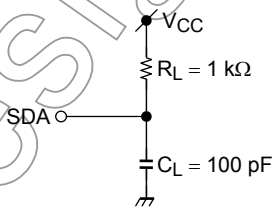
Characteristics	Symbol	Test Condition	1.8 ≤ V_{CC} < 2.3 V		2.3 ≤ V_{CC} ≤ 3.6 V		4.5 ≤ V_{CC} ≤ 5.5 V		Unit
			Min	Max	Min	Max	Min	Max	
Input current	I_{LI}	—	—	±1	—	±1	—	±1	μA
Output leakage current	I_{LO}	—	—	±1	—	±1	—	±1	μA
Low-level output voltage	V_{OL}	I_{OL} = 3.2 mA	—	—	—	0.4	—	0.4	V
		I_{OL} = 1.5 mA	—	0.5	—	—	—	—	
Quiescent supply current	I_{CC1}	—	—	5	—	5	—	5	μA
Supply current during read	I_{CC2}	f = 400 kHz	—	0.2*	—	0.3	—	0.5	mA
Supply current during write	I_{CC3}	f = 400 kHz	—	—	—	1.5	—	2.0	mA

*: f = 100 kHz

AC Characteristics (GND = 0 V, T_{opr} = −40 to 85°C)

Test Conditions

Input pulse voltage	0.1 × V_{CC}~0.9 × V_{CC}
Input rise/fall time	20 ns
Input/output testing voltage	0.5 × V_{CC}
Output load	100 pF + 1 kΩ pull-up resistor



Characteristics	Symbol	1.8 ≤ V_{CC} < 2.3 V		2.3 ≤ V_{CC} ≤ 3.6 V		4.5 ≤ V_{CC} ≤ 5.5 V		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	400	kHz
SCL clock “low” time	t_{LOW}	4.7	—	1.2	—	1.2	—	μs
SCL clock “high” time	t_{HIGH}	4.0	—	0.6	—	0.6	—	μs
Noise suppression time	t_I	—	100	—	50	—	50	ns
SDA output delay	t_{AA}	0.1	4.5	0.1	0.9	0.1	0.9	μs
Bus free time	t_{BUF}	4.7	—	1.2	—	1.2	—	μs
Start condition hold time	$t_{HD.STA}$	4.0	—	0.6	—	0.6	—	μs
Start condition setup time	$t_{SU.STA}$	4.7	—	0.6	—	0.6	—	μs
Data input hold time	$t_{HD.DAT}$	0	—	0	—	0	—	ns
Data input setup time	$t_{SU.DAT}$	250	—	200	—	200	—	ns
SCL, SDA input rise time	t_R	—	1.0	—	0.3	—	0.3	μs
SCL, SDA input fall time	t_F	—	0.3	—	0.3	—	0.3	μs
Stop condition setup time	$t_{SU.STO}$	4.7	—	0.6	—	0.6	—	μs
SDA output hold time	t_{DH}	100	—	50	—	50	—	ns

EEPROM Characteristics (GND = 0 V, 2.3 V ≤ V_{CC} ≤ 2.7 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Write time	t_{WR}	—	—	—	12	ms
Rewrite endurance	N_{EW}	—	1×10^5	—	—	Times
Data retention time	t_{RET}	—	10	—	—	Years

EEPROM Characteristics (GND = 0 V, 2.7 V < V_{CC} ≤ 5.5 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Write time	t_{WR}	—	—	—	10	ms
Rewrite endurance	N_{EW}	—	1×10^5	—	—	Times
Data retention time	t_{RET}	—	10	—	—	Years

Capacitance Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	5	4	pF
Output capacitance	C_O	—	5	3	pF

AC Characteristics Timing Charts

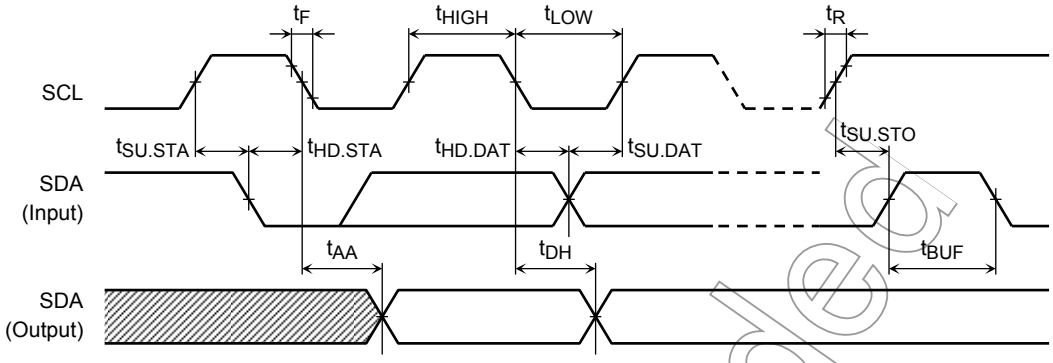


Figure 11 Bus Timing

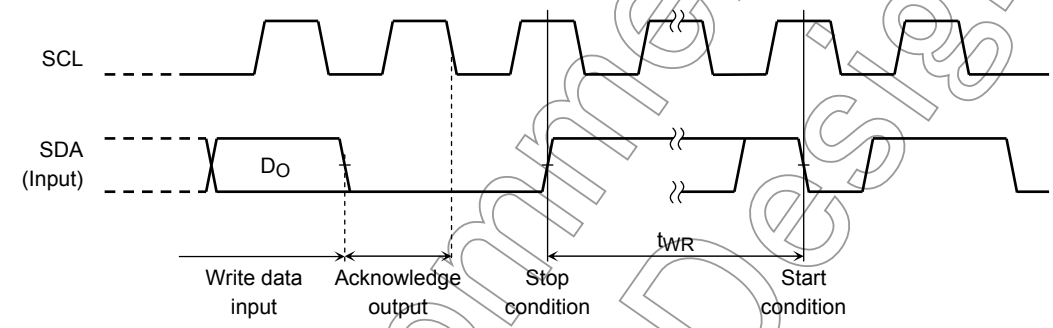
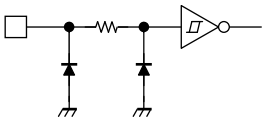
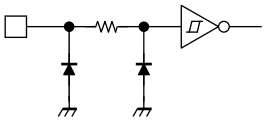
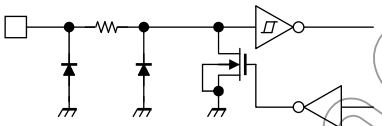


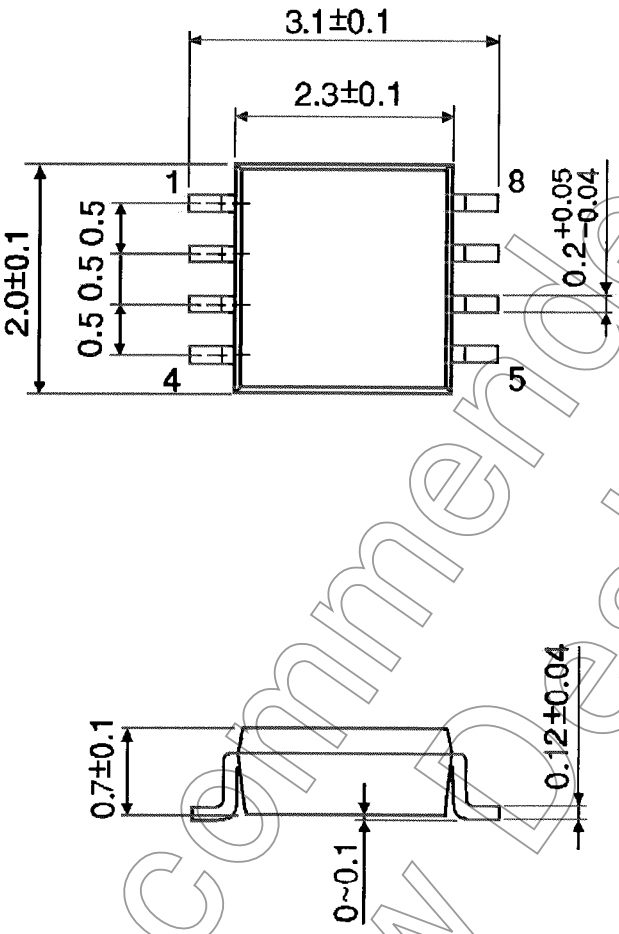
Figure 12 Write Cycle Timing

Input/Output Circuits of Pins

Pin	Type	Input/Output Circuit	Remarks
WP	Input		—
SCL	Input		—
SDA	Input/output		Open-drain output

Package Dimensions

SSOP8-P-0.50A Unit : mm



Weight: 0.01 g (typ.)

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