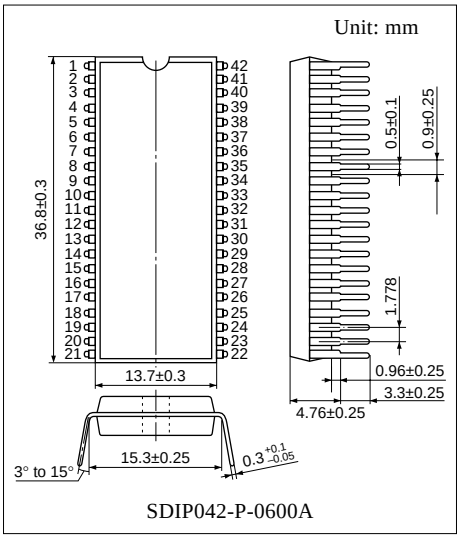
AN5491K

Synchronous signal and deflection distortion correction processing IC supporting I²C bus for HD, wide television



■ Overview

The AN5491K is a deflection processor IC for synchronous signal processing and screen distortion correction. It synchronizes with the input signal of High-vision, wide television, NTSC, PAL and VGA by the external binary input signal of them so that a multimedia television can be realized easily.

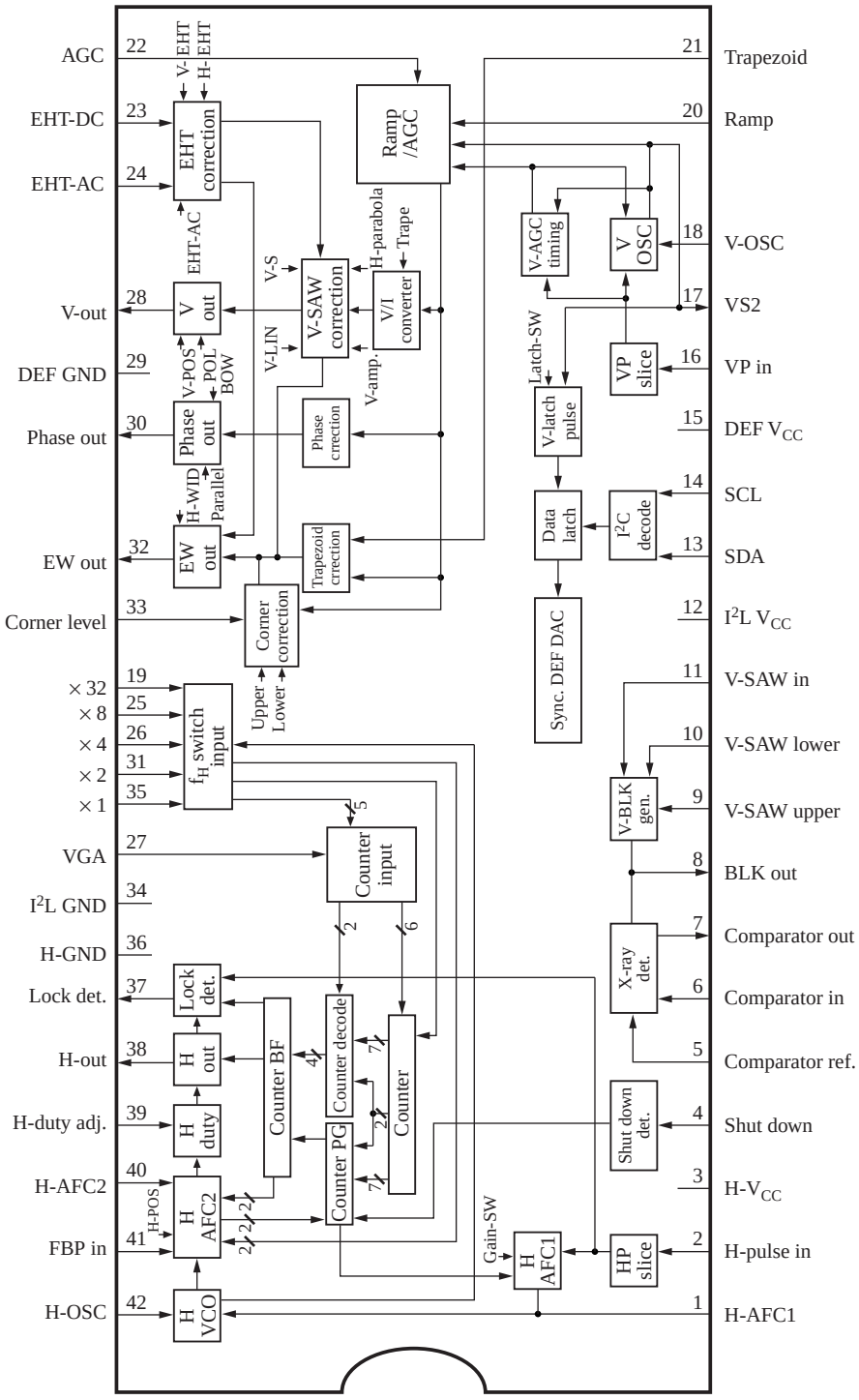
■ Features

- Supports the multiple-point horizontal frequency (15.7 kHz to 62.7 kHz)
- Horizontal duty is controllable by external voltage.
- Built-in full functions for correction (Horizontal and vertical: 16 items)
- Over-current detection, shut-down and hold-down

■ Applications

- High-vision televisions, Wide screen televisions and Projection televisions

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	H-AFC1	22	V-AGC
2	H-pulse input	23	EHT-DC input
3	H-V_{CC} (6.2 V)	24	EHT-AC input
4	Shut down SW	25	× 8
5	Comparator ref. (6.5 V)	26	× 4
6	Comparator	27	VGA
7	Comparator output	28	V-output
8	BLK output	29	DEF GND
9	V-SAW slice voltage (High)	30	Phase output
10	V-SAW slice voltage (Low)	31	× 2
11	V-SAW input	32	EW output
12	I^2L V_{CC} (5 V)	33	Corner slice voltage
13	I^2C SDA input	34	I^2L GND
14	I^2C SCL input	35	× 1
15	DEF V_{CC} (9 V)	36	H-GND
16	V-pulse input	37	Lock det.
17	V-pulse output	38	H-output
18	V-OSC	39	H-duty
19	× 32	40	H-AFC2
20	V-ramp	41	FBP input
21	Trapezoid correction voltage	42	H-OSC

■ Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
Supply voltage	V_{CC}	V_{CC1}	5.6	V
		V_{CC2}	10	
Supply current	I_{CC}	I_{CC1}	24	mA
		I_{CC2}	29	
		I_3	14	
Power dissipation *2	P_D	600		mW
Operating ambient temperature *1	T_{opr}	–20 to +70		°C
Storage temperature *1	T_{stg}	–55 to +150		°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

*2: The power dissipation shown is for the independent IC without a heat sink in free air at T_a = 70°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	4.5 to 5.0 to 5.5	V
	V_{CC2}	8.1 to 9.0 to 9.9	

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics						
Circuit current I_{CC1}	I_{12}	V_{CC1} = 5 V, V_{CC2} = 9 V	13.6	17.0	20.4	mA
Circuit current I_{CC2}	I_{15}	V_{CC1} = 5 V, V_{CC2} = 9 V	16.8	21.0	25.2	mA
Circuit current I_{CC3}	I_3	V_{CC1} = 5 V, V_{CC2} = 9 V, V_{CC3} = 6.5 V	6.0	7.5	9.0	mA
Synchronizing signal processing						
Horizontal free-running oscillation frequency 1 [Divide-by-8]	f_{HO8}	Pin 2: Without input, Pin 25: High Pins 19, 26, 31, 35: Low	61.5	62.7	63.9	kHz
Horizontal free-running oscillation frequency 2 [Divide-by-16]	f_{HO16}	Pin 2: Without input Pins 19, 25, 26, 31, 35: Low	30.8	31.4	32.0	kHz
Horizontal free-running oscillation frequency 3 [Divide-by-32]	f_{HO32}	Pin 2: Without input Pin 19: High	15.4	15.7	16.0	kHz
Horizontal output pulse duty cycle 1 [Divide-by-32]	τ_{HO1}	Pin 2: Without input, Pin 39: 2 V Pin 19: High	11.7	14.0	16.6	µs
Horizontal output pulse duty cycle 2 [Divide-by-32]	τ_{HO2}	Pin 2: Without input, Pin 39: 5 V Pin 19: High	23.9	28.5	33.7	µs
Horizontal high-level output voltage	V_{FHH}	DC voltage for pin 38 high-level	2.8	3.5	4.2	V
Horizontal low-level output voltage	V_{FHL}	DC voltage for pin 38 low-level	0	—	0.3	V
Horizontal output start voltage	V_{FHS}	Minimum voltage of pin 3 to become f > 10 kHz when horizontal oscillation output is 1 V[p-p] or more in divide-by-32 mode.	—	4.2	5.0	V
Screen center variable range 1 [Divide-by-16]	t_{DH16}	Pin 25: Low, Pins 19, 26, 31, 35: High Change amount of phase difference between H_P and H-out of Data 08: [00] to [1F]	2.16	2.70	3.24	µs
Screen center variable range 2 [Divide-by-32]	t_{DH32}	Pin 19: Low, Change amount of phase difference between H_P and H out of Data 08: [00] to [1F]	3.8	4.8	5.8	µs
Horizontal input pulse threshold voltage	V_{T2}	Slice level of pin 2	0.9	1.5	2.1	V
Over-voltage protective operation voltage	V_4	Pin 4 voltage at I_4 = 50 µA	0.60	0.75	0.90	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Deflection correction processing						
V_P pulse for OSD low-level	V_{LOSD}	V_{CC1} = 5 V, V_{CC2} = 9 V	0	—	0.4	V
V_P pulse for OSD high-level	V_{HOSD}	V_{CC1} = 5 V, V_{CC2} = 9 V	2.2	2.75	3.3	V
EHT-AC input pin voltage	V_{24}	Pin 24: Open	2.00	2.45	2.90	V
Vertical input signal threshold voltage	V_{TFV}	Pin 16: Input	0.9	1.5	2.1	V
Vertical free-running oscillation frequency	f_{VO}	Pin 16: Without input external R = 10 kΩ, C = 3.3 μF	35	44	53	Hz
Typical vertical output amplitude	V_V	V amplitude DAC: Typ.	0.88	1.10	1.32	V[p-p]
Typical EW output amplitude	V_{EW}	EW output amplitude for typical vertical output amplitude = 1.25 V[p-p]	0.8	1.0	1.2	V[p-p]
Phase out amplitude	V_{PHASE}	Side pin parallel, DAC: Typ.	– 0.1	0	0.1	V[p-p]
Ramp waveform amplitude	V_{RAMP}	f_V = 50 Hz to 120 Hz	2.15	2.45	2.75	V[p-p]
AGC input and output current	I_{AGC}		1.6	2.0	2.4	mA
Service SW: ON time Vertical output DC	V_{28SW}		3.1	3.5	3.9	V
BLK pulse high-level	V_{HBLK}		4.5	5.0	5.5	V
BLK pulse low-level	V_{LBLK}		0	—	0.4	V
Vertical output amplitude variable ratio (max.)	ΔV_{AMPmax}	V amplitude ratio between typ. → max.	+40	+50	+60	%
Vertical output amplitude variable ratio (min.)	ΔV_{AMPmin}	V amplitude ratio between typ. → max.	–40	–50	–60	%
Vertical output DC variable amount (min.)	$\Delta V_{SHIFTmin}$	Vertical DC: Typ. → min.	– 0.28	– 0.38	– 0.48	V
Vertical output DC variable amount (max.)	$\Delta V_{SHIFTmax}$	Vertical DC: Typ. → max.	+0.28	+0.38	+0.48	V
Vertical output trapezoidal waveform correction variable amount (min.)	$\Delta V_{TRAPmin}$	Trapezoidal waveform correction: Typ. → min.	– 0.28	– 0.38	– 0.48	V
Vertical output trapezoidal waveform correction variable amount (max.)	$\Delta V_{TRAPmin}$	Trapezoidal waveform correction: Typ. → max.	+0.28	+0.38	+0.48	V
External trapezoidal waveform center voltage	V_{21}		2.4	3.0	3.6	V
Vertical output center DC level	V_{28}		2.8	3.5	4.2	V
EW output (min.) to parabolic amplitude change	V_{EWmin}	Parabolic amplitude: Min.	– 0.1	0	0.1	V[p-p]
EW output (max.) to parabolic amplitude change	V_{EWmax}	Parabolic amplitude: Max.	1.4	1.8	2.2	V[p-p]
EW output (min.) (DC) to horizontal amplitude change	ΔV_{EWmin}	Horizontal amplitude: Min.	– 0.95	–1.15	–1.35	V
EW output (max.) (DC) to horizontal amplitude change	ΔV_{EWmax}	Horizontal amplitude: Max.	+0.95	+1.15	+1.35	V
EW output (bottom voltage) 1 to EHT-DC change	ΔV_{EDC1}	EHT-DC: 5.0 V → 3.8 V Horizontal EHT: Max. EHT-AC gain: Min.	+1.04	+1.30	+1.56	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Deflection correction processing (continued)						
EW output (bottom voltage) 2 to EHT-DC change	ΔV_{EDC2}	EHT-DC: 5.0 V → 6.2 V Horizontal EHT: Max. EHT-AC gain: Min.	−1.04	−1.30	−1.56	V
EW output (bottom voltage) 1 to EHT-AC change	ΔV_{EAC1}	EHT-AC: 2.35 V → 1.35 V Horizontal EHT: Max. EHT-AC gain: Max.	+0.25	+0.35	+0.45	V
EW output (bottom voltage) 2 to EHT-AC change	ΔV_{EAC2}	EHT-AC: 2.35 V → 3.35 V Horizontal EHT: Max. EHT-AC gain: Max.	− 0.25	− 0.35	− 0.45	V
EW output parabolic DC level	V_{32}	Typ.	2.2	2.7	3.4	V
Parallelogram correction fluctuation 1 (upper side)	ΔV_{UPH1}	Parallelogram correction: Typ. → min.	+0.16	+0.26	+0.36	V
Parallelogram correction fluctuation 2 (upper side)	ΔV_{UPH2}	Parallelogram correction: Typ. → max.	− 0.16	− 0.26	− 0.36	V
Parallelogram correction fluctuation 3 (lower side)	ΔV_{BPH1}	Parallelogram correction: Typ. → min.	− 0.25	− 0.35	− 0.45	V
Parallelogram correction fluctuation 4 (lower side)	ΔV_{BPH2}	Parallelogram correction: Typ. → max.	+0.16	+0.26	+0.36	V
Bow shape correction fluctuation 1 (upper side)	ΔV_{USD1}	Bow shape correction: Typ. → min.	− 0.24	− 0.34	− 0.44	V
Bow shape correction fluctuation 2 (upper side)	ΔV_{USD2}	Bow shape correction: Typ. → max.	+0.12	+0.22	+0.32	V
Bow shape correction fluctuation 3 (lower side)	ΔV_{BSD1}	Bow shape correction: Typ. → min.	− 0.17	− 0.27	− 0.37	V
Bow shape correction fluctuation 4 (lower side)	ΔV_{BSD2}	Bow shape correction: Typ. → max.	+0.12	+0.22	+0.32	V
I^2C interface						
SCL, SDA input threshold voltage	V_{TH}	V_{CC1} = 5 V	1.5	—	3.0	dB
Sink capacity at ACK	V_{ACK}	I = 3 mA in case of pull-up resistor 1.6 Ω	—	—	0.4	V
Maximum clock frequency	f_{SCL}		100	—	—	kHz

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics						
AGC pulse width	τ_{AGC}		—	95	—	µs
Ramp discharge current	I_{RAMP1}		3.6	—	—	mA
Ramp charge current 1	I_{RAMP2}	f = 120 Hz, Pin 4: 5.7 V	—	138	—	µA
Ramp charge current 2	I_{RAMP3}	f = 30 Hz, Pin 4: 7.5 V	—	32.9	—	µA

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics (continued)						
BLK output amplitude	V_{BLK}		4	5	6	V
Vertical output drive current	I_{28}		−2	—	—	mA
Vertical output amplitude fluctuation with supply voltage	$\frac{V_V}{\Delta V_{CC}}$	Difference of $V_{CCmax} - V_{CCmin}$	—	0.1	—	V
Vertical output DC fluctuation with supply voltage	$\frac{V_{28}}{\Delta V_{CC}}$	Difference of $V_{CCmax} - V_{CCmin}$	—	1.0	—	V
EW output amplitude fluctuation with supply voltage	$\frac{V_{EW}}{\Delta V_{CC}}$	Difference of $V_{CCmax} - V_{CCmin}$	—	0.1	—	V
EW output DC fluctuation with supply voltage	$\frac{V_{32}}{\Delta V_{CC}}$	Difference of $V_{CCmax} - V_{CCmin}$	—	1.0	—	V
Synchronizing signal processing						
Horizontal free-running oscillation frequency [Divide-by-15]	f_{HO15}	Pin 2: Without input, Pin 19: Low Pins 25, 26, 31, 35: High	32.9	33.5	34.1	kHz
Horizontal output pull-in range [Divide-by-8]	f_{HP8}	Pin 2: Without input, Pin 25: High Pins 19, 26, 31, 35: Low	±2 000	±2 600	—	Hz
Comparator detection operation voltage	V_6	Pin 6: Minimum voltage to become high, Pin 5: 6.2 V	5.7	6.3	6.9	V
Lock detection output voltage	V_{37}	V_{37} in horizontal AFC lock mode	5.7	6.3	6.9	V
Lock detection charge and discharge current	I_{LOCK}	DC measurement in divide-by-32	—	±0.8	—	mA
FBP (AFC2) slice level	V_{TFBP}	Minimum voltage of pin 41 at which AFC operates.	1.5	1.9	2.3	V
Horizontal AFC μ	μ	DC measurement in divide-by-32	—	37	—	μA/μs
Horizontal VCO β	β	Slant of β curve near f = 15.7 kHz	—	1.9	—	Hz/mV
FBP allowable range 1 [Divide-by-8]	t_{FBP8}	Time from H-out rise to FBP center	3	—	9	μs
FBP allowable range 2 [Divide-by-16]	t_{FBP16}	Time from H-out rise to FBP center	4	—	13	μs
FBP allowable range 3 [Divide-by-32]	t_{FBP32}	Time from H-out rise to FBP center	6	—	20	μs
AFC1 reference current 1	I_{AFC1}	Data 0C = "11" (D1, D0)	—	0.82	—	mA
AFC1 reference current 2	I_{AFC2}	Data 0C = "01" (D1, D0)	—	1.1	—	mA
AFC1 reference current 3	I_{AFC3}	Data 0C = "10" (D1, D0)	—	1.5	—	mA
AFC1 reference current 4	I_{AFC4}	Data 0C = "00" (D1, D0)	—	2.0	—	mA
Horizontal output pull-in range 1 [Divide-by-16]	f_{HP16}	Pin 2: Without input Pins 19, 25, 26, 31, 35: Low	±1 000	±1 300	—	Hz
Horizontal output pull-in range 2 [Divide-by-32]	f_{HP32}	Pin 2: Without input Pin 19: High	±500	±650	—	Hz

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Deflection correction processing						
Vertical output S-shape variable ratio 1	ΔV_{SC1}	Vertical S-shape: Ratio of min.→max.	—	−28	—	%
Vertical output S-shape variable ratio 2	ΔV_{SC2}	Vertical S-shape: Ratio of min.→ max. (Change of V-out 40% to 60% point)	—	1.5	—	%
Vertical output (upper side) linearity variable ratio 1	ΔV_{ULIN1}	Vertical linearity (upper side): Typ.→max.	—	+12	—	%
Vertical output (upper side) linearity variable ratio 2	ΔV_{ULIN2}	Vertical linearity (upper side): Typ.→min.	—	−10	—	%
Vertical output (lower side) linearity variable ratio 1	ΔV_{BLIN1}	Vertical linearity (lower side): Typ.→max.	—	+9	—	%
Vertical output (lower side) linearity variable ratio 2	ΔV_{BLIN2}	Vertical linearity (lower side): Typ.→min.	—	−11	—	%
Vertical output EHT-DC change 1	ΔV_{EDC1}	EHT-DC = 5.0 V → 3.8 V Vertical EHT: Max., EHT gain: Max.	—	−30	—	%
Vertical output EHT-DC change 2	ΔV_{EDC2}	EHT-DC = 5.0 V → 6.2 V Vertical EHT: Max., EHT gain: Max.	—	+25	—	%
Vertical output EHT-AC change 1	ΔV_{EAC1}	EHT-AC = 2.35 V → 1.35 V EHT: Max., EHT gain: Max.	—	−12	—	%
Vertical output EHT-AC change 2	ΔV_{EAC2}	EHT-AC = 2.35 V → 3.35 V EHT: Max., EHT gain: Max.	—	+12	—	%
EW output (min.) to trapezoidal waveform change	$\Delta V_{TRAPmin}$	Trapezoidal SW: On, Trapezoidal: Typ. → min.	—	−40	—	%
EW output (max.) to trapezoidal waveform change	$\Delta V_{TRAPmax}$	Trapezoidal SW: On, Trapezoidal: Typ. → max.	—	+40	—	%
EW output (min.) to upper corner trapezoidal waveform change	ΔV_{UCmin}	Upper corner: Typ. → min. Corner slice voltage: 1 V	—	−45	—	%
EW output (max.) to upper corner trapezoidal waveform change	ΔV_{UCmax}	Upper corner: Typ. → max. Corner slice voltage: 1 V	—	+45	—	%
EW output (min.) to lower corner trapezoidal waveform change	ΔV_{BCmin}	Lower corner: Typ. → min. Corner slice voltage: 1 V	—	−45	—	%
EW output (max.) to lower corner trapezoidal waveform change	ΔV_{BCmax}	Lower corner: Typ. → max. Corner slice voltage: 1 V	—	+45	—	%
External trapezoidal waveform correction fluctuation 1 (Parabolic amplitude)	ΔV_{ETR1}	External trapezoidal correction: 3 V → 2 V	—	−40	—	%
External trapezoidal waveform correction fluctuation 2 (Parabolic amplitude)	ΔV_{ETR2}	External trapezoidal correction: 3 V → 4 V	—	+40	—	%

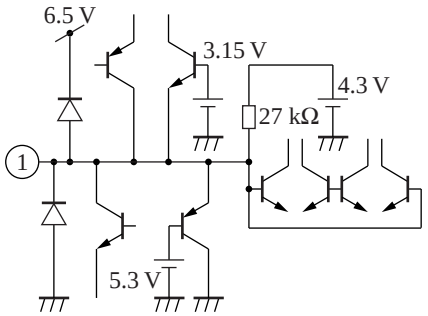
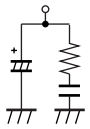
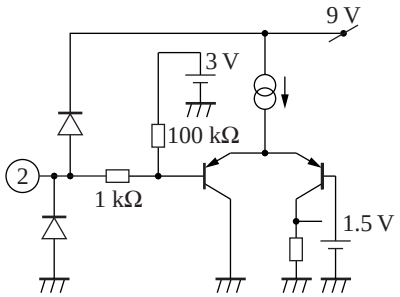
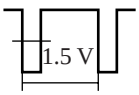
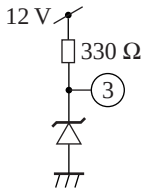
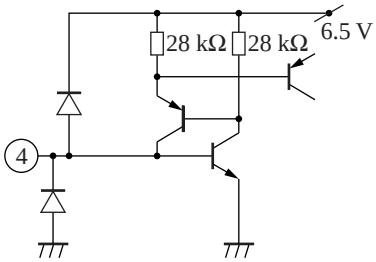
■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

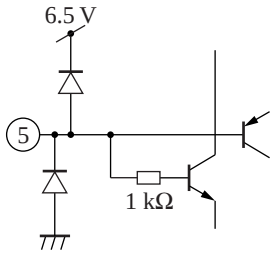
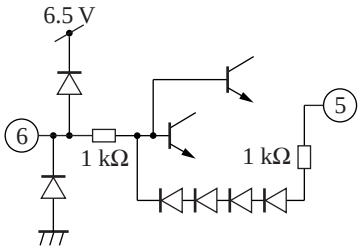
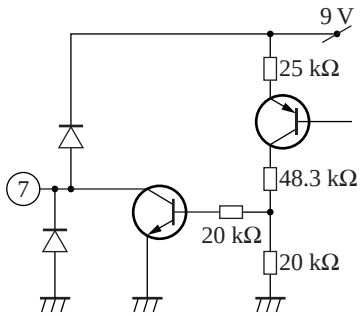
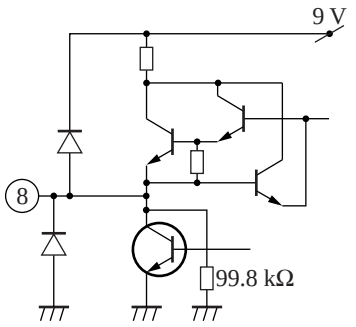
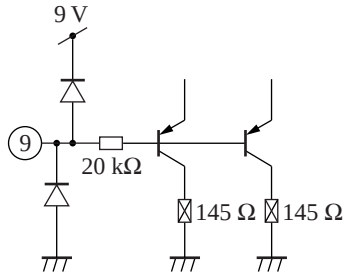
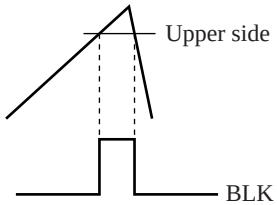
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C interface						
3, 4, 5, 6-bit DAC DNLE	L1	1LSB = {Data(max.) – Data(00)}/7,15,31,63	0.1	1.0	1.9	LSB/step
7-bit DAC DNLE (Except for 40)	L2	1LSB = {Data(max.) – Data(00)}/127	0.1	1.0	1.9	LSB/step
7-bit DAC DNLE (40 only)	L3	1LSB = {Data(max.) – Data(00)}/127	–1.0	1.0	2.0	LSB/step

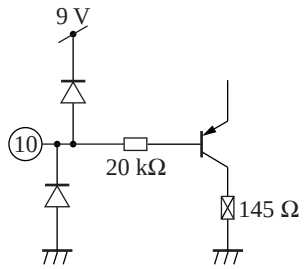
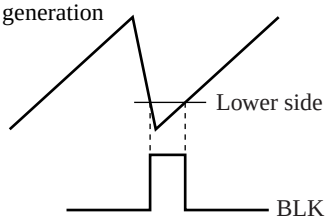
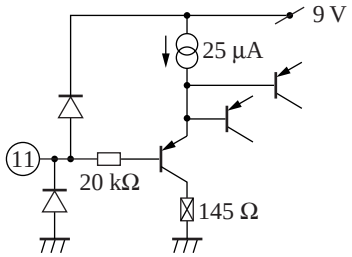
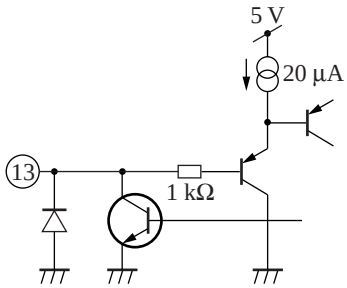
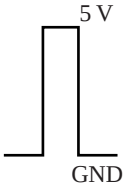
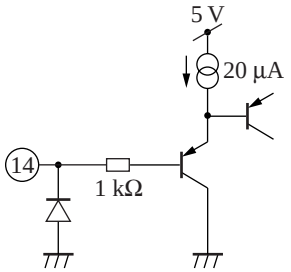
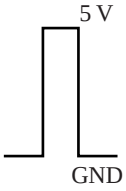
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage
1		AFC1: Horizontal frequency detection pin • Pin for adjusting the frequency of horizontal input pulse and the internal reference pulse. • Connect a lag lead filter. 	 DC approx. 4.3 V
2		H-pulse in: Horizontal synchronizing signal input pin • Polarity is as shown in the right figure (Negative). • Slice level is 1.5 V. • Input polarity is one polarity only (not corresponding to both polarities).	AC 
3		V_{CC}: Horizontal system power supply (6.5 V) pin • Connect an external zener	DC 6.5 V
4		Shut down: Control pin for shut-down • Horizontal output stops (GND) if a voltage 1 V_{BE} and over (more than approx. 0.75 V) is applied to the pin.	DC Normal: GND

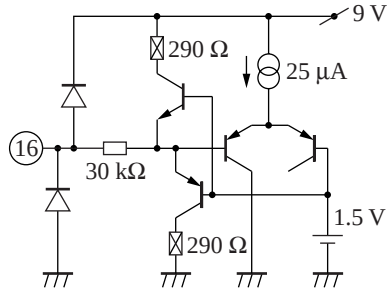
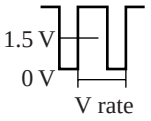
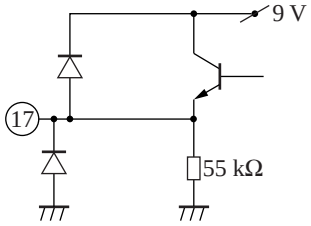
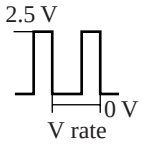
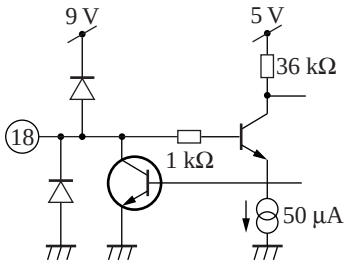
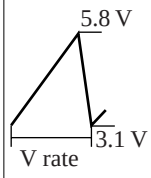
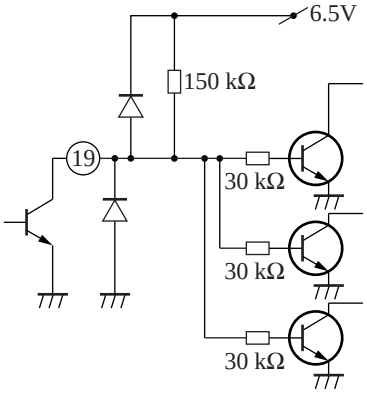
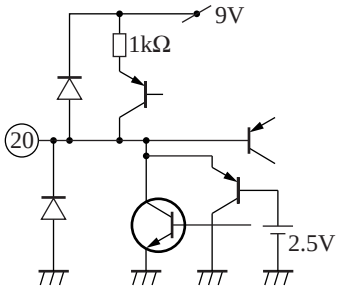
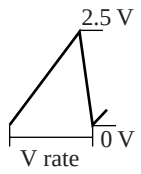
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
5		Comparator ref.: Reference voltage input pin for comparator • Attach zener diode externally (approx. 6.2 V) (Usable as reference voltage for hold-down)	DC
6		Comparator: Input pin for comparator detection • (Usable as pin for hold-down detection)	DC
7		Comparator out: Comparator detection output pin • Connect pull-up resistors outside the IC. (usable as hold-down control pin) Note) Use under 400 μA or less.	DC Normally: High
8		BLK out: Blanking pulse output pin • Normally: Low At BLK: High (5 V)	DC At BLK: High
9		Upper side slice: Upper side slice voltage input pin for BLK pulse generation 	DC

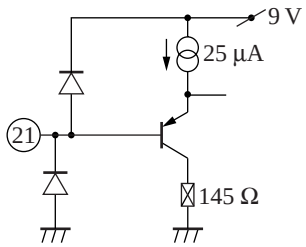
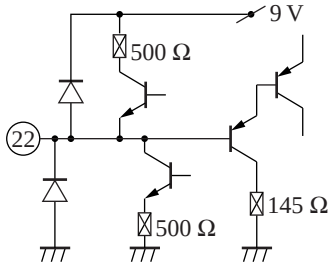
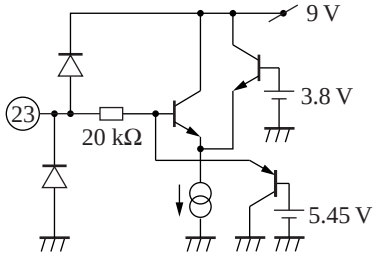
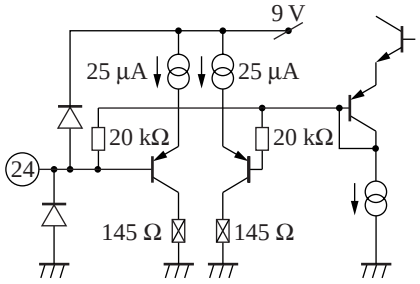
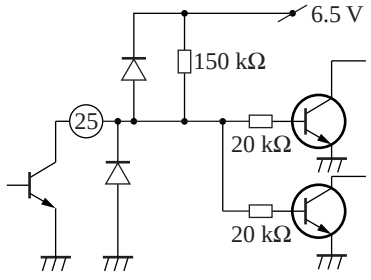
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
10		Lower side slice: Lower side slice voltage input pin for BLK Pulse generation 	DC
11		V-SAW in: V-SAW input pin for BLK pulse generation	AC 
12	—	V_{CC}: Power supply (5 V) pin for DAC/I^2L • Connect a pass capacitor (0.01 µF) between pin 12 and GND (pin 19).	DC 5 V
13		SDA: I^2C data input pin	
14		SCL: I^2C clock input pin	
15	—	V_{CC}: Pin for deflection system power supply (9 V) • Connect a pass capacitor between the pin and GND.	DC 9 V

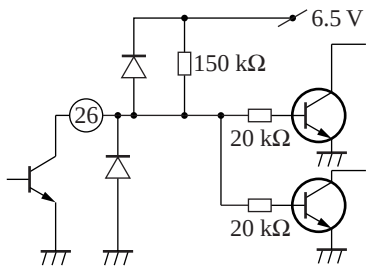
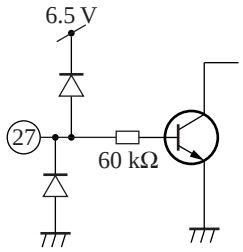
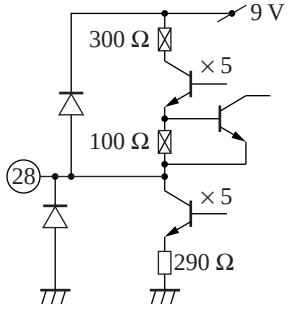
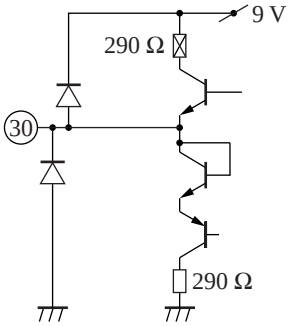
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
16		V-pulse in: Vertical sync. signal input pin • Polarity is as shown in the right figure (Negative) • Slice level is 1.5 V. • Input polarity is only one polarity (Not correspond to both polarities)	AC (Pulse) 
17		V-pulse out: Vertical sync. signal output pin • If vertical sync. signal input is present: Outputs the pulse synchronized with input V. Not present: Outputs free-running V pulse. (Usable for microcomputer OSD control)	AC (Pulse) 
18		V-OSC: Vertical oscillation pin • Connect CR. • Free-running oscillation when there is no input.	AC 
19		× 32: Horizontal free-running oscillation frequency control pin • To be used by high/low control. • Input is controlled by open collector output.	DC
20		V-ramp pin: • The pin for generating reference V sawtooth waveform for IC inside. • Connect an 0.22 µF mylar capacitor.	AC 

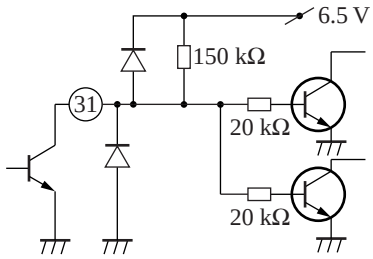
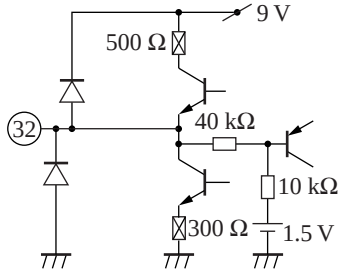
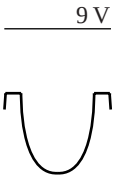
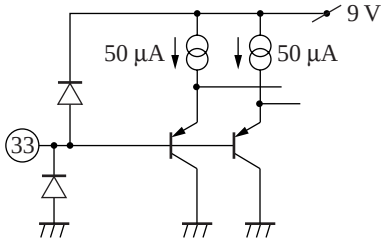
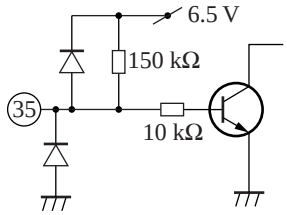
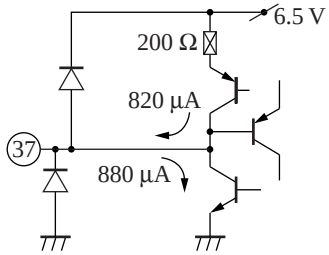
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
21		External trapezoidal waveform: The pin for controlling trapezoidal waveform compensation from outside. • Used by linking to V-position shift (at AC coupling). typ. 3.0 V	DC 2 V to 4 V
22		V-AGC: Vertical AGC pin • AGC pin to make a vertical output amplitude constant. • Connect 3.3 µF tantalum capacitor.	DC
23		EHT-DC: Pin for extremely high-tension compensation (EHT) • DC-coupled to pin.	DC Operating range: 3.8 V to 6.2 V
24		EHT-AC Pin for extremely high-tension compensation • AC-coupled to pin.	AC 2.35 V in an open mode Operating range: 1.35 V to 3.35 V
25		× 8: Horizontal free-running oscillation frequency control pin • To be used by high/low control. • Input is controlled by open collector output.	DC

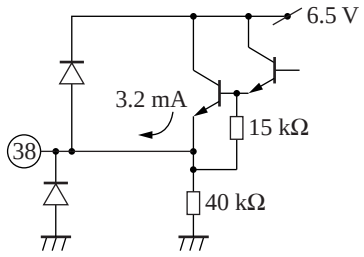
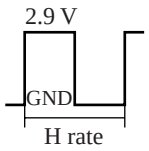
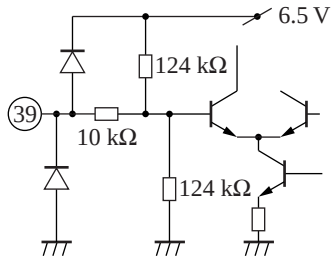
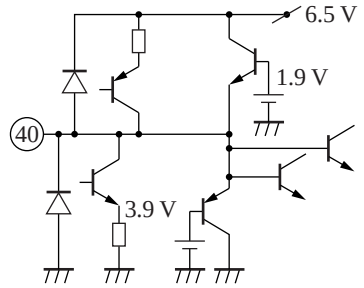
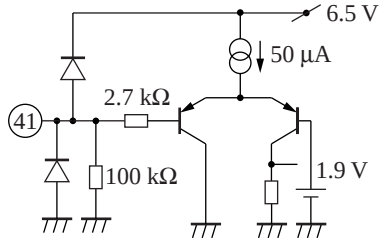
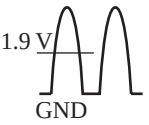
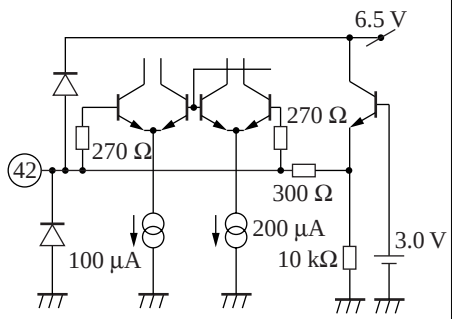
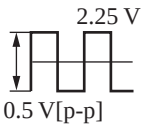
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
26		× 4: Horizontal free-running oscillation frequency control pin • To be used by high/low control. • Input is controlled by open collector output.	DC
27		V-FB: Forced progressive mode pin • To be used by high/low control. • At high: Multi-point mode At low: Progressive mode	DC
28		V-out: V sawtooth waveform output pin • Typ. 1.25 V[p-p]	AC 
29	—	GND: GND pin for deflection-system circuit (9 V)	DC GND
30		Phase out: Pin for side pin (Bow shape) correction, parallelogram correction and control pulse output. • Connect to H-AFC2 pin via 1 µF (non-polarity) capacitor.	AC DC approx. 3.7 V  Max. 300 mV[p-p]

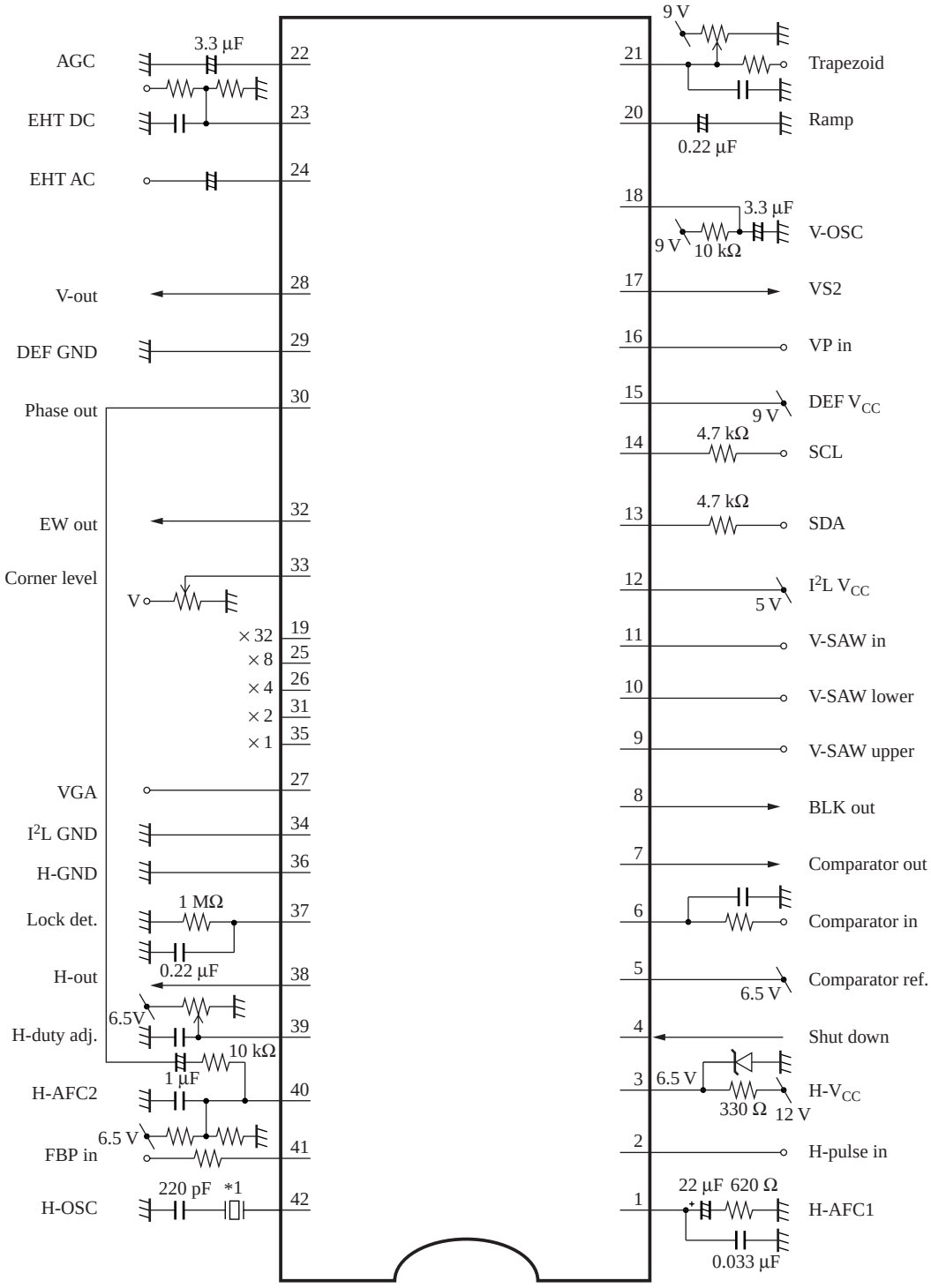
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
31		× 2: Horizontal free-running oscillation frequency control pin • To be used by high/low control. • Input is controlled by open collector output.	DC
32		EW out: Parabolic waveform output pin	AC 
33		Corner slice: The voltage to set a slice point of upper and lower corner correction. • The correction gain can be controlled independently by I²C bus for upper and lower, respectively.	DC Externally set at 0 VDC to 1.25 VDC
34		GND: GND pin for 5 V system (I²C/I²L)	DC GND
35		× 1: Horizontal free-running oscillation frequency control pin • To be used by high/low control.	DC
36	—	GND: GND pin for 6.5 V system (Horizontal system)	DC GND
37		Lock det.: Horizontal lock detection pin • Connect 0.022 µF and 1 MΩ between the pin and GND.	DC At lock mode: 6 V At unlocked mode: GND

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
38		H-out: Horizontal output pin • The length of high-period can be adjusted by a separate pin.	AC 
39		H-duty: Pin for controlling the length of high-period of horizontal output pulse. • Apply DC voltage from the outside.	DC 1 V to 5 V
40		AFC2: Horizontal phase detection pin • Pin for controlling phase difference between horizontal output pulse and FBP. • Phase out waveform is also connected to this pin via capacitor. • Connect 0.015 µF between this pin and GND.	DC 1.5 V to 4.5 V
41		FBP input pin: • Slices at 1.9 V (in the IC) and then uses as AFC2 control pulse. • Do not input any signal under GND inside the IC.	AC 
42		H-OSC: Reference oscillation pin (500 kHz) • Connect CERALOCK (CSB500F48), and temperature guaranteed (N750) 220 pF capacitor in series between this pin and GND.	AC 

■ Application Circuit Example



*1: Horizontal oscillator
TAFCSB500F48
[Murata Manufacturing Co. Ltd.]