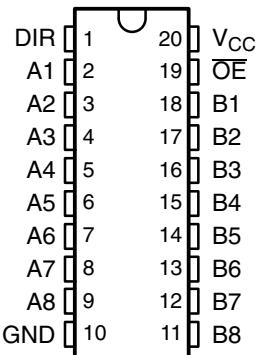
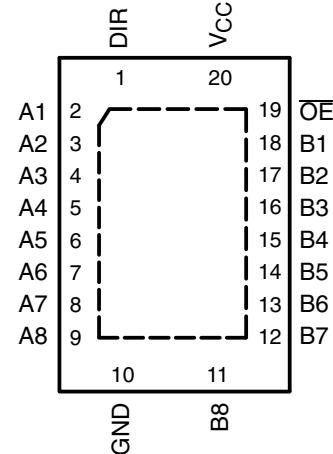


- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



## description/ordering information

This octal bus transceiver is designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT245B is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so the buses are effectively isolated.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ\text{C}$ to $85^\circ\text{C}$	QFN – RGY	Tape and reel	SN74LVT245BRGYR
	SOIC – DW	Tube	SN74LVT245BDW
		Tape and reel	SN74LVT245BDWR
	SOP – NS	Tape and reel	SN74LVT245BNSR
	SSOP – DB	Tape and reel	SN74LVT245BDBR
	TSSOP – PW	Tube	SN74LVT245BPW
		Tape and reel	SN74LVT245BPWR
	VFBGA – GQN	Tape and reel	SN74LVT245BGQNR
	VFBGA – ZQN (Pb-free)		SN74LVT245BZQNR

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



# SN74LVT245B

## 3.3-V ABT OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

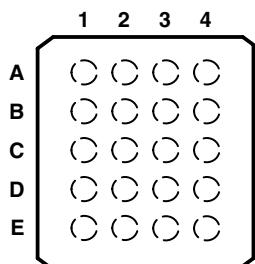
SCES004H – JANUARY 1995 – REVISED SEPTEMBER 2003

### description/ordering information (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQN OR ZQN PACKAGE  
(TOP VIEW)**



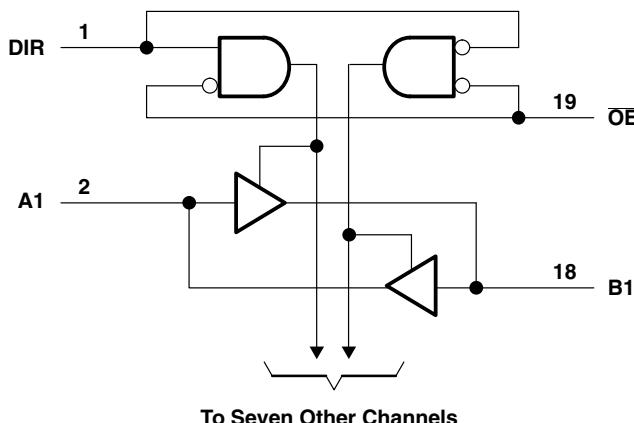
**terminal assignments**

	1	2	3	4
A	A1	DIR	$V_{CC}$	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

**FUNCTION TABLE**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### logic diagram (positive logic)



Pin numbers shown are for the DB, DW, NS, PW, and RGY packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**<sup>†</sup>

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JEDEC 51-7.  
 4. The package thermal impedance is calculated in accordance with JEDEC 51-5.

### **recommended operating conditions (see Note 5)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage		5.5	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200	$\mu$ s/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74LVT245B**  
**3.3-V ABT OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCES004H – JANUARY 1995 – REVISED SEPTEMBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT	
$V_{IK}$		$V_{CC} = 2.7 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2	V	
$V_{OH}$		$V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			V	
		$V_{CC} = 2.7 \text{ V}$ , $I_{OH} = -8 \text{ mA}$	2.4				
		$V_{CC} = 3 \text{ V}$ , $I_{OH} = -32 \text{ mA}$	2				
$V_{OL}$		$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$	0.2		V	
			$I_{OL} = 24 \text{ mA}$	0.5			
		$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$	0.4			
			$I_{OL} = 32 \text{ mA}$	0.5			
			$I_{OL} = 64 \text{ mA}$	0.55			
$I_I$	Control inputs	$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$		$\mu\text{A}$	
		$V_{CC} = 0$ or $3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$		10			
	A or B ports <sup>‡</sup>	$V_{CC} = 3.6 \text{ V}$	$V_I = 5.5 \text{ V}$	20			
			$V_I = V_{CC}$	1			
			$V_I = 0$	-5			
$I_{off}$		$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5 \text{ V}$		$\pm 100$		$\mu\text{A}$	
$I_{OZH}$		$V_{CC} = 3.6 \text{ V}$ , $V_O = 3 \text{ V}$		5		$\mu\text{A}$	
$I_{OZL}$		$V_{CC} = 3.6 \text{ V}$ , $V_O = 0.5 \text{ V}$		-5		$\mu\text{A}$	
$I_{OZPU}$		$V_{CC} = 0$ to $1.5 \text{ V}$ , $V_O = 0.5 \text{ V}$ to $3 \text{ V}$ , $\overline{OE}$ = don't care		$\pm 100$		$\mu\text{A}$	
$I_{OZPD}$		$V_{CC} = 1.5 \text{ V}$ to $0$ , $V_O = 0.5 \text{ V}$ to $3 \text{ V}$ , $\overline{OE}$ = don't care		$\pm 100$		$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high	0.19		$\text{mA}$	
			Outputs low	5			
			Outputs disabled	0.19			
$\Delta I_{CC}^§$		$V_{CC} = 3 \text{ V}$ to $3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND		0.2		$\text{mA}$	
$C_i$		$V_I = 3 \text{ V}$ or $0$		4		$\text{pF}$	
$C_{io}$		$V_O = 3 \text{ V}$ or $0$		9		$\text{pF}$	

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> Unused terminals are at  $V_{CC}$  or GND.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than  $V_{CC}$  or GND.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

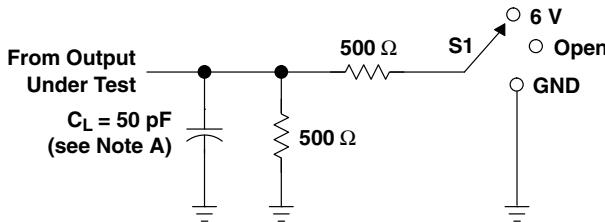
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$			UNIT
			MIN	TYP <sup>†</sup>	MAX	
$t_{PLH}$	A or B	B or A	1.2	2.3	3.5	ns
			1.2	2.1	3.5	
$t_{PZH}$	$\overline{OE}$	A or B	1.3	3.2	5.5	ns
			1.7	3.4	5.5	
$t_{PZL}$	$\overline{OE}$	A or B	2.2	3.5	5.9	ns
			2.2	3.4	5	
$t_{PHZ}$	$\overline{OE}$	A or B	2.2	3.5	5.9	ns
			2.2	3.4	5	

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



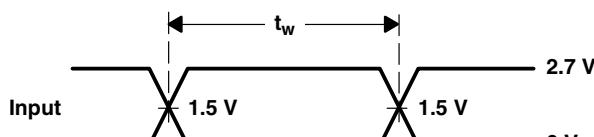
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND

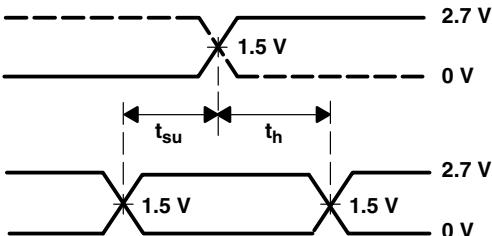
LOAD CIRCUIT



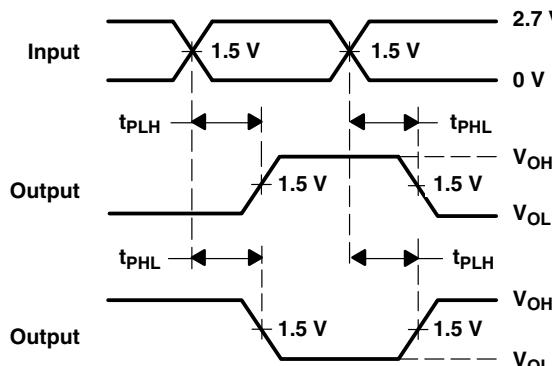
VOLTAGE WAVEFORMS  
PULSE DURATION



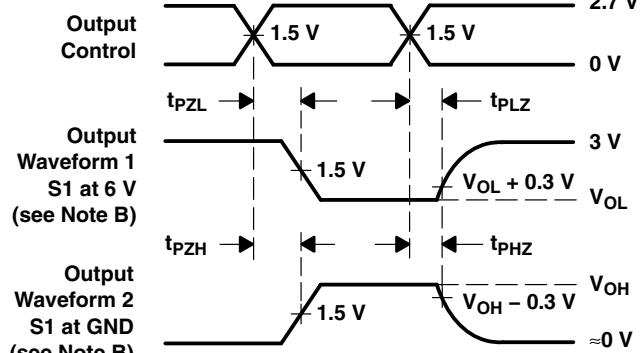
Data Input



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- The outputs are measured one at a time with one transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVT245BDBLE	OBsolete	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVT245BDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BPWLE	OBsolete	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVT245BPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVT245BRGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LX245B	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

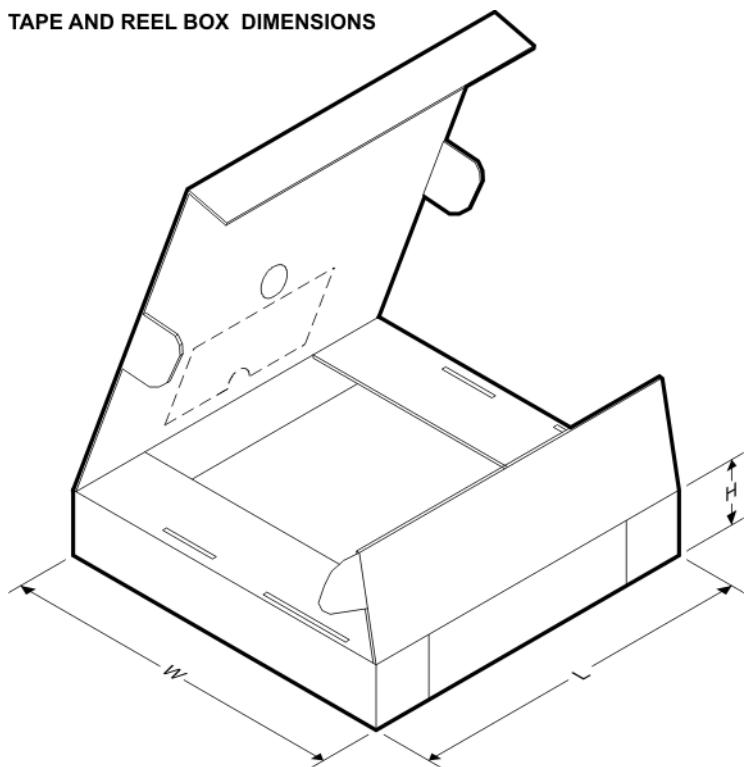
**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT245BDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVT245BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVT245BNSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVT245BPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVT245BRGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

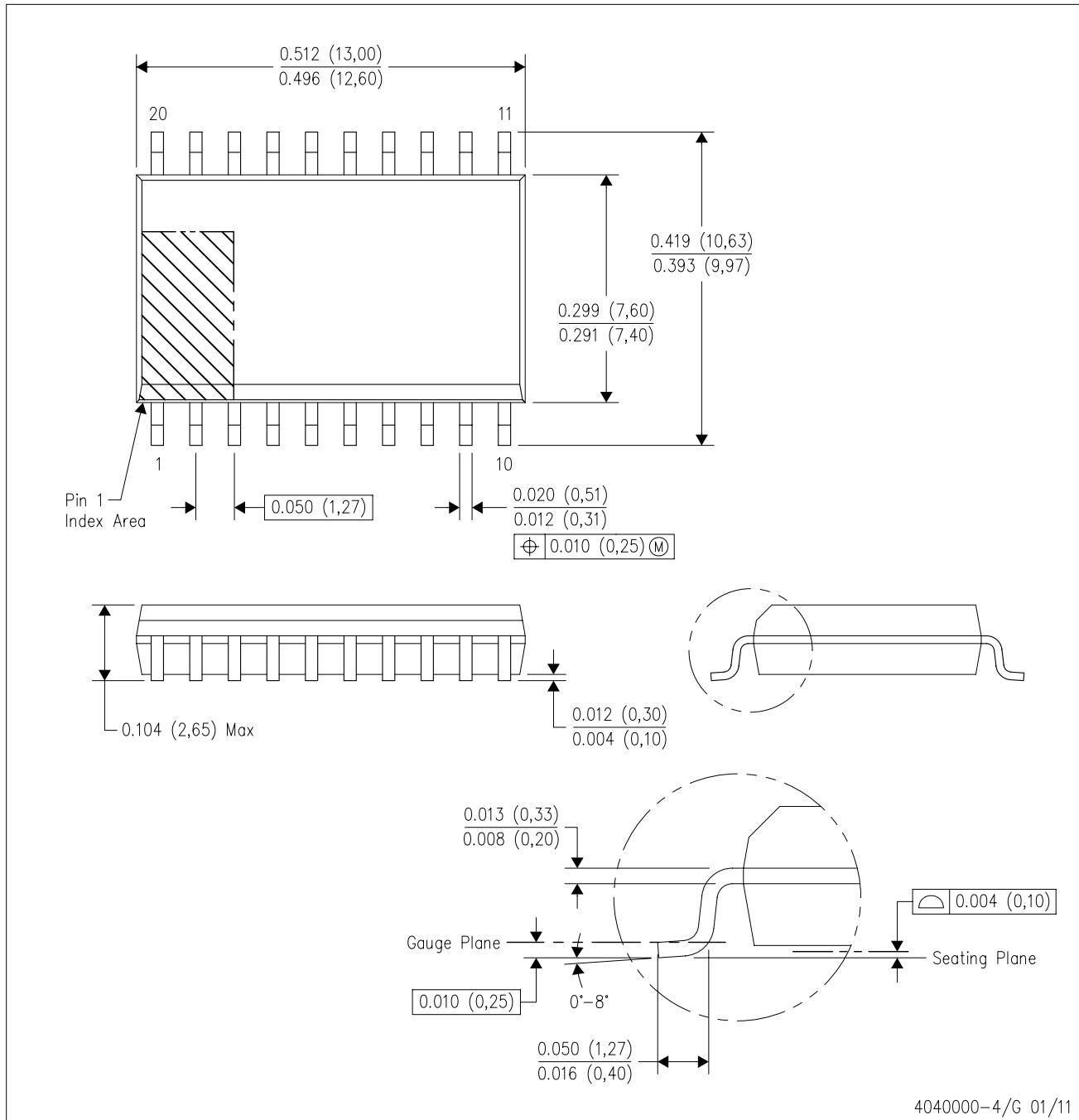
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT245BDBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVT245BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVT245BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVT245BPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVT245BRGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

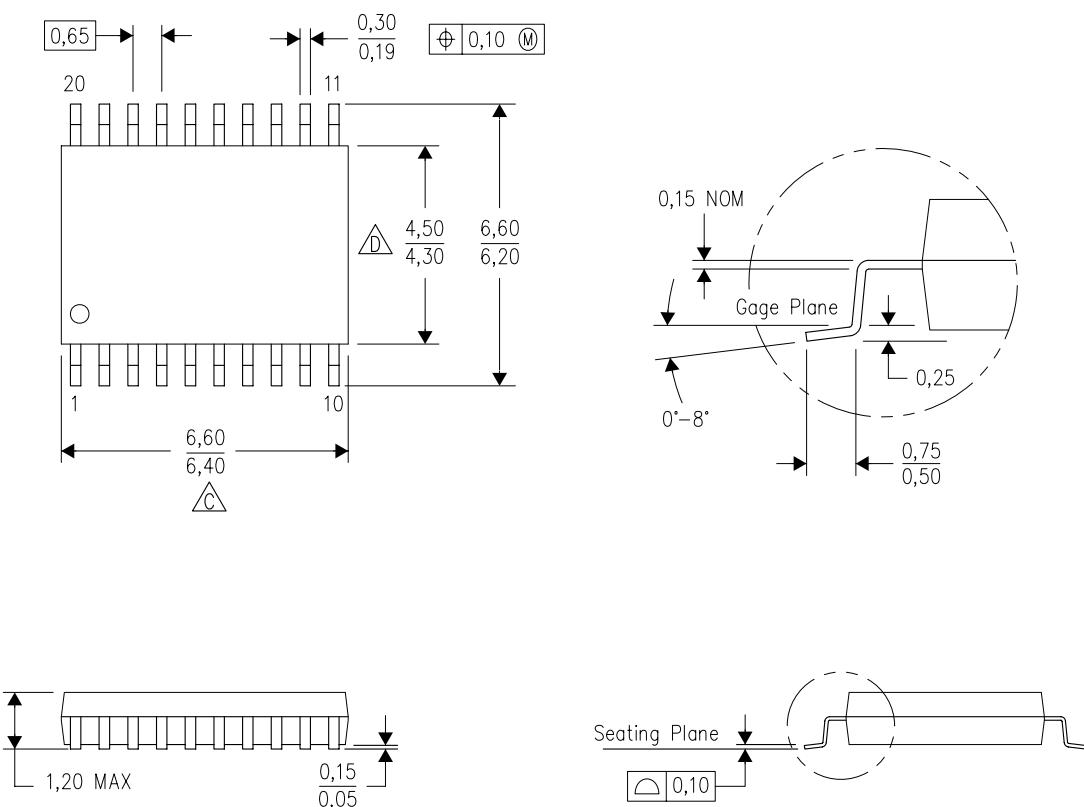


NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

**D** Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

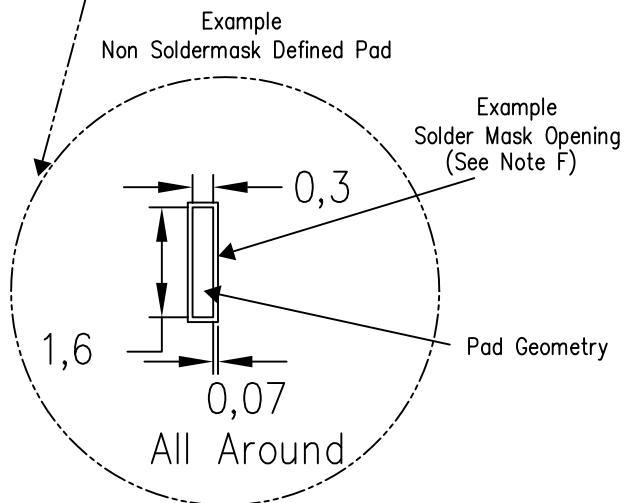
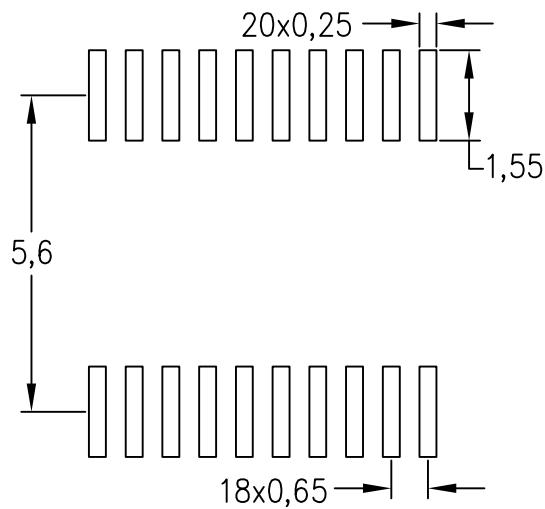
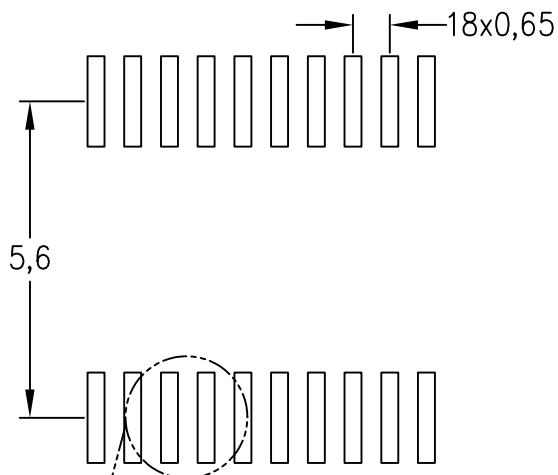
E. Falls within JFDEC M0-153

## PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/F 12/12

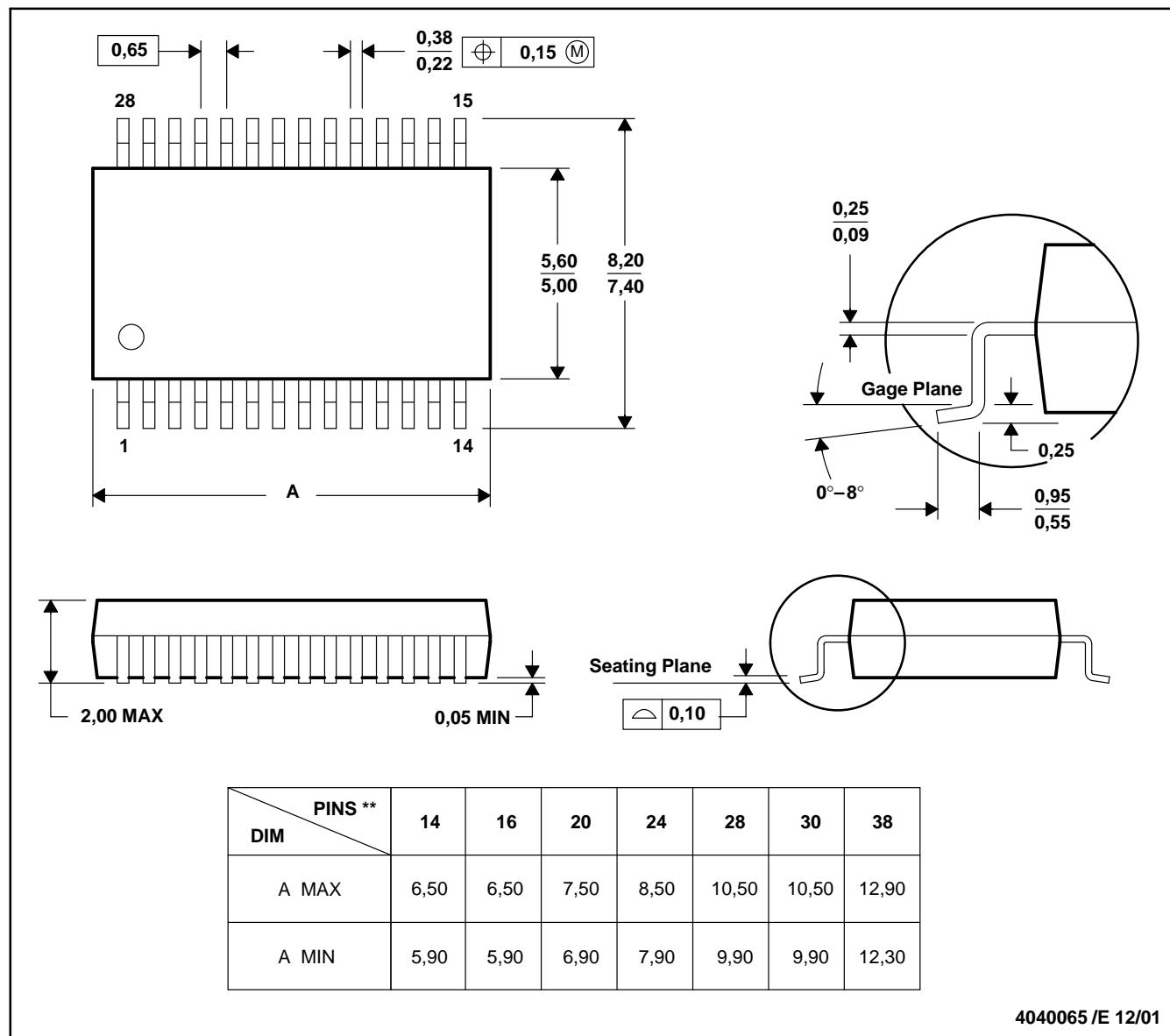
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

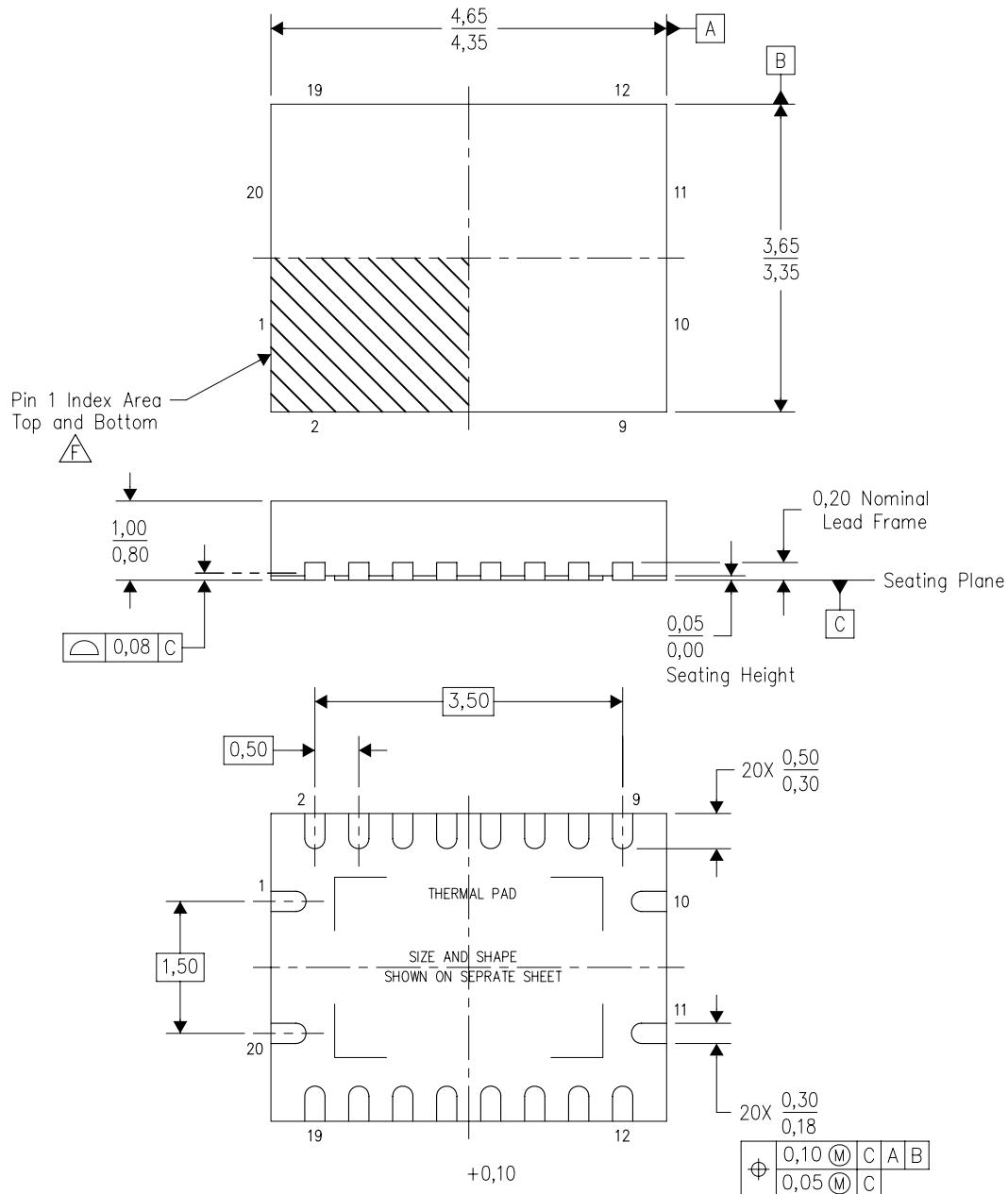


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## MECHANICAL DATA

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-4/l 06/2011

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

# THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N20)

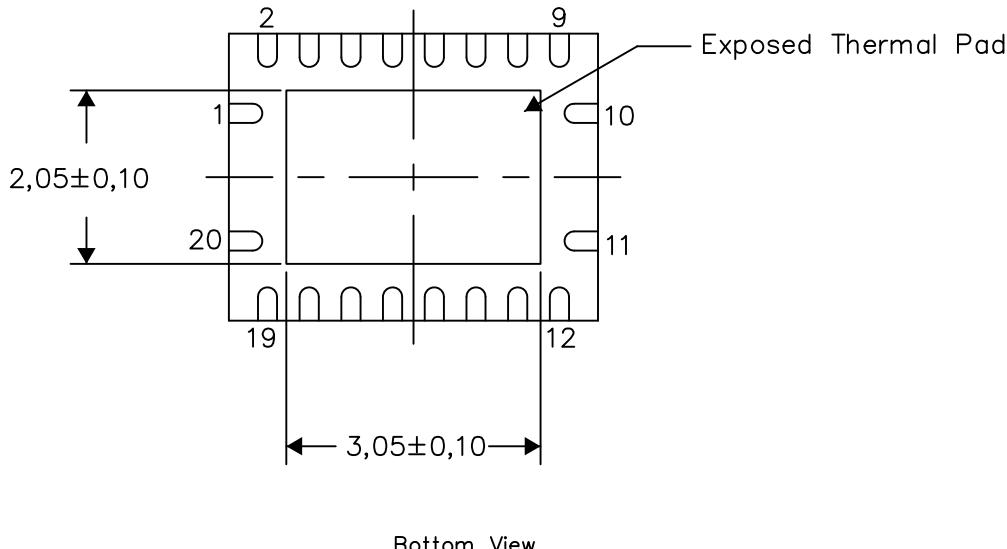
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

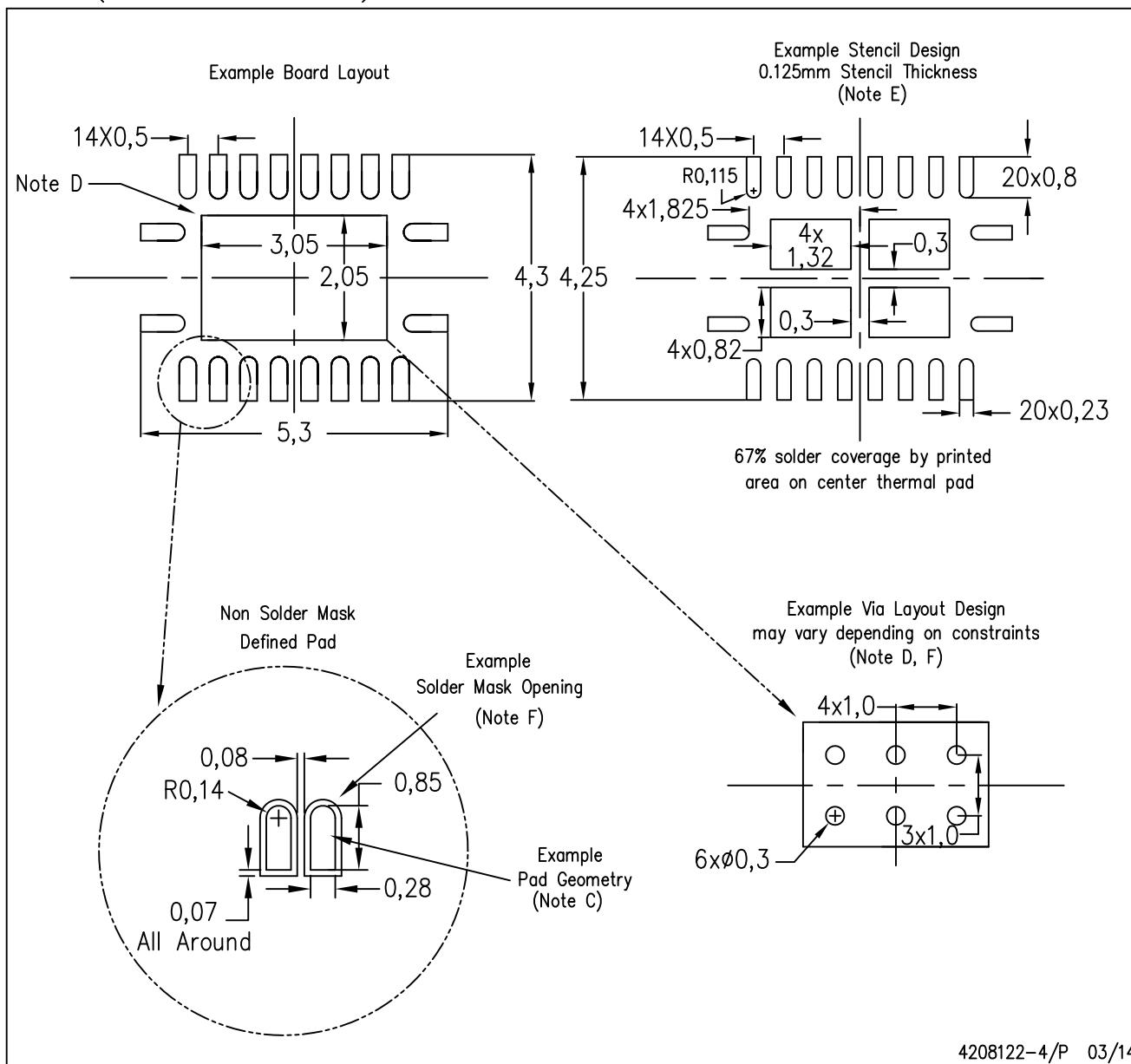
Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-4/P 03/14

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
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