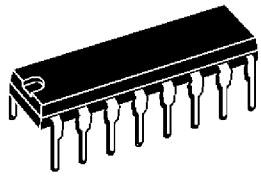
SGS-THOMSON MICROELECTRONICS

TEA2164S

SWITCH MODE POWER SUPPLY PRIMARY CIRCUIT

- POSITIVE AND NEGATIVE OUTPUT CURRENT UP TO 1.2A AND – 1.7A
- A TWO LEVEL COLLECTOR CURRENT LIMITATION
- COMPLETE TURN OFF AFTER LONG DURATION OVERLOADS
- UNDER AND OVER VOLTAGE LOCK-OUT
- SOFT START BY PROGRESSIVE CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- BURST MODE OPERATION UNDER STAND-BY CONDITIONS



POWERDIP16
(Plastic Package)

ORDER CODE : TEA2164S

DESCRIPTION

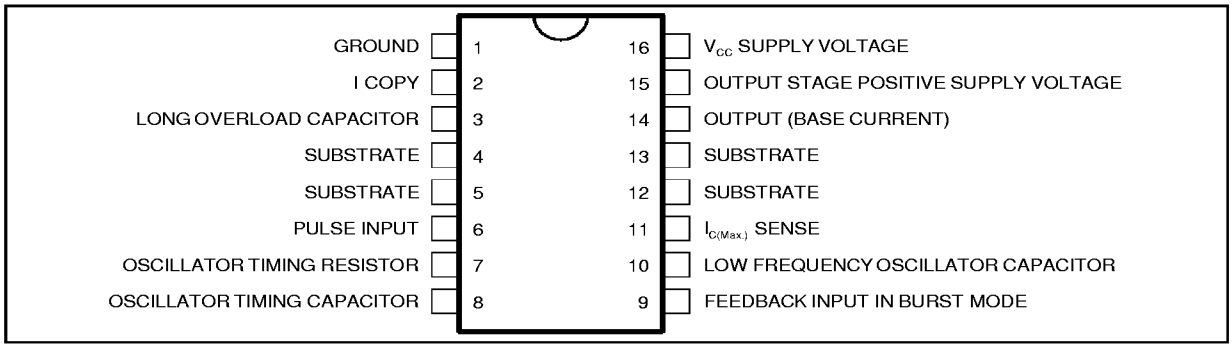
In a master slave architecture, the TEA2164S control IC achieves the slave function. Primarily designed for TV receivers and monitors applications, this circuit provides an easy synchronization and smart solution for low power stand by operation.

Located at the primary side the TEA2164S control IC ensures :

- the power supply start-up
- the power supply control under stand-by conditions
- the process of the regulation signals sent by the master circuit located at the secondary side
- direct base drive of the bipolar switching transistor
- the protection of the transistor and the power supply under abnormal conditions.

For more details, refer to application note AN409.

PIN CONNECTIONS



BLOCK DIAGRAM

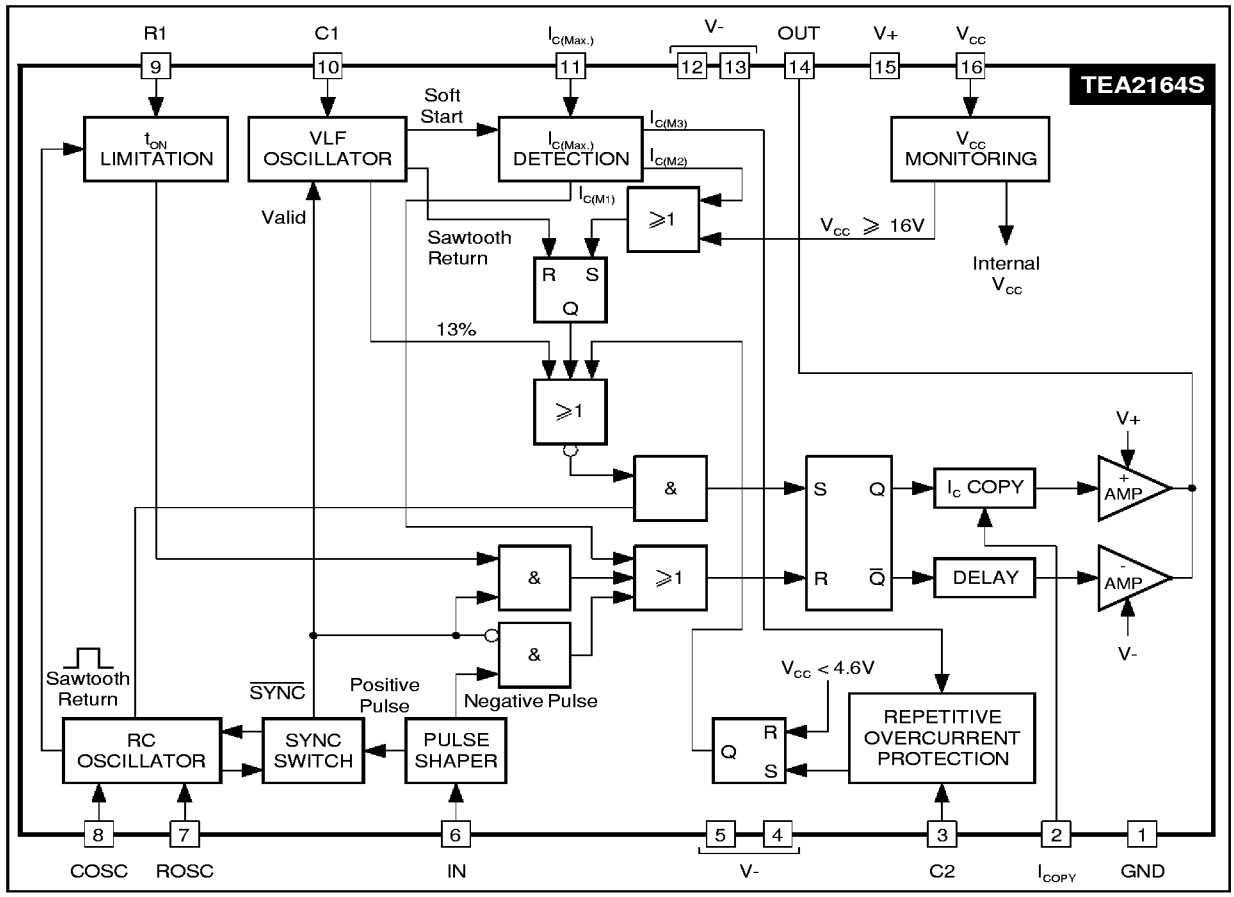
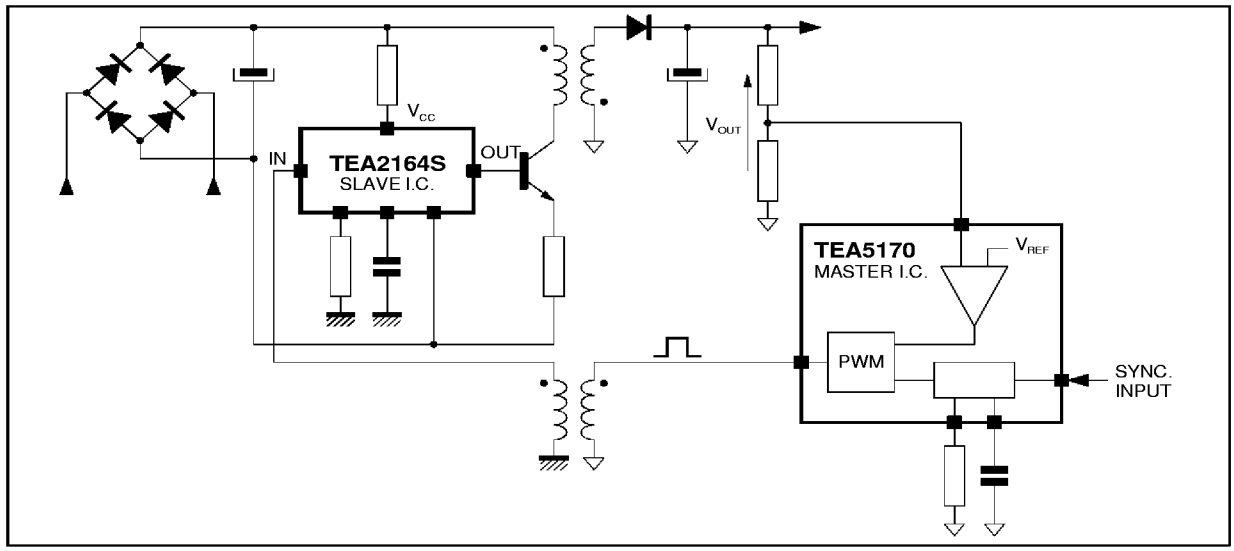


Figure 1 : Simplified Application Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive Power Supply V16-V1	18	V
V+	Positive Power Supply of the Output Stage V15-V1	18	V
V–	Negative Power Supply V4, 5, 12, 13-V1	– 5	V
V_{CC} - V– V+ - V–	Total Power Supply V16-V4, 5, 12, 13 or V15-V4, 5, 12, 13	20	V
I_{out+}	Positive Output Current	1.5	A
I_{out-}	Negative Output Current	2	A
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature	– 40, + 150	°C

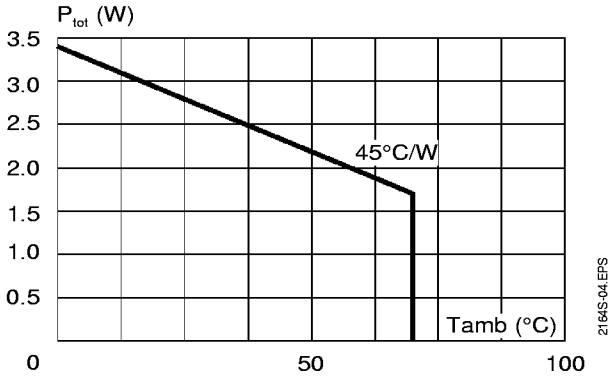
2164S-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction Case Thermal Resistance	11	°C/W

2164S-02.TBL

MAXIMUM POWER DISSIPATION

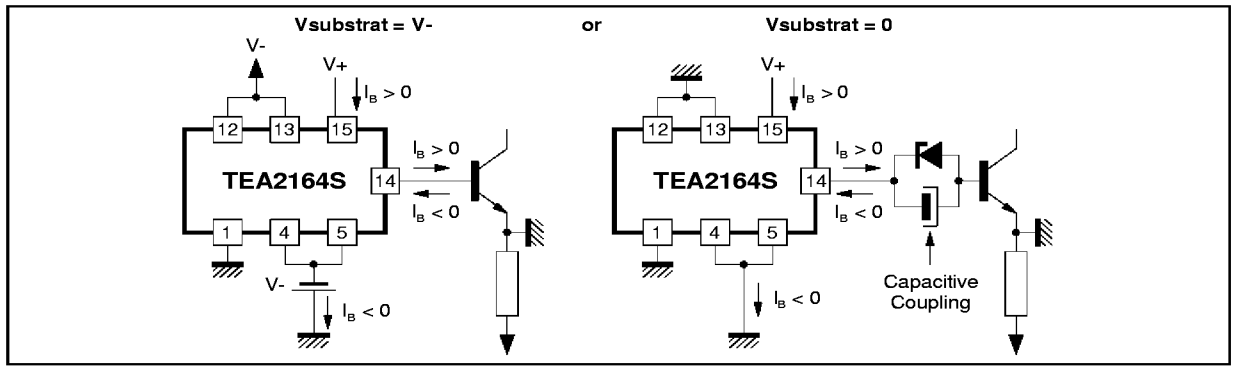


RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Positive Power Supply		10	14	V
V–	Negative Power Supply (see Figure 2)	-5		0	V
V_{CC} – V–	Total Power Supply			18	V
I_{out+}	Positive Output Current			1.2	A
I_{out-}	Negative Output Current			1.7	A
Fsw	Switching Frequency			50	khz
Ro	Oscillator Resistor Range	30		150	kΩ
Co	Oscillator Capacitor Range	470		2700	pF
C1	Starting Oscillator Capacitor Range	0.1		4.7	µF
C2	Repetitive Overload Protection Capacitor	1		22	µF
$\lvert V_{in} \rvert$	Input Pulses Amplitude (peak) (derivated pulses - time constant = 1 µs)	0.5		1	V
T_{oper}	Operating Ambiant Temperature	– 20		70	°C

2164S-03.TBL

Figure 2 : Substrat Biasing



ELECTRICAL OPERATING CHARACTERISTICS

$T_{amb} = 25^oC$, $V_{CC} = 10V$, $V_{CC-} = 0V$, potentials referenced to ground (Pin 1) (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLY					
V_{CC} (start)	Starting Voltage (V_{CC} increasing)	8	9	9.6	V
V_{CC} (stop)	Stopping Voltage (V_{CC} decreasing)	5	6.2	7.4	V
ΔV_{CC}	Hysteresis (V_{CC} start – V_{CC} stop)	2	2.8	3.5	V
V_{ccmax}	Overvoltage Lock-out	14.8	15.5	16.2	V
$I_{ccstart}$	Starting Positive Supply Current	0.5	0.8	1.5	mA
CURRENT LIMITATION AND PROTECTION (Pin 11)					
VCM1	Pulse by Pulse Current Limitation Threshold (see Note) TEA2164SL (Low range) TEA2164SH (high range)	 -1 -0.875	 -0.925 -0.775	 -0.825 -0.700	 V V
VCM2	Current Monitoring 2nd Threshold	1200	1350	1500	mV
ΔVCM	ΔVCM = VCM2 – VCM1 (L or H)	300	500	700	mV
REPETITIVE OVERCURRENT PROTECTION					
VCM3	Repetitive Overcurrent Threshold (Pin 11)	-1.1	-0.9	-0.7	V
VCM3 - VCM1	VCM3 - VCM1 (L or H)	-0.09	0.05	0.2	V
VC2	Lock-out Voltage on Pin 3	2.4	3	3.6	V
I3 disch	Capacitor C2 Discharge Current (synchronized mode)	10	20	30	µA
I3 ch.	Capacitor C2 Charge Current	50	80	110	µA
OSCILLATOR, MAX DUTY CYCLE, SYNCHRONIZATION					
T_o	Oscillator Initial Accuracy (RT = 50kΩ, CT = 1nF)	19.3	21	22.7	µs
$T_{on(max)}$	Maximum Duty Cycle ($T_{syn} = 1.05\ T_o$)	60	70	85	%
$\frac{T_{syn}}{T_O}$	Synchronization Window	1.0		1.5	
OUTPUT STAGE					
I_{14}/I_2	I_c Copy Current Gain		1000		
I_{BON}	Base Current Starting Pulse		300		mA
VERY LOW FREQUENCY OSCILLATOR					
	Burst Duty Cycle		13		%

2164S-04.TBL

Note : For the best accuracy of VCM1 value the TEA2164S is marked as follows : TEA2164SL (low range) or TEA2164SH (high range).

I - FIELD OF APPLICATION

The TEA2164S control circuit has been designed primarily for discontinuous mode flyback built with a master-slave architecture, whatever the field of application.

But due to its capability to synchronize the transistor switching-off with an external signal (line flyback) and due to an adapted burst-mode operation for a low power stand-by operation, the TEA2164 offers a smart solution for monitors and TV sets applications.

Power supply main features :

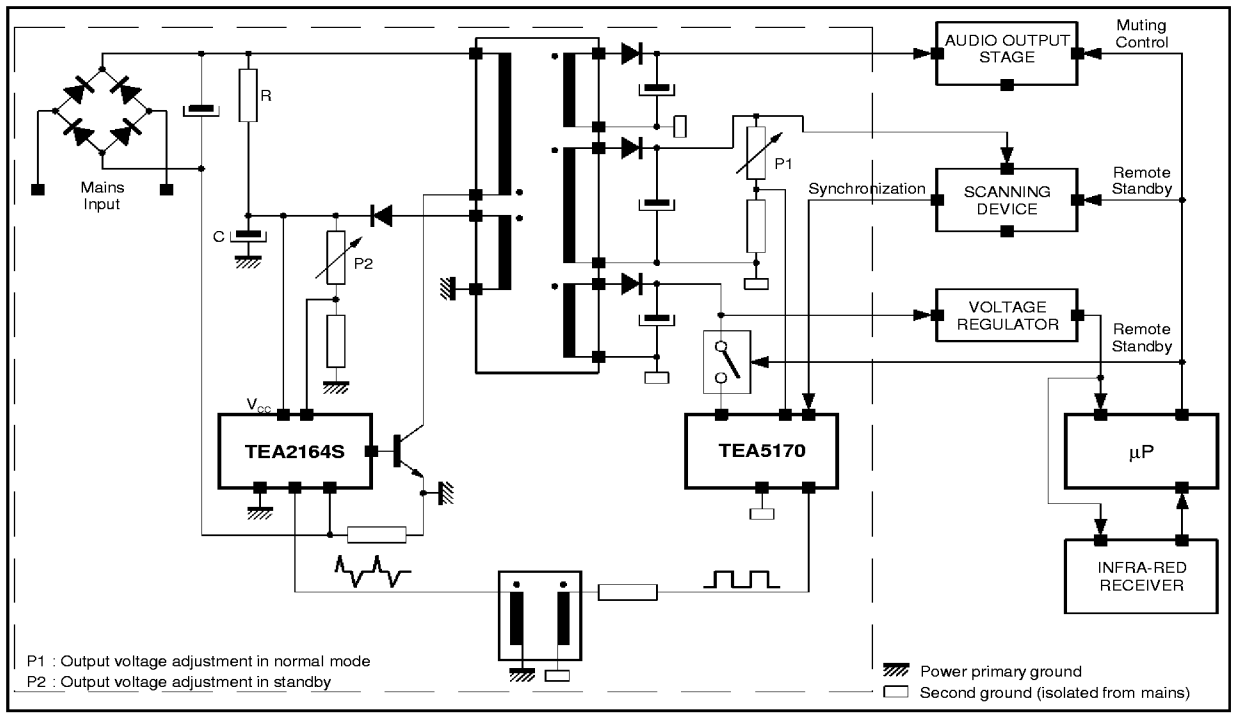
- maximum output power 140W (transistor forced gain : 3.5)
- stand-by mode output power (1W ≤ Psb ≤ 6W ; efficiency > 50%)
- operating frequency up to 50kHz
- power-switch : bipolar transistor

Adapted master-circuit :

- Monitor application → TEA5170
- Standard TV application → TEA2028B, TEA2029C, TEA2128, TEA5170
- Digital TV application → TEA5170

(TEA2028B, TEA2029C and TEA2128 are deflection processors with built-in PWM generator).

Figure 3 : Master Slave Power Supply Architecture



II - GENERAL DESCRIPTION

In a master slave architecture, the TEA2164S Control IC, located at the primary side of an off line power supply achieves the slave function ; whereas the master circuit is located at the secondary side. The link between both circuits is realized by a small pulse transformer (Figure 4).

In the operation of the master-slave architecture, four majors cases must be considered :

- normal operating
- stand-by mode
- power supply start-up
- abnormal conditions : off load, short circuit, ...

II.1 - Normal Operating (master slave mode)

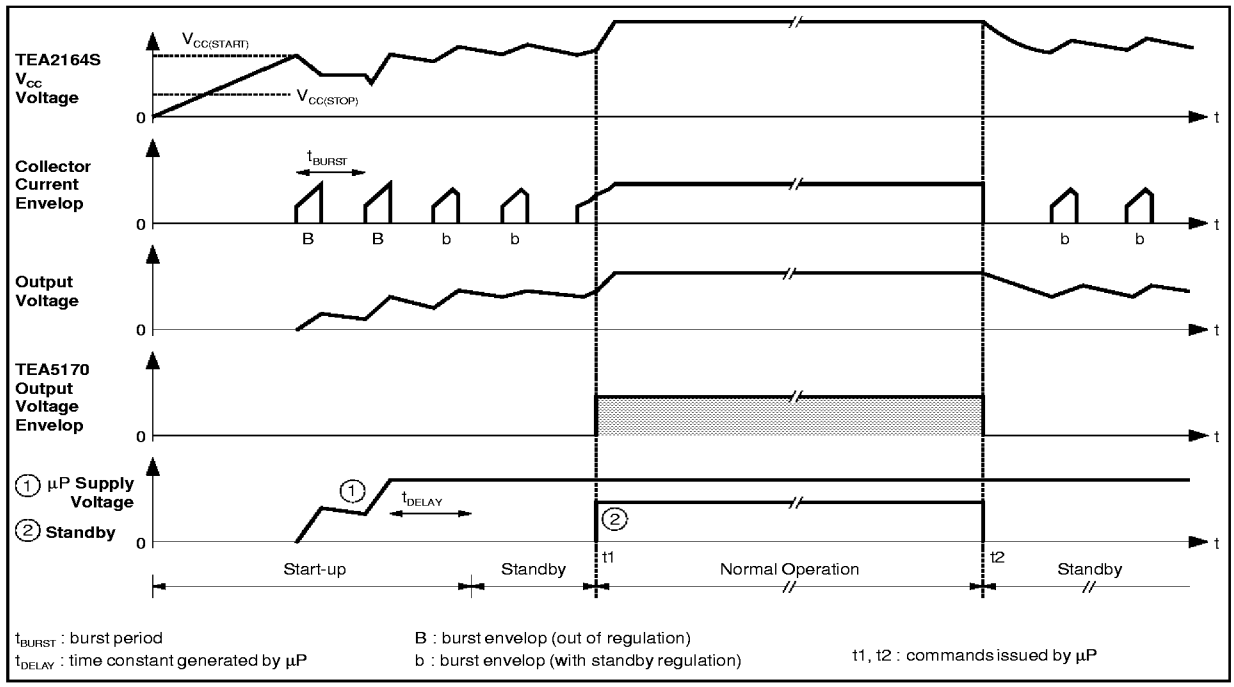
In this configuration, the master circuit generates a pulse width modulated signal issued from the monitoring of the output voltage which needs the best accuracy (in TV applications : the horizontal deflection stage supply voltage). The master circuit power supply can be supplied by another output.

The PWM signal are sent towards the primary side through small differentiating transformer. For the TEA2164S positive pulses are transistor switching-on commands ; and negative pulses are transistor switching-off commands (Figure 5). In this configuration, only by synchronizing the master oscillator, the switching transistor may be synchronized with an external signal.

II.2 - Stand-by Mode

In this configuration the master circuit no longer sends PWM signals, the structure is not synchronized ; and the TEA2164S operates in burst mode. The average power consumption at the secondary side may be very low 1W ≤ P ≤ 6W (as it is consumed in TV set during stand by).
By action on the maximum duty cycle control, a primary loop maintains a semi-regulation of the output voltages. Voltage on feed-back is applied on Pin 9.
Burst period is externally programmed by capacitor C1.

Figure 4 : System Description Waveforms



II - GENERAL DESCRIPTION (continued)

Figure 5 : Master Slave Mode Waveforms

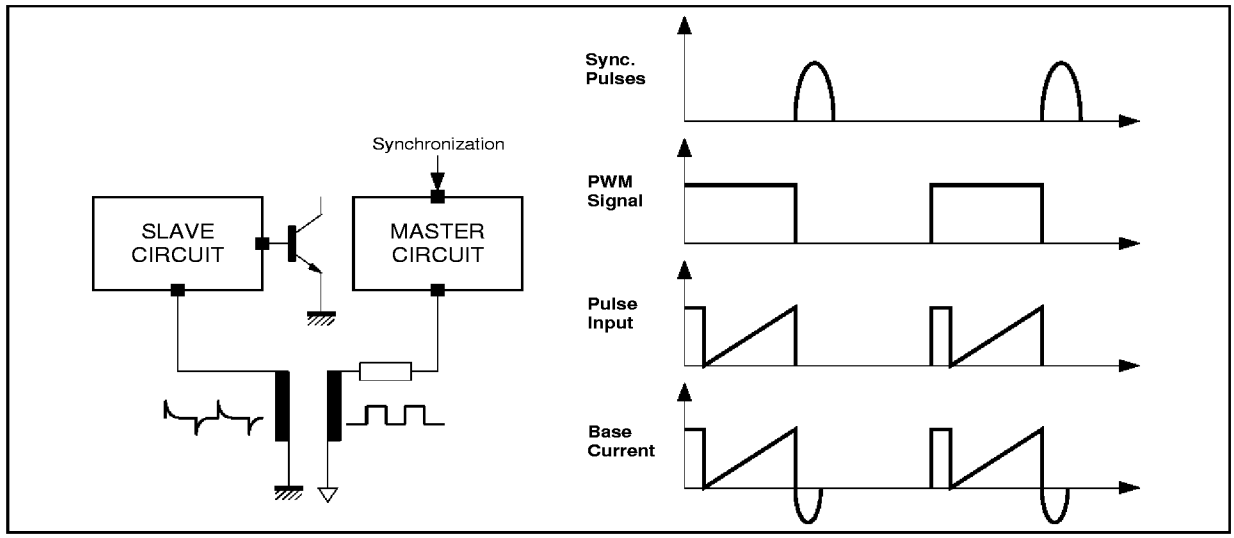
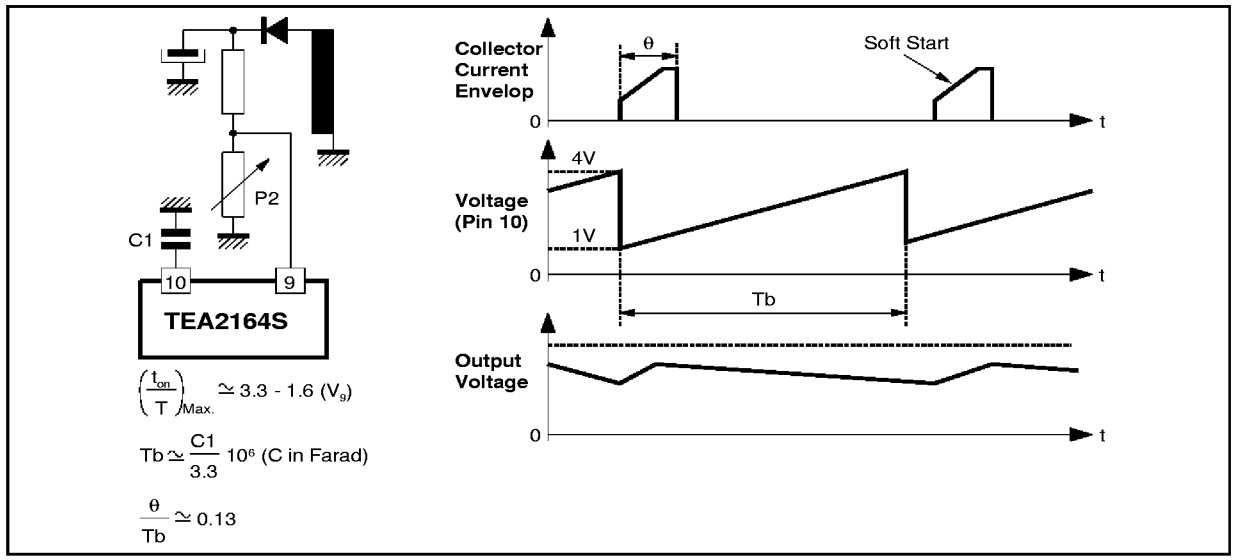


Figure 6 : Burst Mode Waveforms



II.3 - Power Supply Start-up

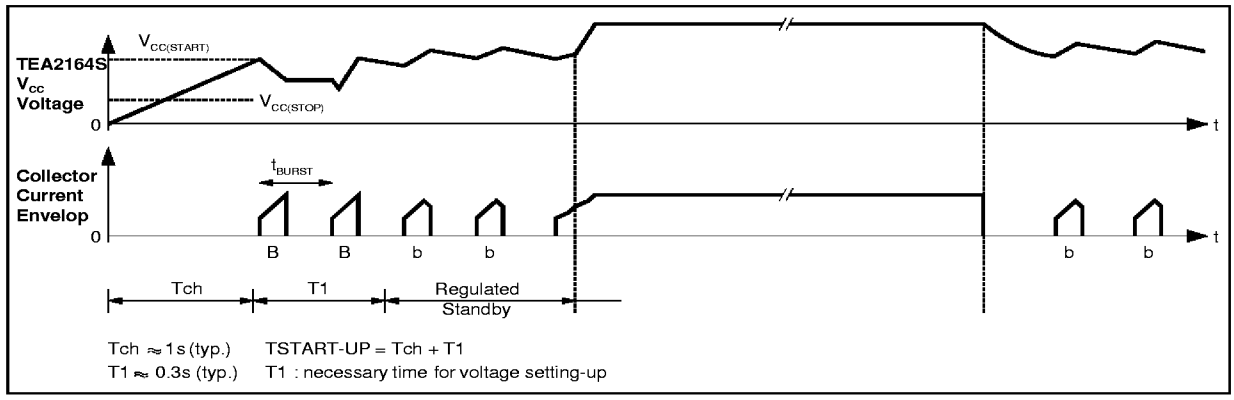
After the mains have been switched-on, the V_{CC} storage capacitor of the TEA2164S is charged through a high value resistor connected to the rectified high voltage.

When Vcc reaches V_{CC} start threshold (9V typ), the TEA2164 starts operating in burst mode. Since available output power is low in burst mode the output power consumption must remain low before complete setting-up of output voltage.

In TV application it can be achieved by maintaining the TV in stand-by mode during start-up (Figure 7).

II - GENERAL DESCRIPTION (continued)

Figure 7 : Power Supply Start-up



II.4 - Abnormal conditions : safety functions

Overvoltage Protection

When V_{CC} exceeds V_{CC} max, an internal flip-flop stops output conduction signals. The circuit will start again after the capacitor C1 discharge ; it means : after loss of synchronization or after V_{CC} stop crossing (Figure 8).

In flyback converters, this function protects the power supply against output voltage runaway.

Under Voltage Lock-out

The TEA2164S control circuit stops operating when V_{CC} goes under V_{CC} stop.

Power Limitation, Current Protection, Long Duration Overload Protection

- Output power limitation : by a pulse by pulse collector current limitation the TEA2164S limits the maximum output power. V_{CM1} is the corresponding voltage threshold, its detection is memorized up to the next period.
- Current protection (transistor protection)
  Under particular conditions a hard overload or short circuit may induce a flux runaway in spite of the current limitation (V_{CM1}).
  The TEA2164S control circuit features a second current protection, V_{CM2}. When this threshold is reached an internal flip-flop memorizes it and output conduction signals are inhibited. The circuit will send base drives again after capacitor C1 discharge (Figure 8).
- Long duration overload protection : (Figure 9)
  An overload is detected when the sense-voltage on Pin 11 reaches V_{CM3} before a negative pulse has been applied to Pin 6. In this case the capacitor C2 (connected to Pin 3) is charged with I_3 ch up to the end of the period and discharged with I_3 disch until a next V_{CM3} detector. By this way in case of long duration overload, the capacitor keeps charging at each period and its voltage encreases gradually. When the voltage on Pin 3 exceeds V_{C2}, the TEA2164S control circuit stops sending base drives and memorizes this event. No restart is allowed as long as $V_{pin\ 3}$ is higher than V_{C2} and V_{CC} higher than 4.8V.

**** Remark :***

- The harder is the overload the faster is the protection
- The capacitor keeps charging between two burst after V_{CM2} detection.

II - GENERAL DESCRIPTION (continued)

Figure 8 : Overvoltages Lock-out

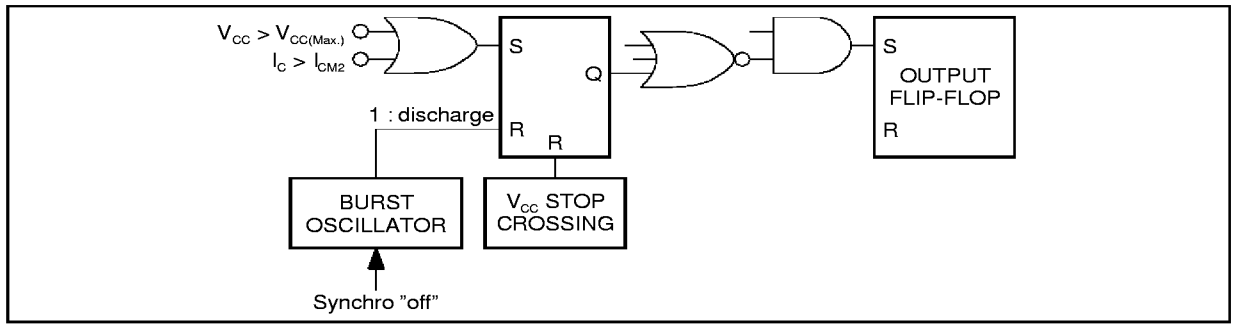


Figure 9 : Long Duration Overload Monitoring Circuit

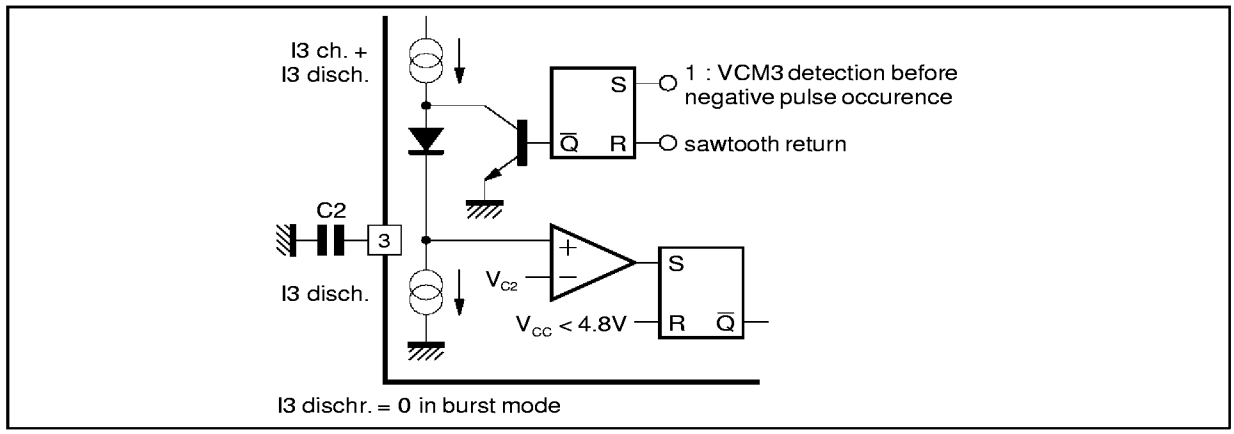
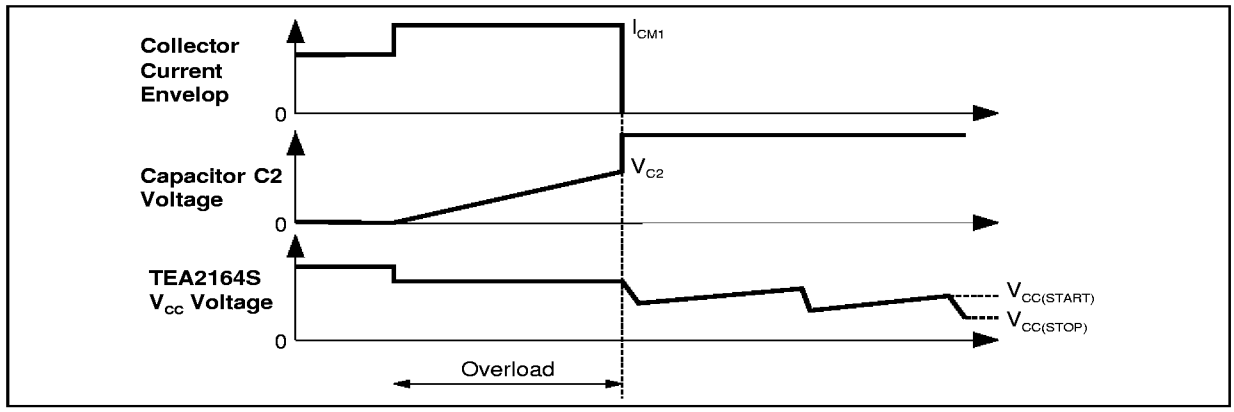
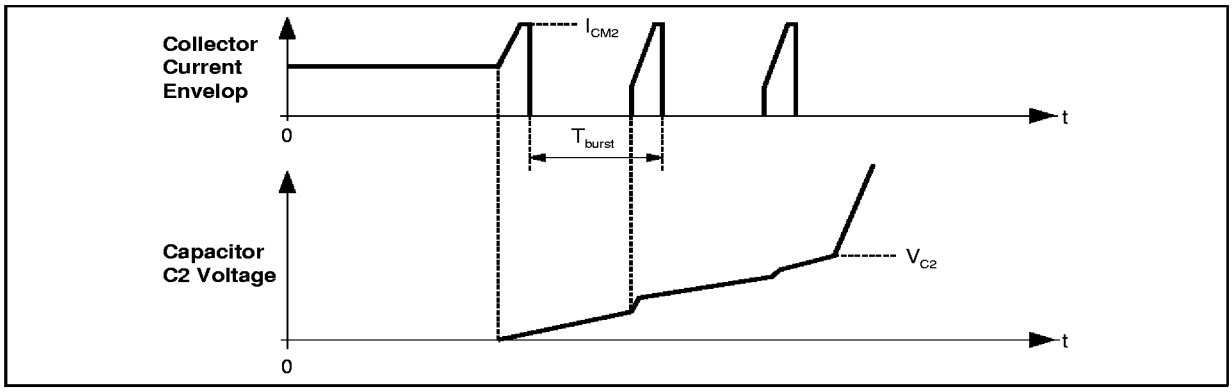


Figure 10 : Long Duration Overload Detection



II - GENERAL DESCRIPTION (continued)

Figure 11 : Repetitive Over-current Protection



III - SWITCHING OSCILLATOR AND SYNCHRONIZATION

III.1. Switching oscillator

When the TEA2164S control circuit operates in burst mode, the switching frequency is fixed by the free frequency oscillator. The period is determined by two external components C_O and R_O.

III.2. Synchronization

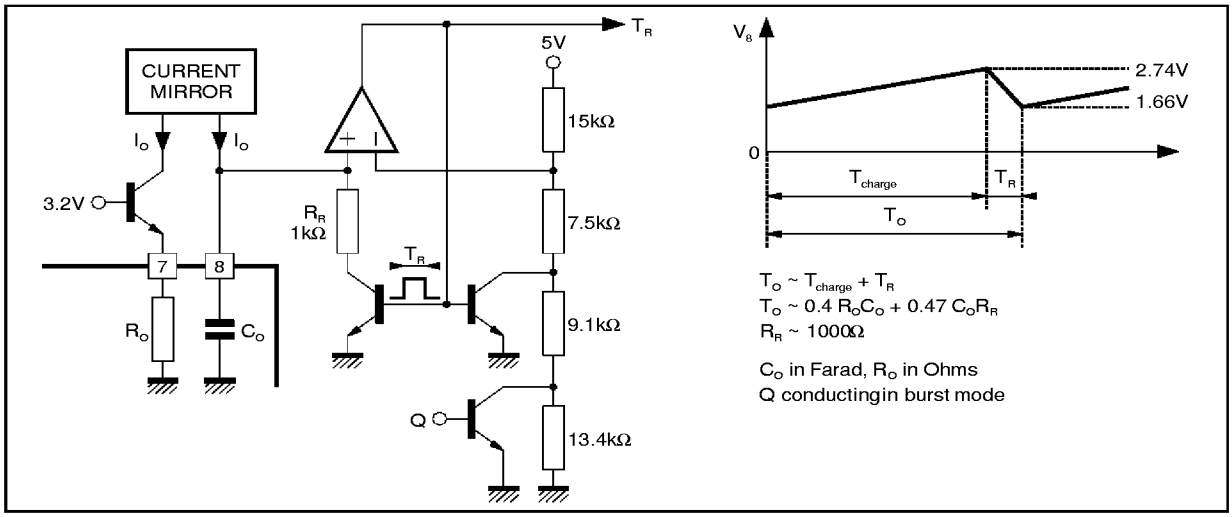
When the master-circuit starts to send pulses both oscillators are not synchonuous.

In order to avoid any erratic conduction of the power transistor, the first synchronization pulse will arrive simultanously with the sawtooth return of the TEA2164S oscillator.

To get synchronization the free frequency must be higher than the synchronization frequency.

$$T_O < T_{sync.} < 1.50\ T_O$$

Figure 12 : Free Frequency Running



III - SWITCHING OSCILLATOR AND SYNCHRONIZATION (continued)

Figure 13 : Synchronization Pulse Shaper and Synchronization

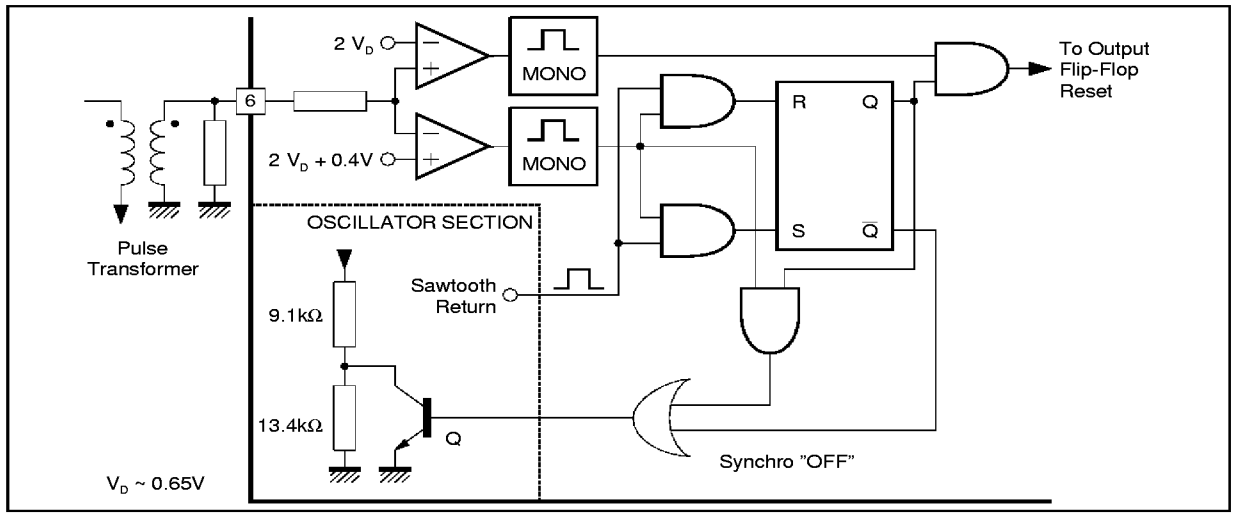
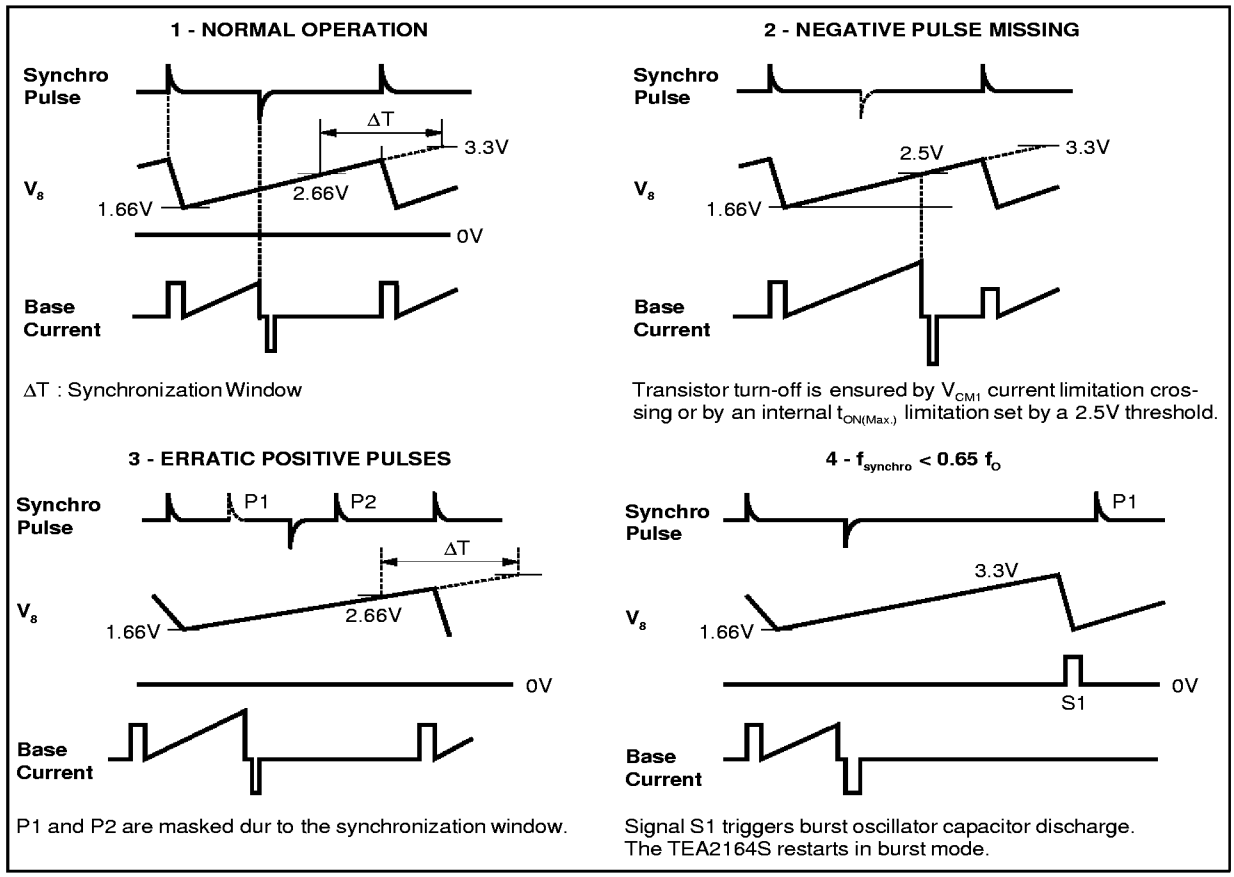


Figure 14 : Operation after Synchronization



IV - MAXIMUM DUTY CYCLE LIMITATION

Burst mode : The maximum duty cycle is controlled by the voltage on Pin 9 (Figure 15).

Synchronized mode : Normally the maximum duty cycle is set by the master circuit. However the maximum conducting time will never exceed the value given by the comparison of the oscillator wave-form with the 2.5V internal threshold.

V - OUTPUT STAGE

TEA2164S output stage has been designed to drive switching bipolar transistor.

- Each base drive begins with a positive pulse I_{BON} that realizes an efficient transistor turn-on.
- After the starting pulse I_{BON}, the base current is proportional to the collector current. The current gain is easily fixed by a resistor R_B (Figure 16).
- A fast and safe transistor turn-off is realized by a fast positive base current cut-off and by applying a negative base drive which draws stored carriers. A typical 0.7s delay prevents from cross-conduction of positive and negative output stages.

Remark : In order to reduce power dissipation on the positive output stage with the low gain transistors, for high base currents the positive output stage operates in saturated mode (Figure 17). This can be achieved by using a resistor between V_{CC} and V+.

Figure 15 : Maximum Duty Cycle Limitation

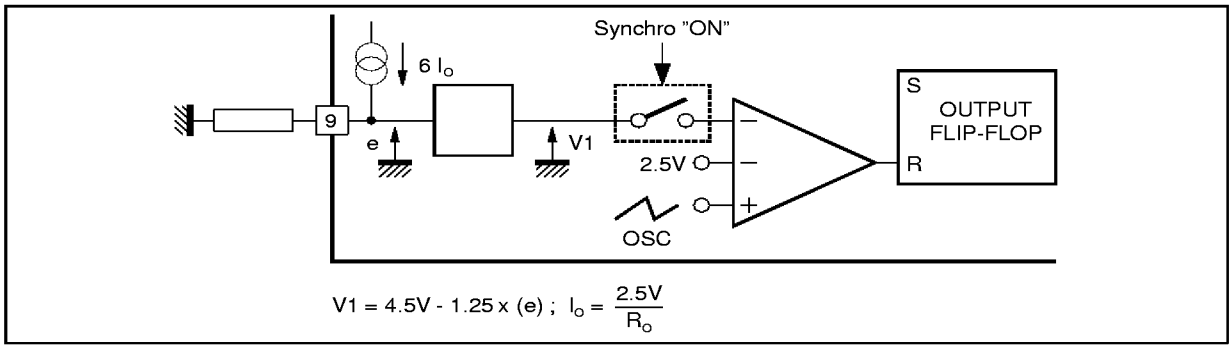
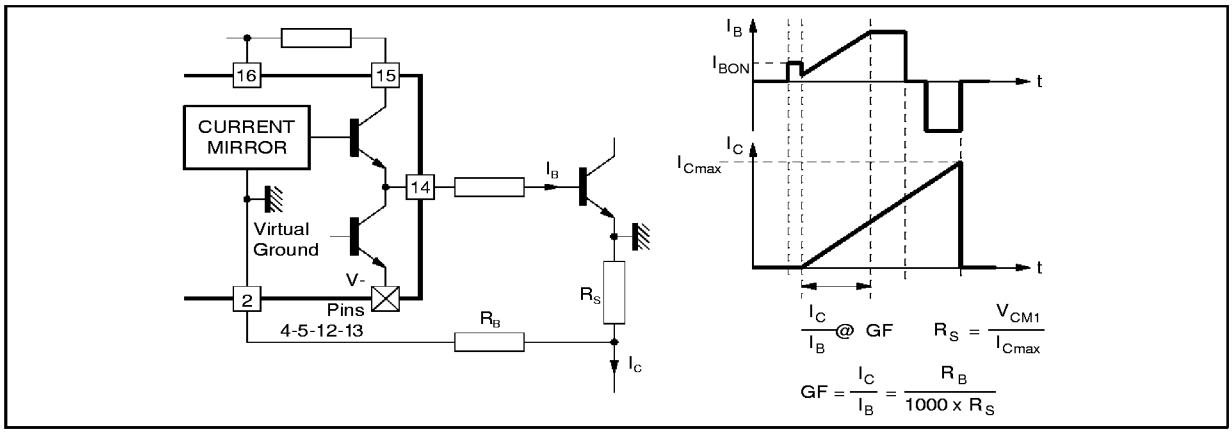
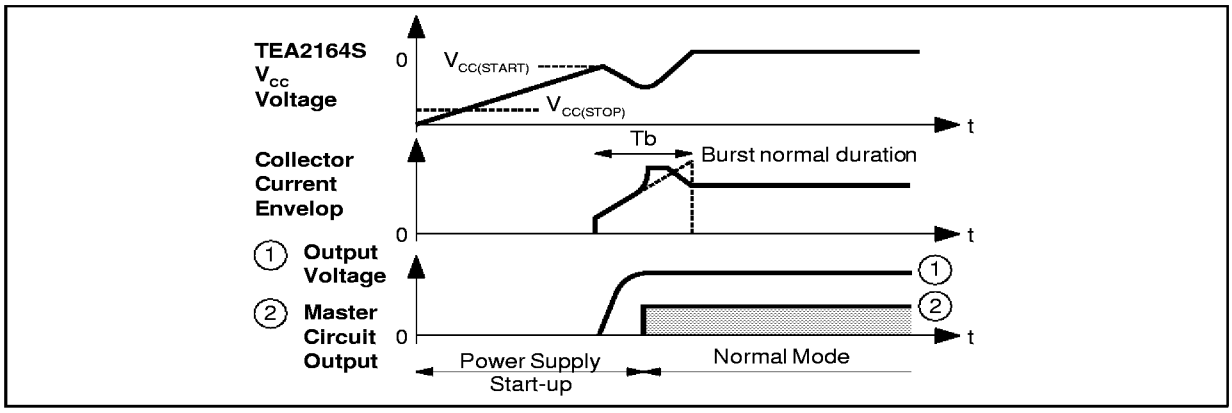


Figure 16 : Output Stage Architecture and Base Drive



V - OUTPUT STAGE (continued)

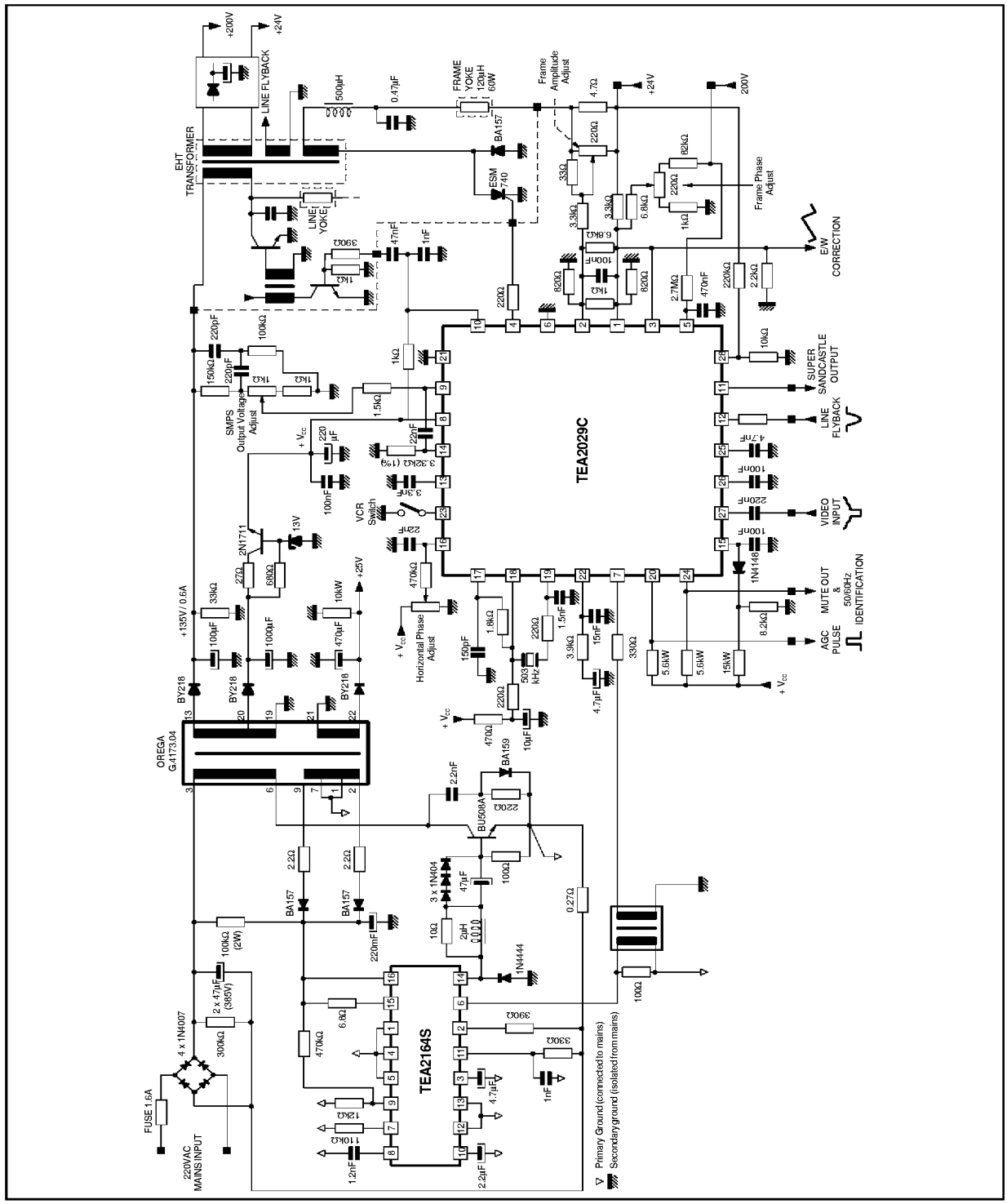
Figure 17 : Power Supply Start-up and Normal Operation



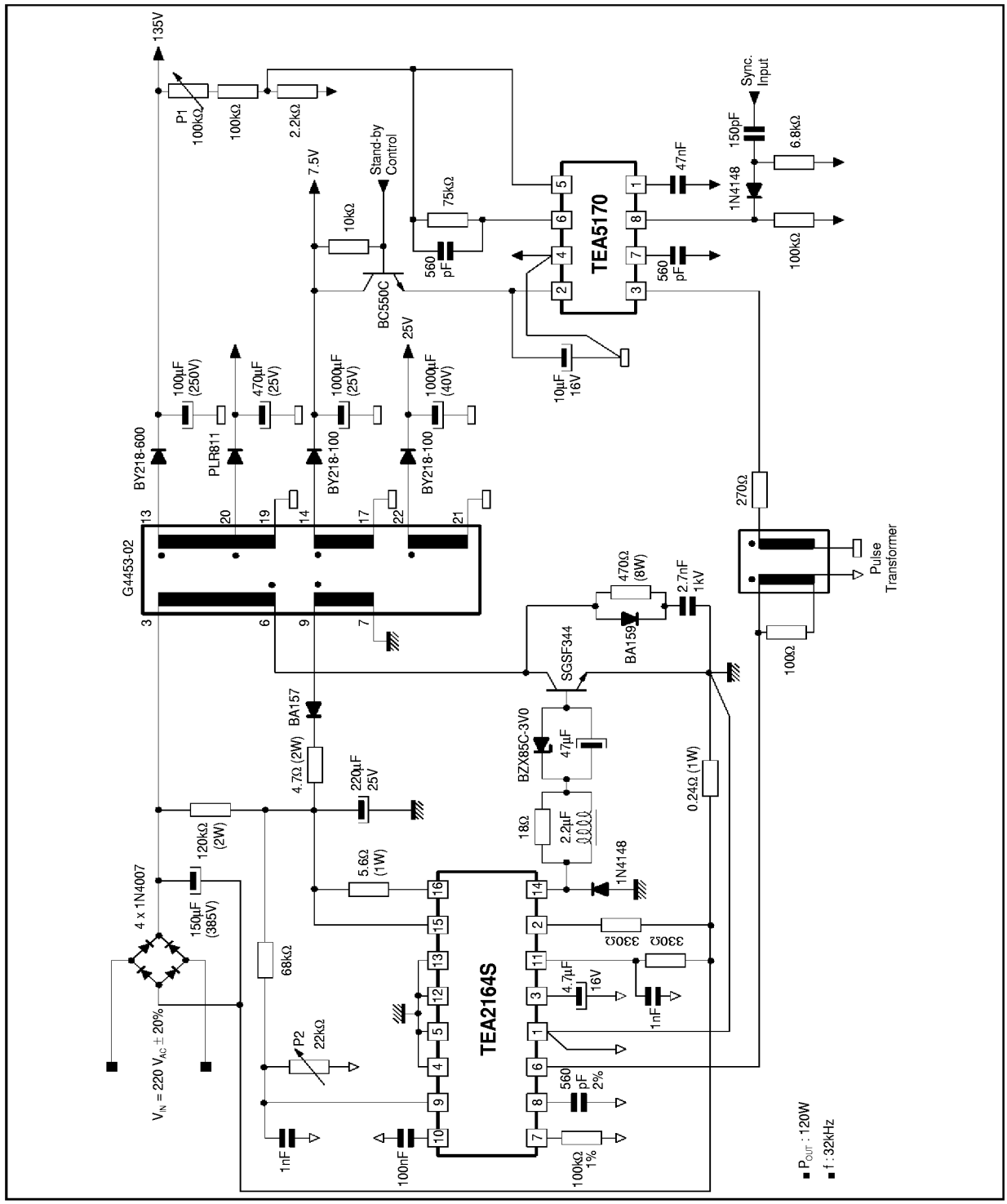
VI - MONITOR APPLICATIONS

In most of monitor applications, the power supply must start-up under full load conditions and the stand -by mode is no longer useful.
The energy of the starting burst must be high enough to ensure start-up, then the capacitor C1 must be higher in these applications than on TV application (typ. : 1µF).

COMPLETE APPLICATION DIAGRAM (SMPS + DEFLECTION) (with stand-by function)

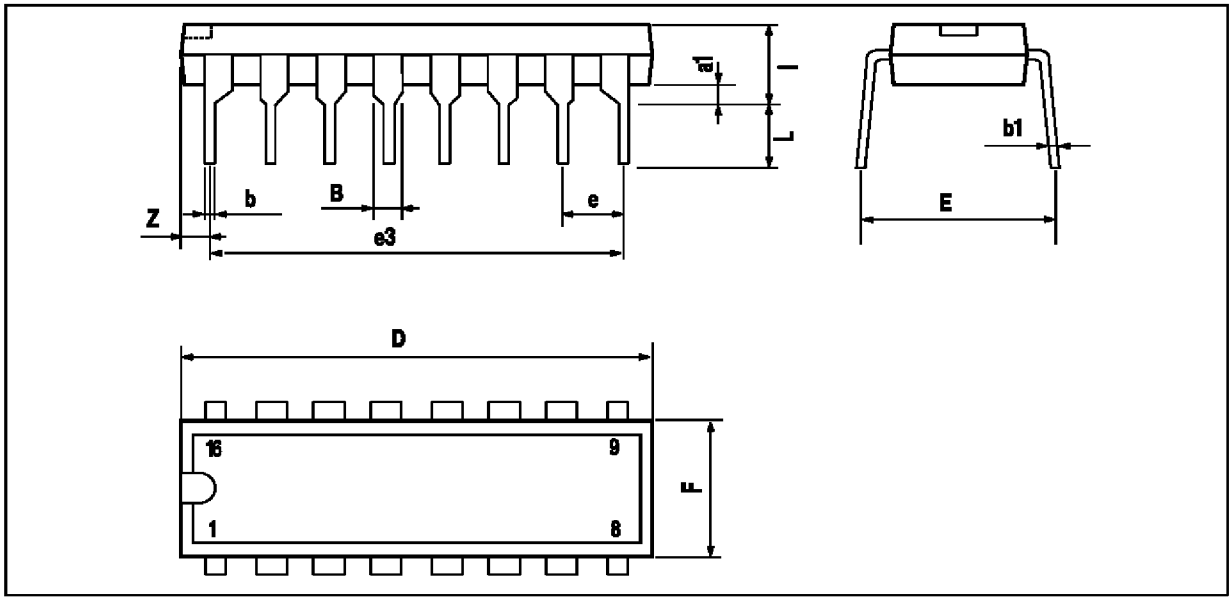


STAND-ALONE 32kHz POWER SUPPLY ELECTRICAL DIAGRAM



PACKAGE MECHANICAL DATA

16 PINS - PLASTIC POWERDIP



PM-DIP16.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

DIP16PW.TBL