- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V$_{CC}$ and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11030 . . . J PACKAGE
74ACT11030 . . . D OR N PACKAGE
(TOP VIEW)

```
        ____  ____
C  [ 1      14 ] D
B  [ 2      13 ] E
A  [ 3      12 ] F
GND[ 4      11 ] V_CC
Y  [ 5      10 ] NC
NC [ 6       9 ] G
NC [ 7       8 ] H
```
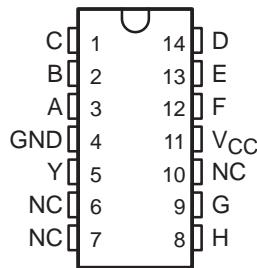
54ACT11030 . . . FK PACKAGE
(TOP VIEW)

```
            E  F  NC V_CC NC
            3  2  1  20  19
      D  [ 4              18 ] G
      NC [ 5              17 ] NC
      C  [ 6              16 ] H
      NC [ 7              15 ] NC
      B  [ 8              14 ] NC
            9  10 11 12 13
            A  GND NC Y  NC
```
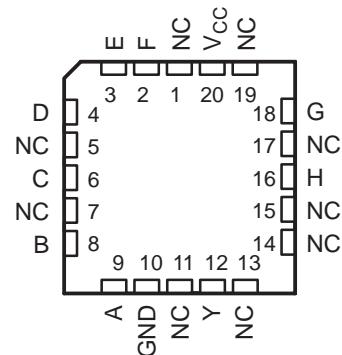
NC – No internal connection

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H} \text{ or}$$
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The 54ACT11030 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11030 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

| INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol†

logic diagram (positive logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.
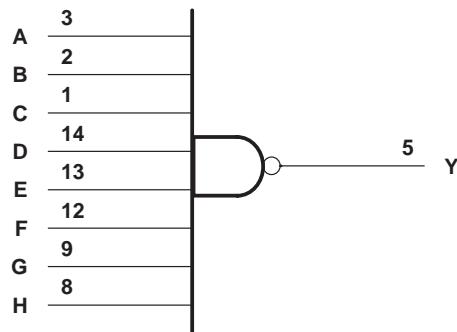
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TEXAS INSTRUMENTS

54ACT11030, 74ACT11030
8-INPUT POSITIVE-NAND GATES

SCLS050 – MARCH 1987 – REVISED APRIL 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		54ACT11030		74ACT11030		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			54ACT11030		74ACT11030		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24\ mA$		4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50\ mA$†		5.5 V				3.85				
	$I_{OH} = -75\ mA$†		5.5 V						3.85		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24\ mA$		4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50\ mA$†		5.5 V					1.65			
	$I_{OL} = 75\ mA$†		5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND		5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54ACT11030		74ACT11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A thru H	Y	1.5	5.4	8.1	1.5	8.8	1.5	8.5	ns
t_{PHL}			1.5	5.9	7.8	1.5	9.3	1.5	8.7	

operating characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	$C_L = 50\ pF$,	$f = 1\ MHz$	41	pF

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

From Output Under Test

C_L = 50 pF (see Note A)

500 Ω

LOAD CIRCUIT

Input (see Note B)

3 V

1.5 V

1.5 V

0 V

t_{PHL}

t_{PLH}

Output

V_{OH}

50% V_{CC}

50% V_{CC}

V_{OL}
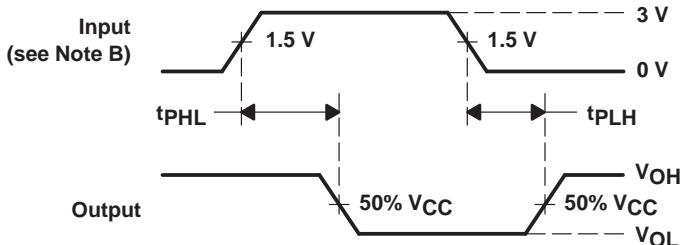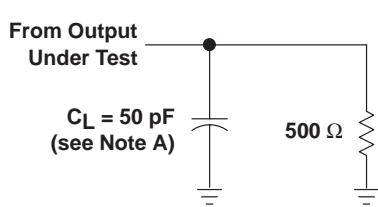
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74ACT11030D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	ACT11030
74ACT11030DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11030
74ACT11030DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11030
74ACT11030N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74ACT11030N
74ACT11030N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74ACT11030N

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
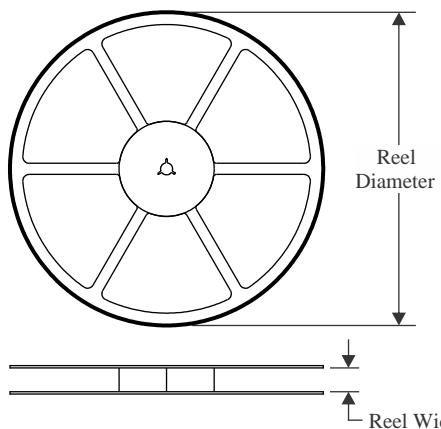
TAPE DIMENSIONS
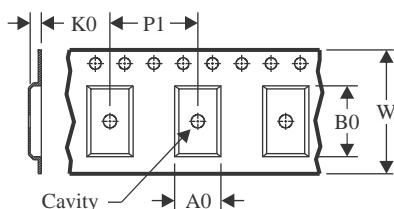
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
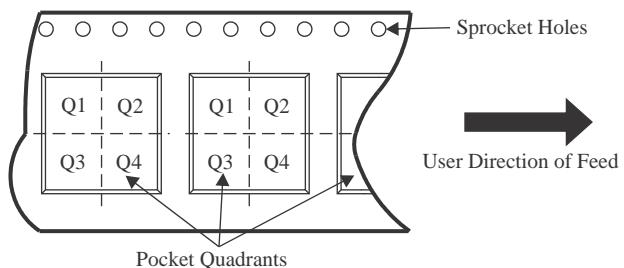
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT11030DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
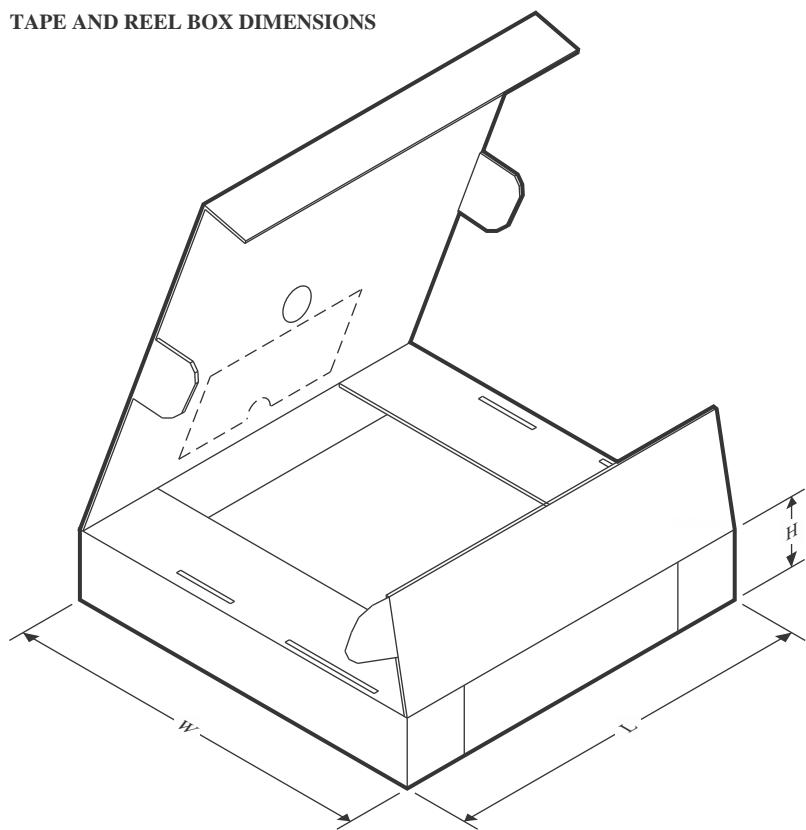
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT11030DR	SOIC	D	14	2500	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

TUBE
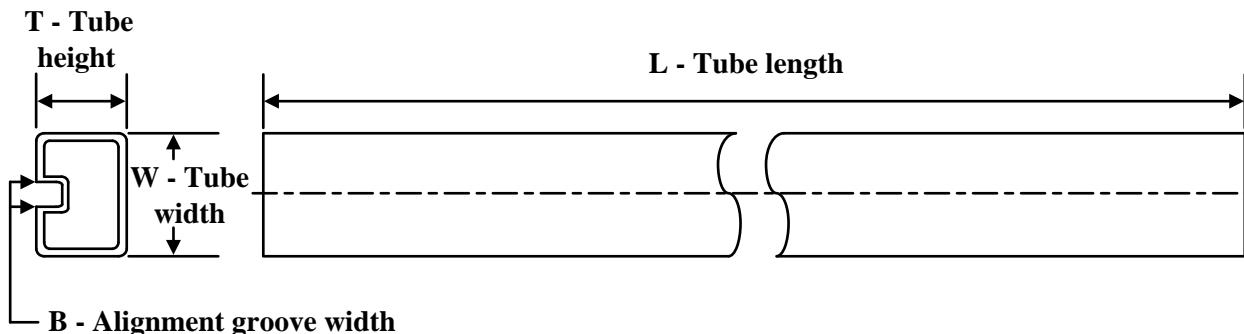
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74ACT11030N	N	PDIP	14	25	506	13.97	11230	4.32
74ACT11030N	N	PDIP	14	25	506	13.97	11230	4.32
74ACT11030N.A	N	PDIP	14	25	506	13.97	11230	4.32
74ACT11030N.A	N	PDIP	14	25	506	13.97	11230	4.32

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

0.010 (0,25) M

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

6.2
5.8 TYP

A

PIN 1 ID
AREA

1

14

12X 1.27

8.75
8.55
NOTE 3

2X
7.62

7

8

14X 0.51
0.31

B

4.0
3.8
NOTE 4

⊕ 0.25Ⓜ C A B

C

SEATING PLANE

◯ 0.1 C

1.75 MAX

SEE DETAIL A

0.25
0.13 TYP

0.25
GAGE PLANE

0° - 8°

1.27
0.40

0.25
0.10

DETAIL A
TYPICAL
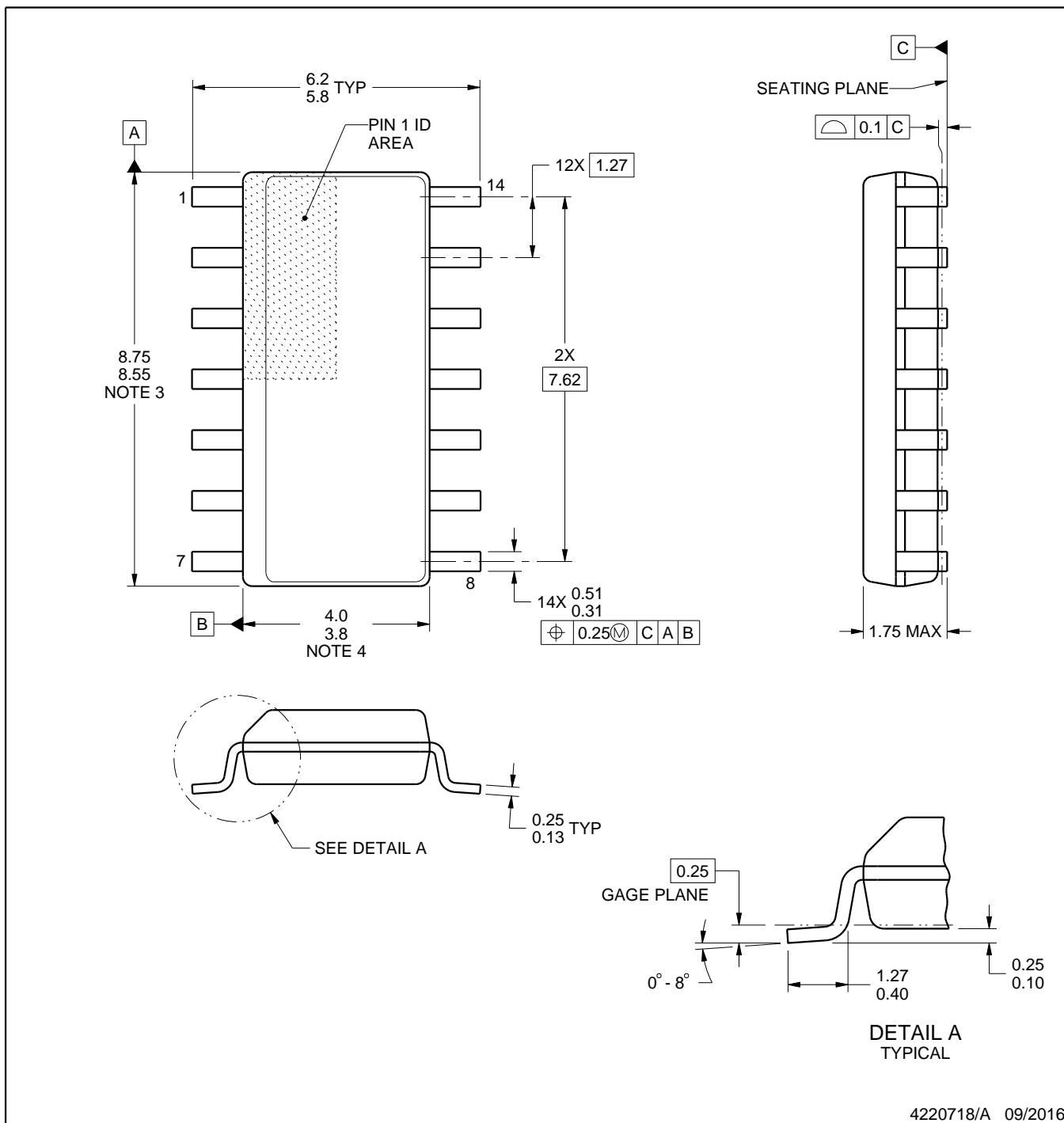
4220718/A   09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

D0014A

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

14

SYMM

7

8

(R0.05)
TYP

(5.4)
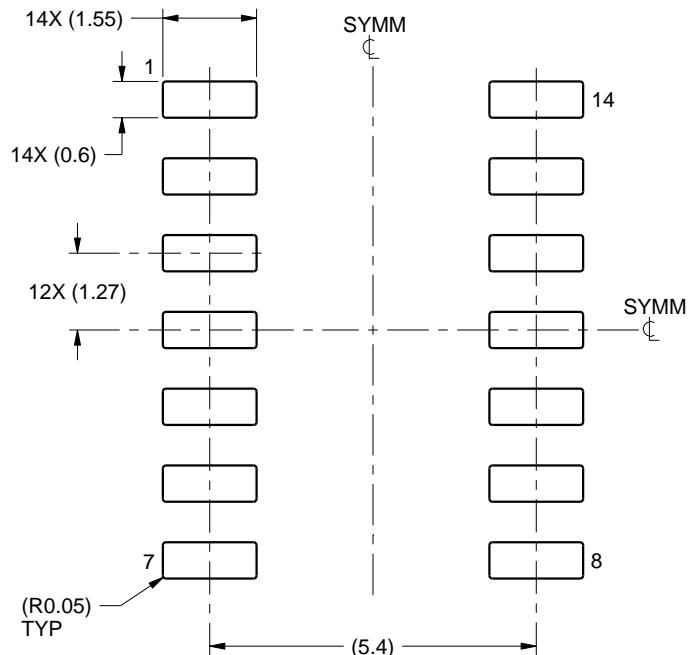
LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND
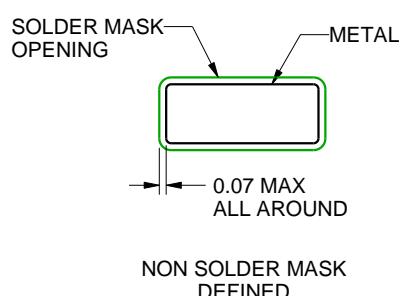
**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND
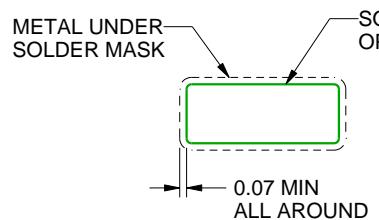
**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.55)

SYMM

1

14

14X (0.6)

12X (1.27)

SYMM

7

8

(5.4)
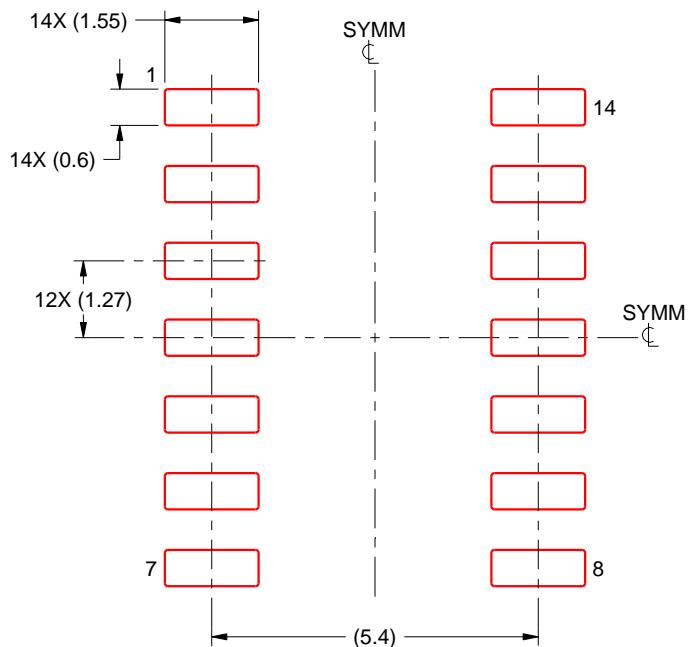
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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