Document Number: A2T26H300-24S
Rev. 0, 9/2015

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 60 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2496 to 2690 MHz.

2600 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.8 Vdc, P_{out} = 60 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

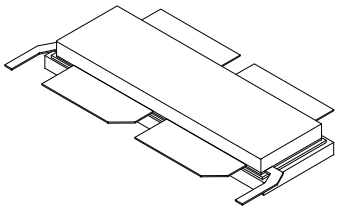
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	14.5	42.5	7.9	–30.7
2590 MHz	15.0	43.4	7.9	–32.2
2690 MHz	14.9	43.3	7.8	–33.5

Features

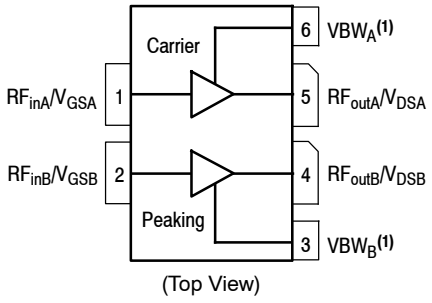
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

A2T26H300-24SR6

2496–2690 MHz, 60 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-1230S-4L2L



(Top View)

Figure 1. Pin Connections

1. Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 79°C, 60 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.8 Vdc, 2590 MHz	$R_{\theta JC}$	0.29	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 160 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 800 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.6 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 240 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.4 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.8 Vdc, P_{out} = 60 W Avg., f = 2496 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	13.4	14.5	16.4	dB
Drain Efficiency	η_D	37.5	42.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.5	7.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	–30.7	–29.0	dBc
Load Mismatch (2) (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 800 mA, V_{GSB} = 0.8 Vdc, f = 2590 MHz, 100 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 355 W Pulsed CW Output Power (3 dB Input Overdrive from 229 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.8 Vdc, 2496–2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	209	—	W
P_{out} @ 3 dB Compression Point (3)	P3dB	—	363	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496–2690 MHz frequency range)	Φ	—	–26.7	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	100	—	MHz
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 60 W Avg.	G_F	—	0.95	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.011	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.005	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T26H300-24SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	NI-1230S-4L2L

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

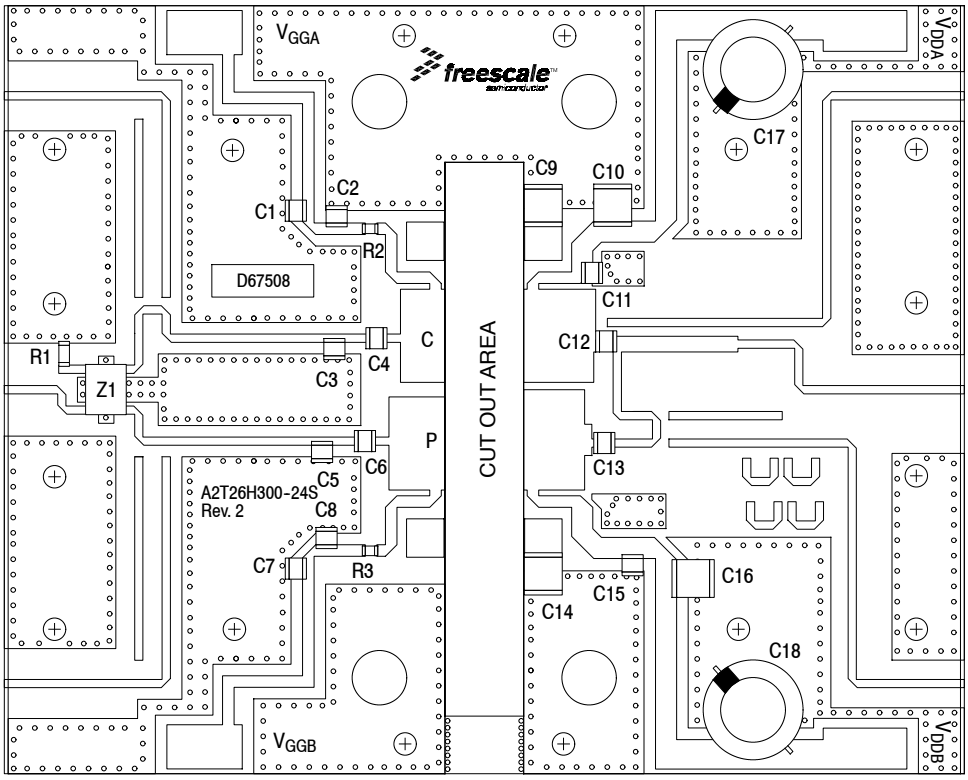


Figure 2. A2T26H300-24SR6 Test Circuit Component Layout

Table 6. A2T26H300-24SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C7, C9, C10, C14, C16	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C4, C6, C8, C11, C13, C15	5.1 pF Chip Capacitors	ATC100B5R1CT500XT	ATC
C3	0.4 pF Chip Capacitor	ATC100B0R4CT500XT	ATC
C5	1.0 pF Chip Capacitor	ATC100B1R0CT500XT	ATC
C12	3.0 pF Chip Capacitor	ATC100B3R0CT500XT	ATC
C17, C18	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26	Multicomp
R1	50 Ω, 4 W Termination	CW12010T0050GBK	ATC
R2, R3	2.7 Ω, 1/4 W Chip Resistors	CRCW12062R7FKEA	Vishay
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	X3C25P1-02S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D67508	MTL

TYPICAL CHARACTERISTICS

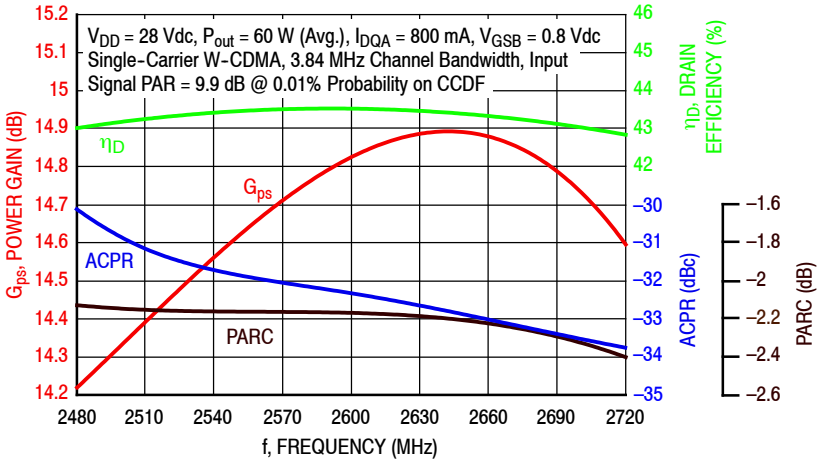


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 60 Watts Avg.

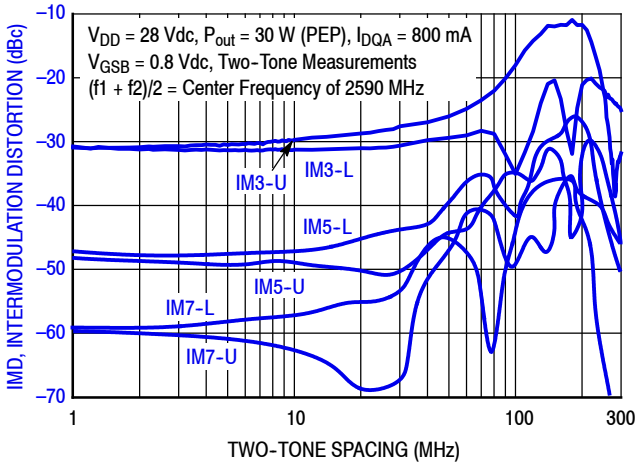


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

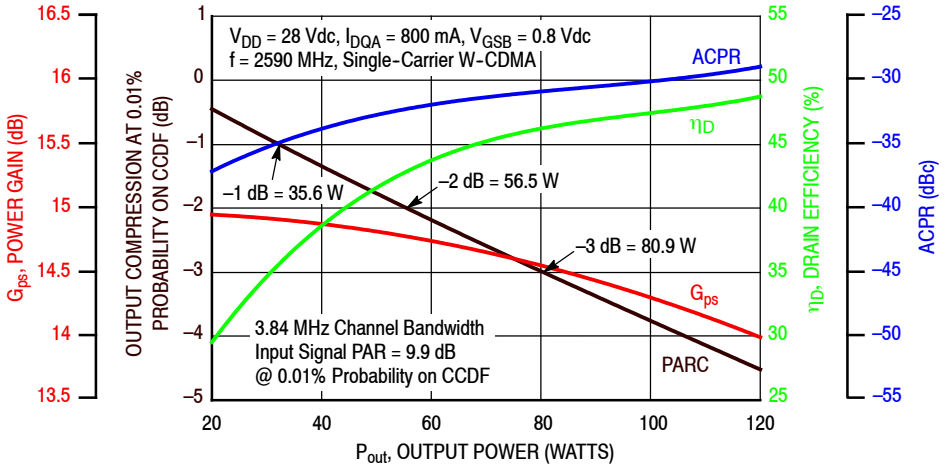


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

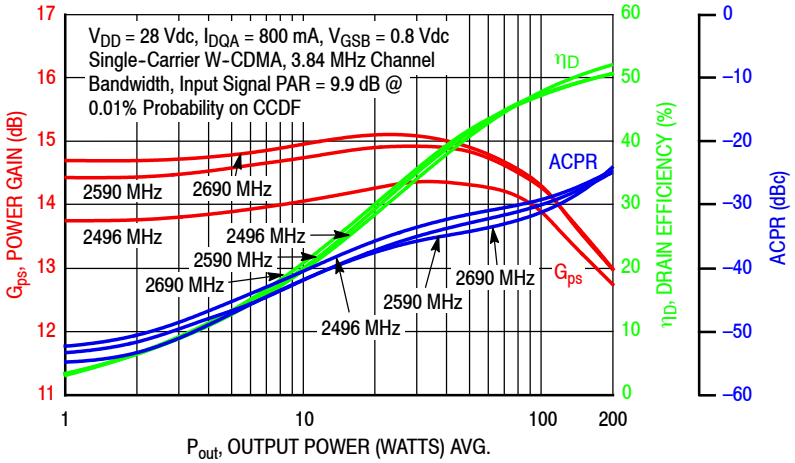


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

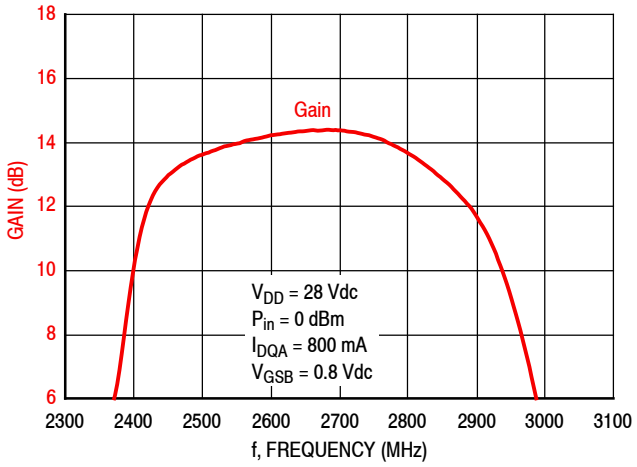


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 789 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.30 – j11.5	5.55 + j11.0	2.11 – j4.78	16.4	52.3	171	56.1	–12
2590	10.3 – j13.6	9.67 + j12.0	2.07 – j4.80	16.8	52.3	171	55.7	–13
2690	20.7 – j5.59	17.0 + j6.10	2.00 – j5.08	17.2	52.2	166	54.3	–14

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.30 – j11.5	5.42 + j11.9	1.97 – j4.97	14.1	53.1	204	56.5	–17
2590	10.3 – j13.6	10.2 + j13.7	1.97 – j5.09	14.5	53.0	201	55.3	–18
2690	20.7 – j5.59	20.0 + j6.30	1.95 – j5.29	14.9	52.9	194	54.1	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 789 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.30 – j11.5	5.44 + j11.6	4.68 – j3.61	18.8	50.7	117	65.9	–19
2590	10.3 – j13.6	9.41 + j12.8	3.87 – j2.92	19.3	50.6	114	65.0	–21
2690	20.7 – j5.59	17.1 + j7.04	3.14 – j3.24	19.5	50.7	117	63.3	–22

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	5.30 – j11.5	5.11 + j12.3	4.60 – j3.58	16.8	51.3	135	65.8	–26
2590	10.3 – j13.6	9.55 + j14.3	3.53 – j3.29	17.0	51.6	143	64.5	–28
2690	20.7 – j5.59	19.9 + j7.66	3.01 – j3.40	17.3	51.4	139	62.8	–29

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

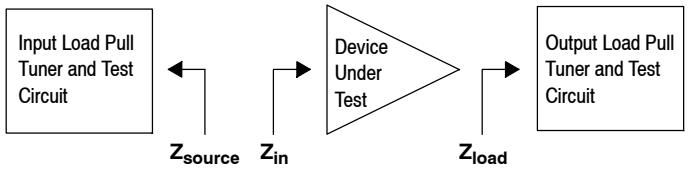


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.65 – j13.4	4.31 + j12.3	1.32 – j4.52	12.8	54.4	273	53.0	–26
2590	14.5 – j14.0	9.13 + j14.9	1.29 – j4.66	12.9	54.3	272	52.4	–25
2690	23.6 – j0.90	21.6 + j7.82	1.36 – j5.13	13.0	54.4	275	53.3	–27

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.65 – j13.4	4.39 + j12.9	1.27 – j4.62	10.6	54.9	310	53.7	–32
2590	14.5 – j14.0	10.0 + j15.9	1.29 – j4.80	10.8	54.9	309	52.7	–31
2690	23.6 – j0.90	24.0 + j5.56	1.38 – j5.30	10.9	55.0	313	53.7	–33

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

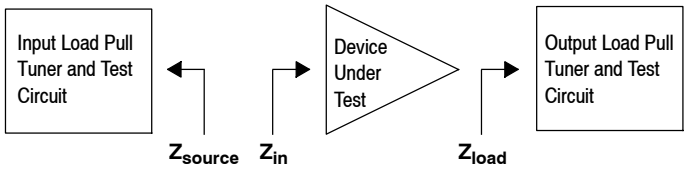
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.65 – j13.4	3.94 + j12.4	3.26 – j4.65	14.0	52.8	193	62.9	–35
2590	14.5 – j14.0	8.38 + j15.3	3.43 – j3.91	14.1	52.5	179	63.0	–36
2690	23.6 – j0.90	22.0 + j9.77	2.60 – j4.07	14.1	53.1	205	63.9	–36

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	6.65 – j13.4	4.14 + j12.9	2.87 – j4.85	11.9	53.6	229	61.9	–41
2590	14.5 – j14.0	9.48 + j16.2	3.01 – j4.32	12.0	53.5	224	61.7	–41
2690	23.6 – j0.90	24.7 + j7.38	2.60 – j4.22	12.1	53.7	235	62.8	–43

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2590 MHz

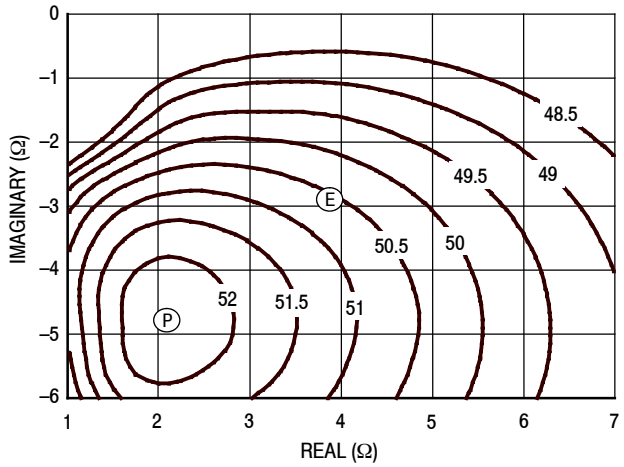


Figure 8. P1dB Load Pull Output Power Contours (dBm)

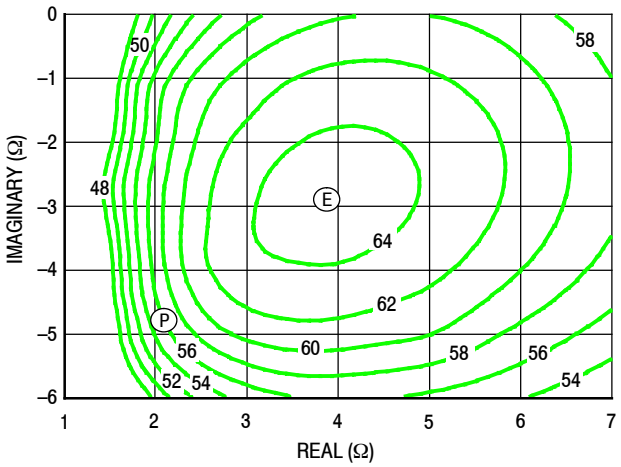


Figure 9. P1dB Load Pull Efficiency Contours (%)

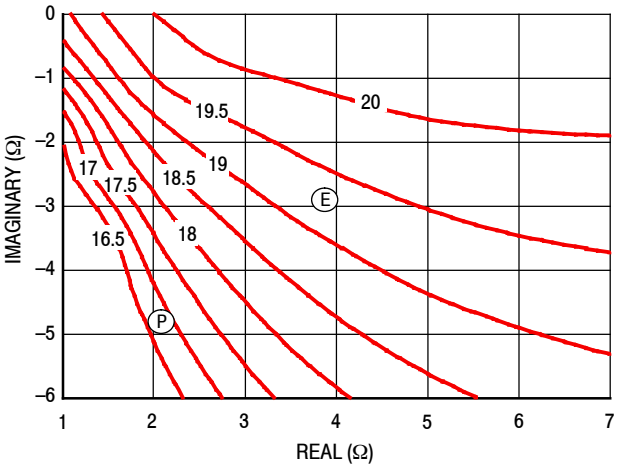


Figure 10. P1dB Load Pull Gain Contours (dB)

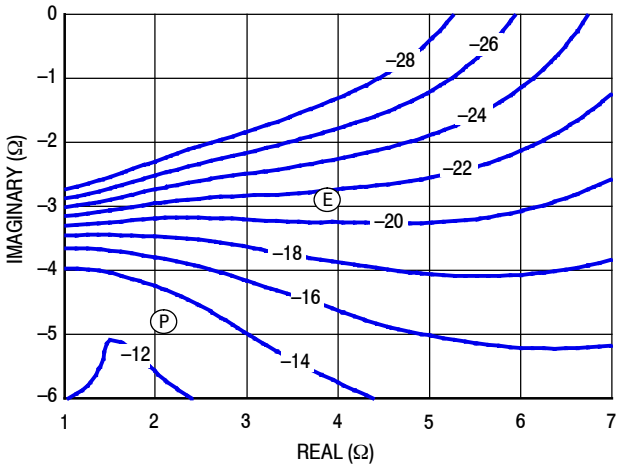


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2590 MHz

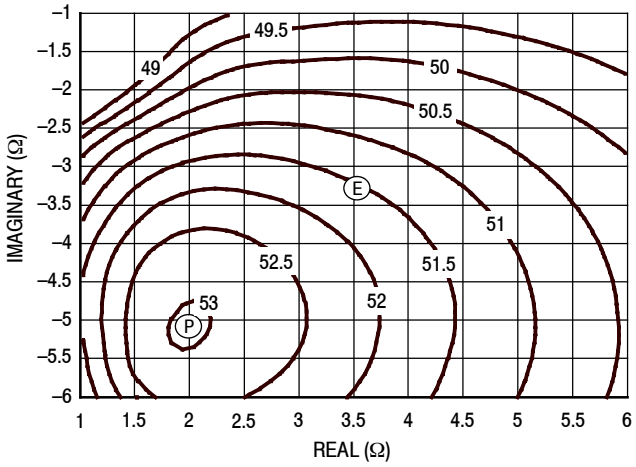


Figure 12. P3dB Load Pull Output Power Contours (dBm)

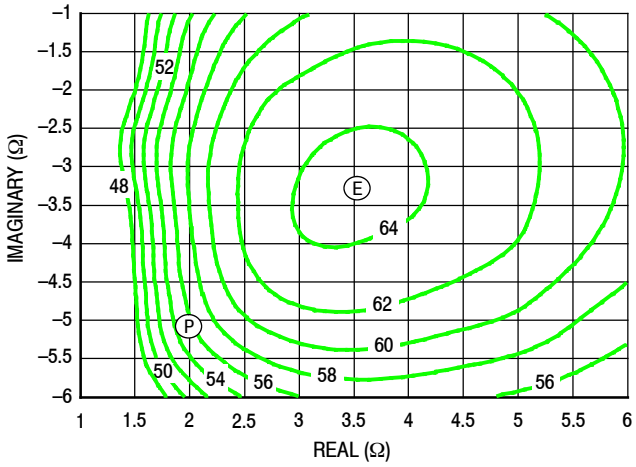


Figure 13. P3dB Load Pull Efficiency Contours (%)

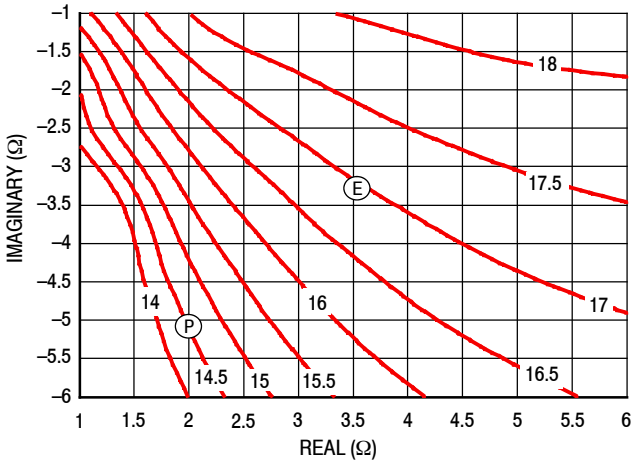


Figure 14. P3dB Load Pull Gain Contours (dB)

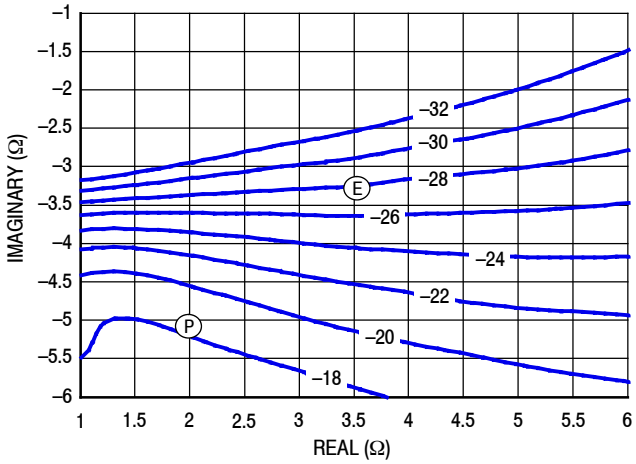


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

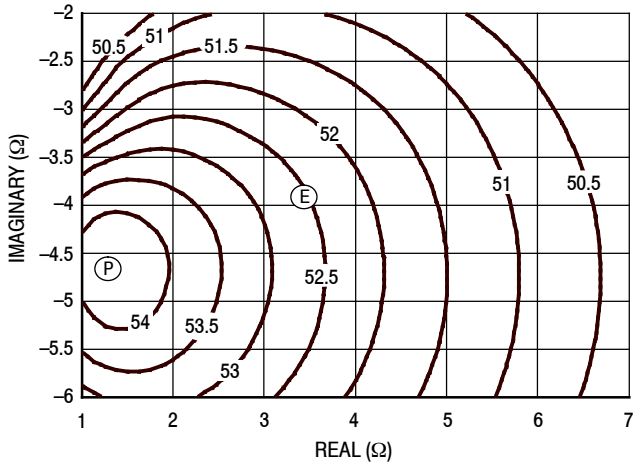


Figure 16. P1dB Load Pull Output Power Contours (dBm)

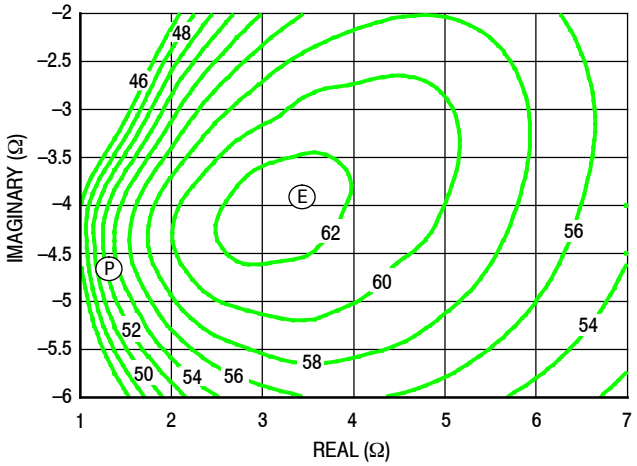


Figure 17. P1dB Load Pull Efficiency Contours (%)

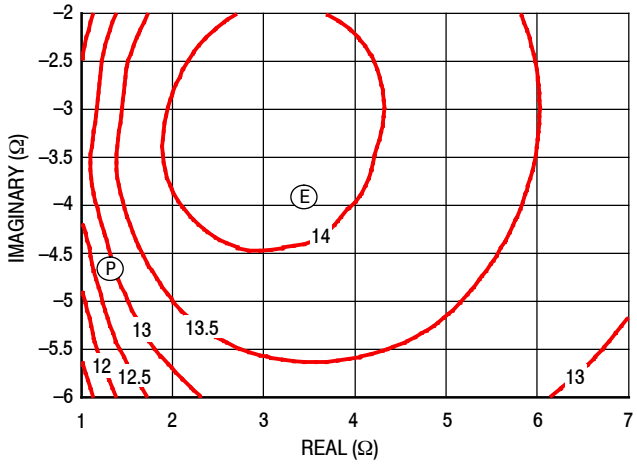


Figure 18. P1dB Load Pull Gain Contours (dB)

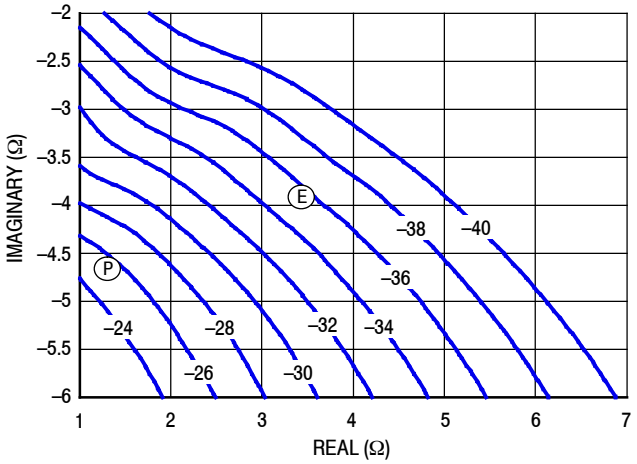


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

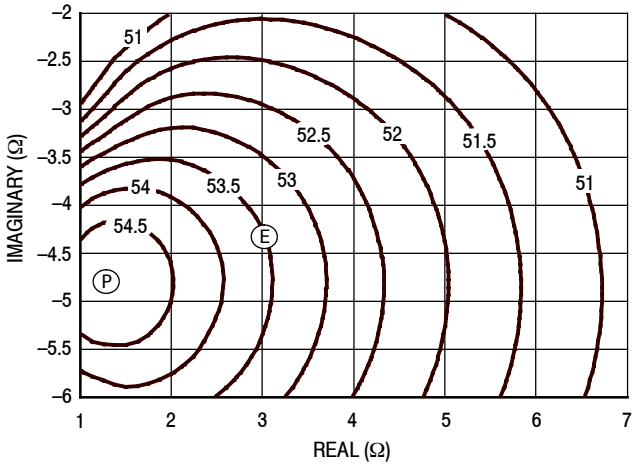


Figure 20. P3dB Load Pull Output Power Contours (dBm)

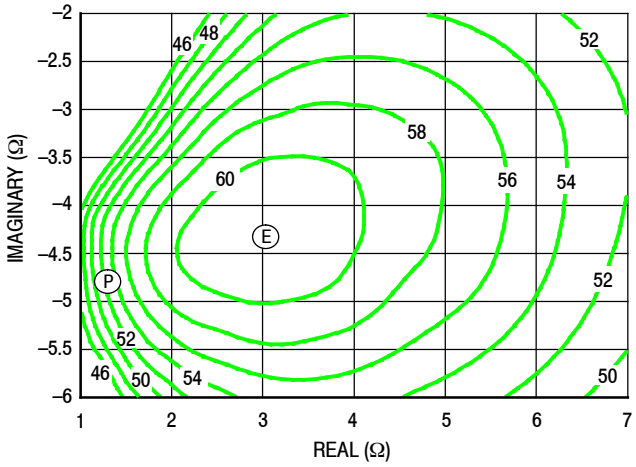


Figure 21. P3dB Load Pull Efficiency Contours (%)

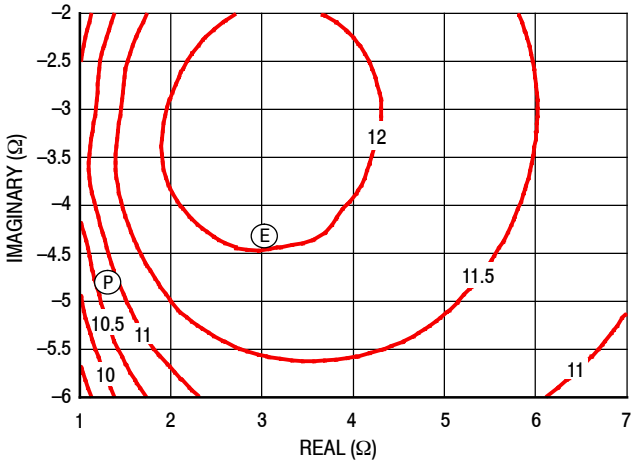


Figure 22. P3dB Load Pull Gain Contours (dB)

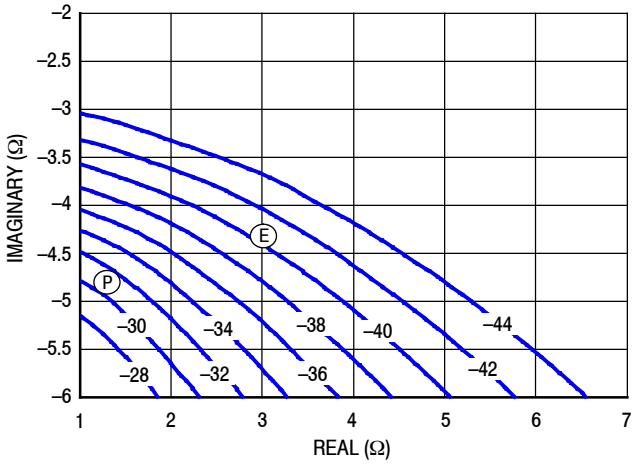


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

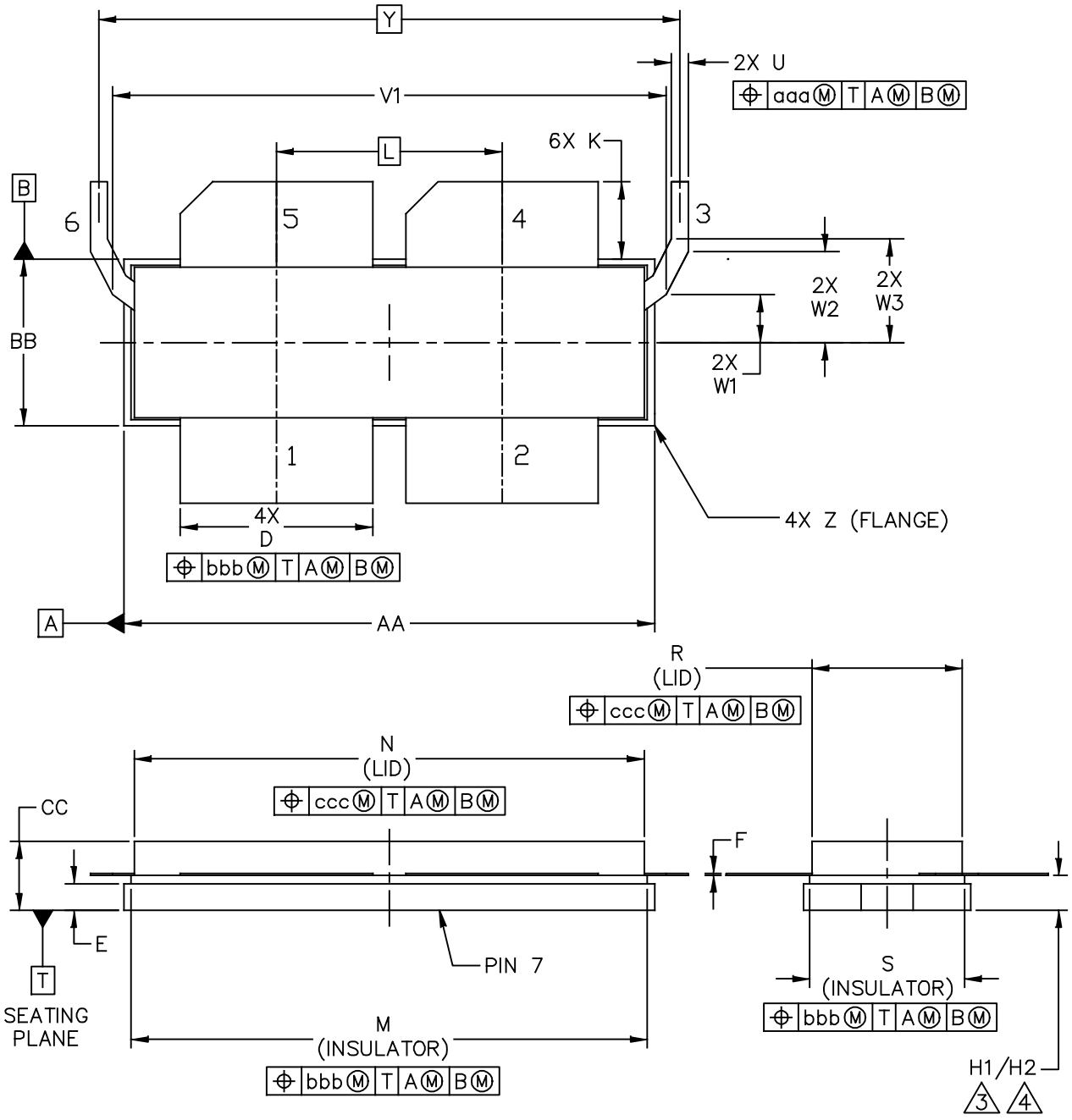
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2015	• Initial Release of Data Sheet

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