December 2004

FDM6296
Single N-Channel, Logic-Level, PowerTrench® MOSFET

Features

- 11.5 A, 30 V $R_{DS(ON)}$ = 10.5 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 15 mΩ @ V_{GS} = 4.5 V
- Low Qg, Qgd and Rg for efficient switching performance
- Low Profile – MicroFET 3.3 x 3.3 mm

Applications

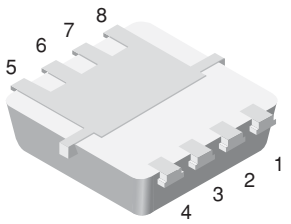
- Point of Load Converter
- 1/16 Brick Synchronous Rectifier

General Description

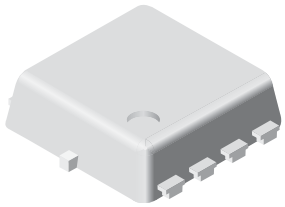
This single N-Channel MOSFET in the thermally efficient Micro-FET package has been specifically designed to perform well in Point of Load converters. Providing an optimized balance between Rds(on) and gate charge this device can be effectively used as a “high side” control switch or “low side” synchronous rectifier.

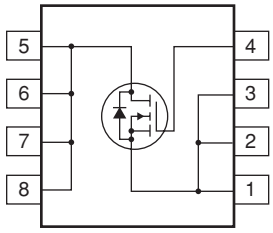
MicroFET

Bottom



Top





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	11.5	A
	– Pulsed		40	
P_D	Power Dissipation (Steady State)	(Note 1a)	2.5	W
		(Note 1b)	1.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	108	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6296	FDM6296	7”	12mm	3000 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		29		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 11.5 A V_{GS} = 4.5 V, I_D = 10 A V_{GS} = 10 V, I_D = 11.5A, T_J = 125°C		8.7 10.6 13	10.5 15 17	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D =11.5 A		47		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1507		pF
C_{oss}	Output Capacitance			415		pF
C_{rss}	Reverse Transfer Capacitance			128		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.1		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			27	44	ns
t_f	Turn–Off Fall Time			13	23	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 11.5 A, V_{GS} = 5 V		12	17	nC
Q_{gs}	Gate–Source Charge			4		nC
Q_{gd}	Gate–Drain Charge			3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.9	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 11.5 A, d_{iF}/d_t = 100 A/µs		29		nS
Q_{rr}	Diode Reverse Recovery Charge			20		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in_ 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   (a). $R_{\theta JA}$ = 52°C/W when mounted on a 1in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
   (b). $R_{\theta JA}$ = 108°C/W when mounted on a minimum pad of 2 oz copper
2. Pulse Test: Pulse Width < 300ms, Duty Cycle < 2.0%

Typical Characteristics

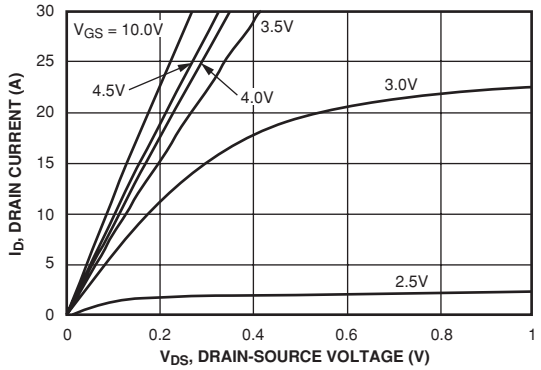


Figure 1. On-Region Characteristics

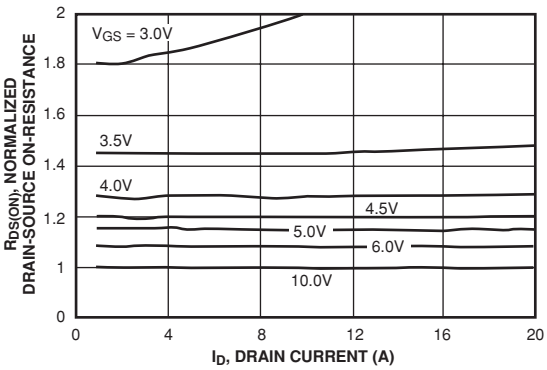


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

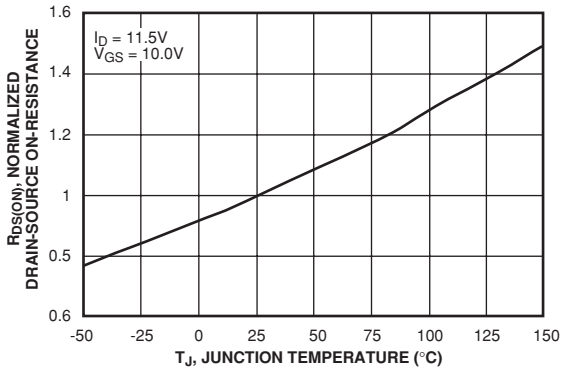


Figure 3. On-Resistance Variation with Temperature

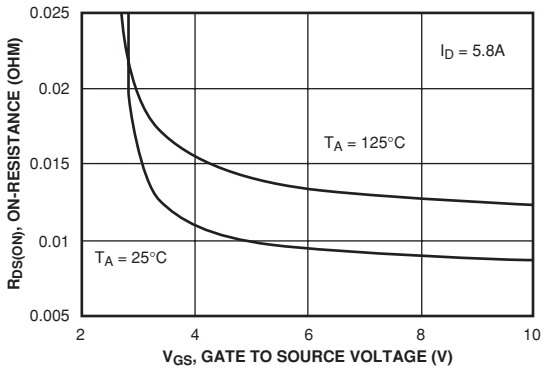


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

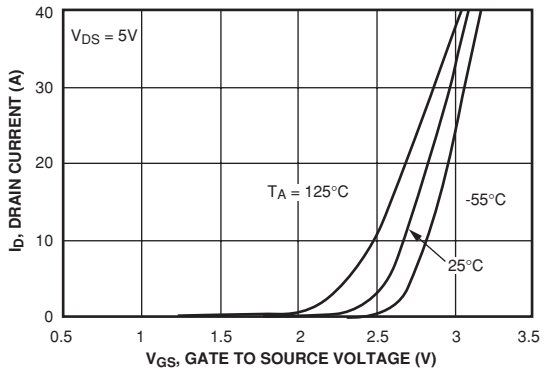


Figure 5. Transfer Characteristics

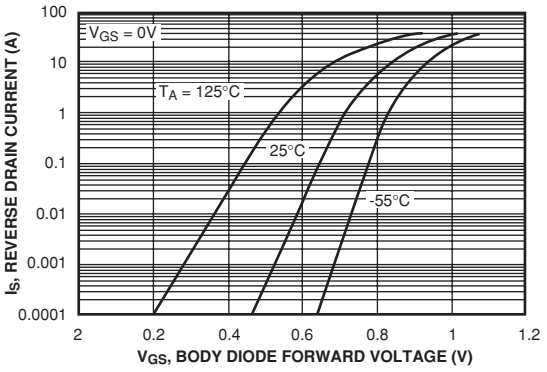


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

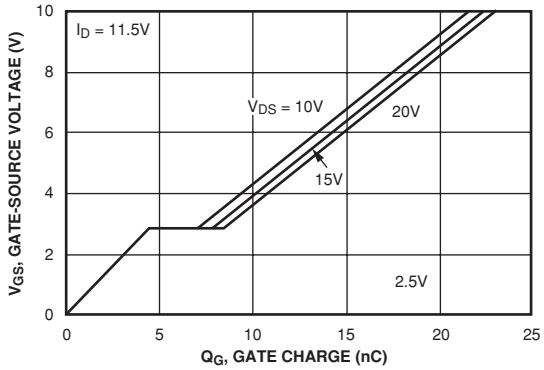


Figure 7. Gate Charge Characteristics

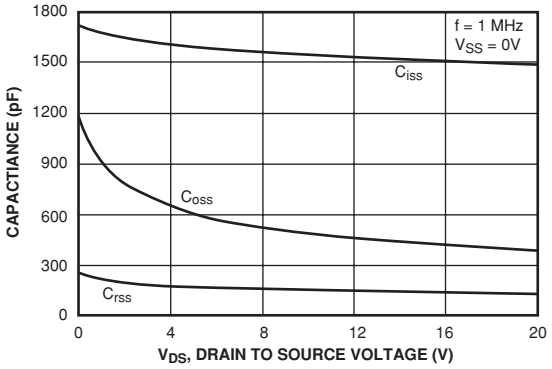


Figure 8. Capacitance Characteristics

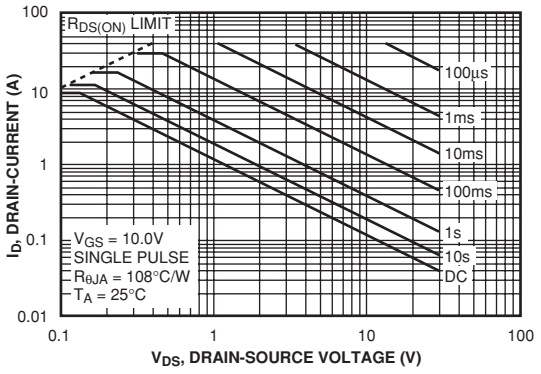


Figure 9. Maximum Safe Operating Area

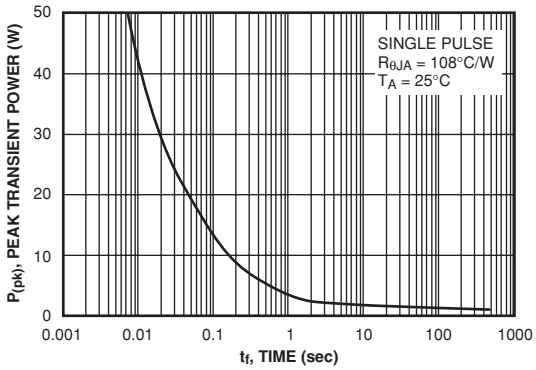


Figure 10. Single Pulse Maximum Power Dissipation

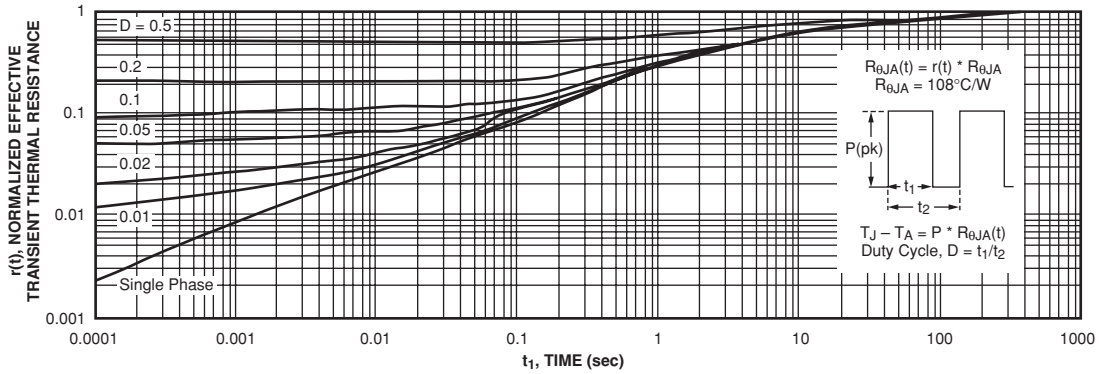
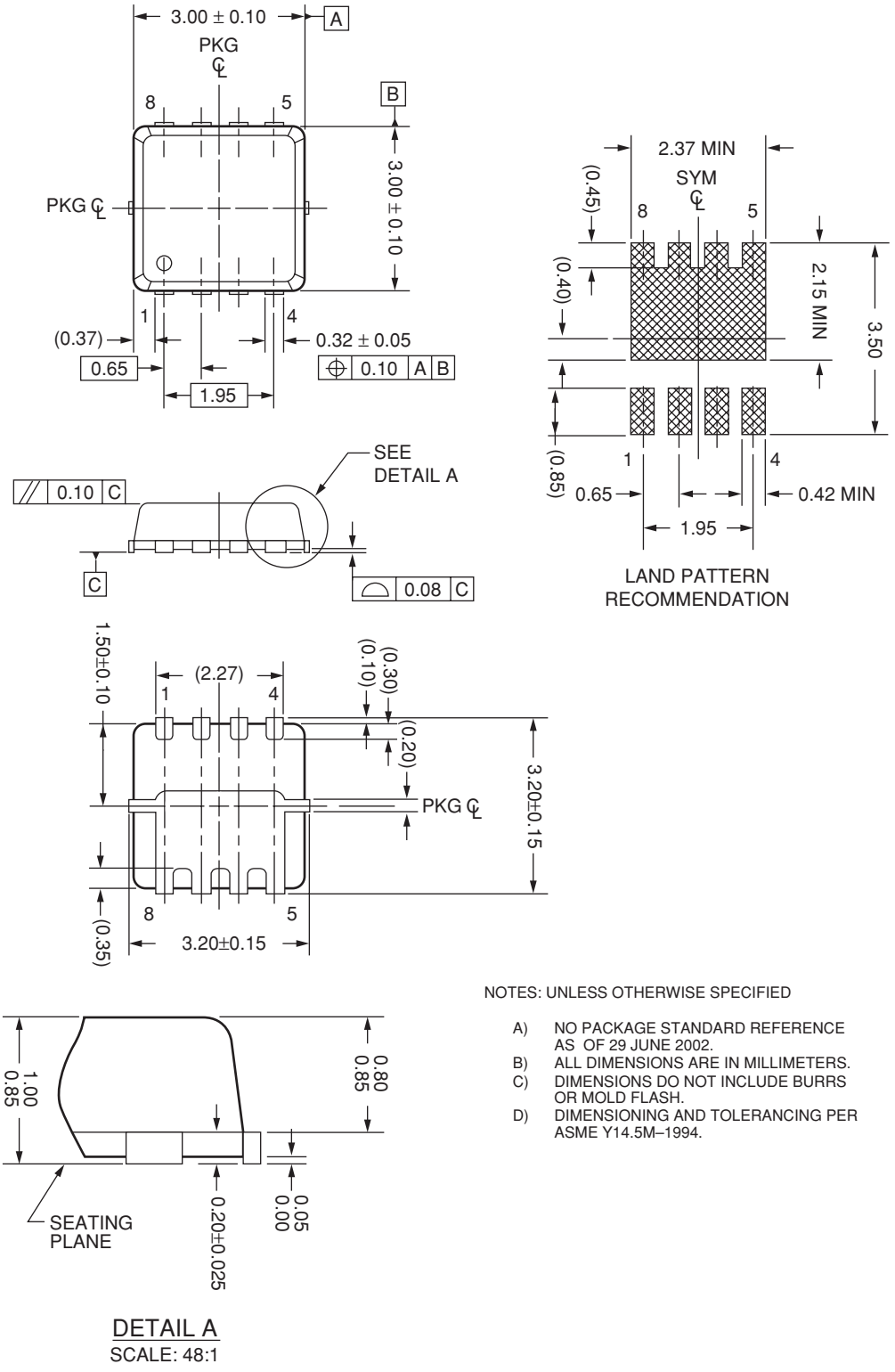


Figure 5. Transfer Characteristics

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

A) NO PACKAGE STANDARD REFERENCE AS OF 29 JUNE 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	Power247™	Stealth™
ActiveArray™	FASTr™	LittleFET™	PowerEdge™	SuperFET™
Bottomless™	FPS™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CoolFET™	FRFET™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QFET®	SuperSOT™-8
DOME™	GTO™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	HiSeC™	MSX™	QT Optoelectronics™	TinyLogic®
E²CMOS™	I²C™	MSXPro™	Quiet Series™	TINYOPTO™
EnSigna™	*i-Lo*™	OCX™	RapidConfigure™	TruTranslation™
FACT™	ImpliedDisconnect™	OCXPro™	RapidConnect™	UHC™
FACT Quiet Series™		OPTOLOGIC®	μSerDes™	UltraFET®
Across the board. Around the world.™		OPTOPLANAR™	SILENT SWITCHER®	UniFET™
The Power Franchise®		PACMAN™	SMART START™	VCX™
Programmable Active Droop™		POP™	SPM™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I14