



## 2.5-V/3.3-V OSCILLATOR GAIN STAGE/BUFFERS

### FEATURES

- Low-Voltage PECL Input and Low-Voltage PECL or LVDS Outputs
- Clock Rates to 2 GHz
  - 140-ps Output Transition Times
  - 0.11 ps Typical Intrinsic Phase Jitter
  - Less than 630 ps Propagation Delay Times
- 2.5-V or 3.3-V Supply Operation

- 2-mm × 2-mm Small-Outline No-Lead Package

### APPLICATIONS

- PECL-to-LVDS Translation
- Clock Signal Amplification

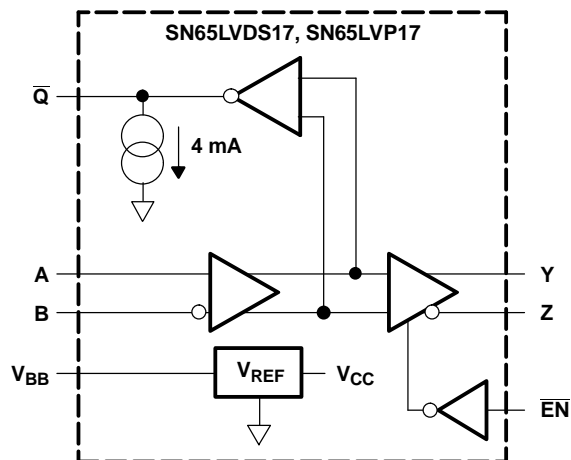
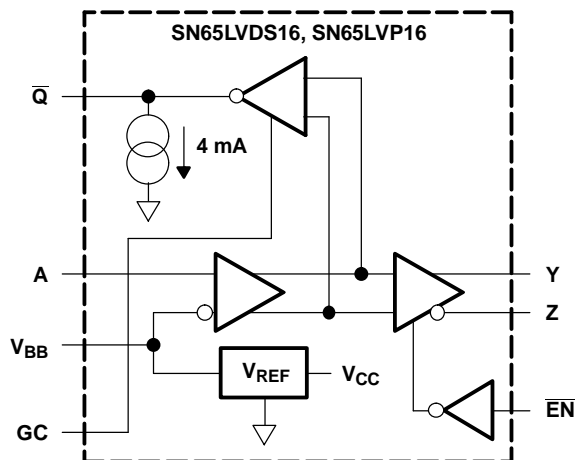
### DESCRIPTION

These four devices are high-frequency oscillator gain stages supporting both LVPECL or LVDS on the high gain outputs in 3.3-V or 2.5-V systems. Additionally, provides the option of both single-ended input (PECL levels on the SN65LVx16) and fully differential inputs on the SN65LVx17.

The SN65LVx16 provides the user a Gain Control (GC) for controlling the  $\bar{Q}$  output from 300 mV to 860 mV either by leaving it open (NC), grounded, or tied to  $V_{CC}$ . (When left open, the  $\bar{Q}$  output defaults to 575 mV.) The  $\bar{Q}$  on the SN65LVx17 defaults to 575 mV as well.

Both devices provide a voltage reference ( $V_{BB}$ ) of typically 1.35 V below  $V_{CC}$  for use in receiving single-ended PECL input signals. When not used,  $V_{BB}$  should be unconnected or open.

All devices are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### AVAILABLE OPTIONS<sup>(1)</sup>

INPUT	OUTPUT	GAIN CONTROL	BASE PART NUMBER	PART MARKING
Single-ended	LVDS	Yes	SN65LVDS16	EL
Single-ended	LVPECL	Yes	SN65LVP16	EK
Differential	LVDS	No	SN65LVDS17	EN
Differential	LVPECL	No	SN65LVP17	EM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	UNIT
$V_{CC}$ Supply voltage <sup>(2)</sup>	–0.5 V to 4 V
$V_I$ Input voltage	–0.5 V to $V_{CC} + 0.5$ V
$V_O$ Output voltage	–0.5 V to $V_{CC} + 0.5$ V
$I_O$ $V_{BB}$ output current	±0.5 mA
HBM electrostatic discharge <sup>(3)</sup>	±3 kV
CDM electrostatic discharge <sup>(4)</sup>	±1500 V
Continuous power dissipation	See Power Dissipation Ratings Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground see [Figure 1](#)).

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A-7

(4) Tested in accordance with JEDEC Standard 22, Test Method C101

### DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ <sup>(1)</sup>	$T_A = 85^\circ\text{C}$ POWER RATING
DRF	Low-K <sup>(2)</sup>	403 mW	4.0 mW/°C	161 mW
	High-K <sup>(3)</sup>	834 mW	8.3 mW/°C	333 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

### THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT	
$\theta_{JB}$	Junction-to-board thermal resistance		93.3	°C/W	
$\theta_{JC}$	Junction-to-case thermal resistance		101.7		
$P_D$	Device power dissipation	Typical	$V_{CC} = 3.3\text{ V}$ , $T_A = 25^\circ\text{C}$ , 2 GHz, LVDS	132	mW
			$V_{CC} = 3.3\text{ V}$ , $T_A = 25^\circ\text{C}$ , 2 GHz, LVPECL	83	
	Maximum	$V_{CC} = 3.6\text{ V}$ , $T_A = 85^\circ\text{C}$ , 2 GHz, LVDS	173		
		$V_{CC} = 3.6\text{ V}$ , $T_A = 85^\circ\text{C}$ , 2 GHz, LVPECL	108		

## RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		2.375	2.5 or 3.3	3.6	V
$V_{IC}$	Common-mode input voltage ( $V_{IA} + V_{IB}$ )/2	SN65LVDS17 or SN65LVP17	1.2	$V_{CC} - (V_{ID}/2)$		V
$ V_{ID} $	Differential input voltage magnitude $ V_{IA} - V_{IB} $	SN65LVDS17 or SN65LVP17	0.08		1	V
$V_{IH}$	High-level input voltage to $\overline{EN}$	$\overline{EN}$			$V_{CC}$	V
		SN65LVDS16 or SN65LVP16	$V_{CC} - 1.17$		$V_{CC} - 0.44$	
$V_{IL}$	Low-level input voltage to $\overline{EN}$	$\overline{EN}$	0		0.8	V
		SN65LVDS16 or SN65LVP16	$V_{CC} - 2.25$		$V_{CC} - 1.52$	
$I_O$	Output current to $V_{BB}$		$-400^{(1)}$		400	$\mu A$
$R_L$	Differential load resistance,		90		132	$\Omega$
$T_A$	Operating free-air temperature		-40		85	$^{\circ}C$

(1) The algebraic convention, where the least positive (more negative) value is designated minimum, is used in this data sheet.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>CC</sub>	Supply current	R <sub>L</sub> = 100 Ω, $\overline{EN}$ at 0 V, Other inputs open		40	48	mA
		Outputs unloaded, $\overline{EN}$ at 0 V, Other inputs open		25	30	
V <sub>BB</sub>	Reference voltage <sup>(2)</sup>	I <sub>BB</sub> = −400 μA	V <sub>CC</sub> − 1.44	V <sub>CC</sub> − 1.35	V <sub>CC</sub> − 1.25	V
I <sub>IH</sub>	High-level input current, $\overline{EN}$	V <sub>I</sub> = 2 V	−20		20	μA
I <sub>IAH</sub> or I <sub>IBH</sub>	High-level input current, A or B	V <sub>I</sub> = V <sub>CC</sub>	−20		20	
I <sub>IL</sub>	Low-level input current, $\overline{EN}$	V <sub>I</sub> = 0.8 V	−20		20	
I <sub>IAL</sub> or I <sub>IBL</sub>	Low-level input current, A or B	V <sub>I</sub> = GND	−20		20	
SN65LVDS16/17 Y AND Z OUTPUT CHARACTERISTICS						
V <sub>OD</sub>	Differential output voltage magnitude,  V <sub>OY</sub> − V <sub>OZ</sub>	See Figure 1 and Figure 2	247	340	454	mV
Δ V <sub>OD</sub>	Change in differential output voltage magnitude between logic states				50	
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage (see Figure 3)			1.125		1.375
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage between logic states	See Figure 3	−50		50	mV
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage				50	
I <sub>OYZ</sub> or I <sub>OZZ</sub>	High-impedance output current	$\overline{EN}$ at V <sub>CC</sub> , V <sub>O</sub> = 0 V or V <sub>CC</sub>	−1		1	μA
I <sub>OYS</sub> or I <sub>OZS</sub>	Short-circuit output current	$\overline{EN}$ at 0 V, V <sub>OY</sub> or V <sub>OZ</sub> = 0 V	−62		62	mA
I <sub>OS(D)</sub>	Differential short-circuit output current,  I <sub>OY</sub> − I <sub>OZ</sub>	$\overline{EN}$ at 0 V, V <sub>OY</sub> = V <sub>OZ</sub>	−12		12	

(1) Typical values are at room temperature and with a  $V_{CC}$  of 3.3 V.

(2) Single-ended input operation is limited to  $V_{CC} \geq 3.0 V$ .

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>SN65LVP16/17 Y AND Z OUTPUT CHARACTERISTICS</b>						
V <sub>OYH</sub> or V <sub>OZH</sub>	High-level output voltage	3.3 V; 50 Ω from Y and Z to V <sub>CC</sub> – 2 V	V <sub>CC</sub> – 1.05		V <sub>CC</sub> – 0.82	V
V <sub>OYL</sub> or V <sub>OZL</sub>	Low-level output voltage		V <sub>CC</sub> – 1.83		V <sub>CC</sub> – 1.57	
V <sub>OYL</sub> or V <sub>OZL</sub>	Low-level output voltage	2.5 V; 50 Ω from Y and Z to V <sub>CC</sub> – 2 V	V <sub>CC</sub> – 1.88		V <sub>CC</sub> – 1.57	
V <sub>OD</sub>	Differential output voltage magnitude,  V <sub>OH</sub> – V <sub>OL</sub>		0.6	0.8	1	
I <sub>OYZ</sub> or I <sub>OZZ</sub>	High-impedance output current	EN at V <sub>CC</sub> , V <sub>O</sub> = 0 V or V <sub>CC</sub>	–1		1	μA
<b>Q̄ OUTPUT CHARACTERISTICS (see Figure 1)</b>						
V <sub>OH</sub>	High-level output voltage	No load		V <sub>CC</sub> – 0.94		V
V <sub>OL</sub>	Low-level output voltage	GC Tied to GND, No load		V <sub>CC</sub> – 1.22		V
		GC Open, No load		V <sub>CC</sub> – 1.52		
		GC Tied to V <sub>CC</sub> , No load		V <sub>CC</sub> – 1.82		
V <sub>O(pp)</sub>	Peak-to-peak output voltage	GC Tied to GND		300		mV
		GC Open		575		
		GC Tied to V <sub>CC</sub>		860		

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PD</sub>	Propagation delay time, t <sub>PLH</sub> or t <sub>PHL</sub>	A to Q̄		340	460	ps
		D to Y or Z		460	630	
t <sub>SK(P)</sub>	Pulse skew,  t <sub>PLH</sub> – t <sub>PHL</sub>	See Figure 4			20	
t <sub>SK(PP)</sub>	Part-to-part skew <sup>(2)</sup>	V <sub>CC</sub> = 3.3 V			80	ps
		V <sub>CC</sub> = 2.5 V			130	
t <sub>r</sub>	20%-to-80% differential signal rise time	See Figure 4		85	140	ps
t <sub>f</sub>	20%-to-80% differential signal fall time			85	140	ps
t <sub>jit(per)</sub>	RMS period jitter <sup>(3)</sup>	2-GHz 50%-duty-cycle square-wave input, See Figure 5		2	3	ps
t <sub>jit(cc)</sub>	Peak cycle-to-cycle jitter <sup>(4)</sup>			15	23	
t <sub>jit(ph)</sub>	Intrinsic phase jitter	2 GHz		0.11		ps
t <sub>PHZ</sub>	Propagation delay time, high-level-to-high-impedance output	See Figure 6			30	ns
t <sub>PLZ</sub>	Propagation delay time, low-level-to-high-impedance output				30	
t <sub>PZH</sub>	Propagation delay time, high-impedance-to-high-level output				30	
t <sub>PZL</sub>	Propagation delay time, high-impedance-to-low-level output				30	

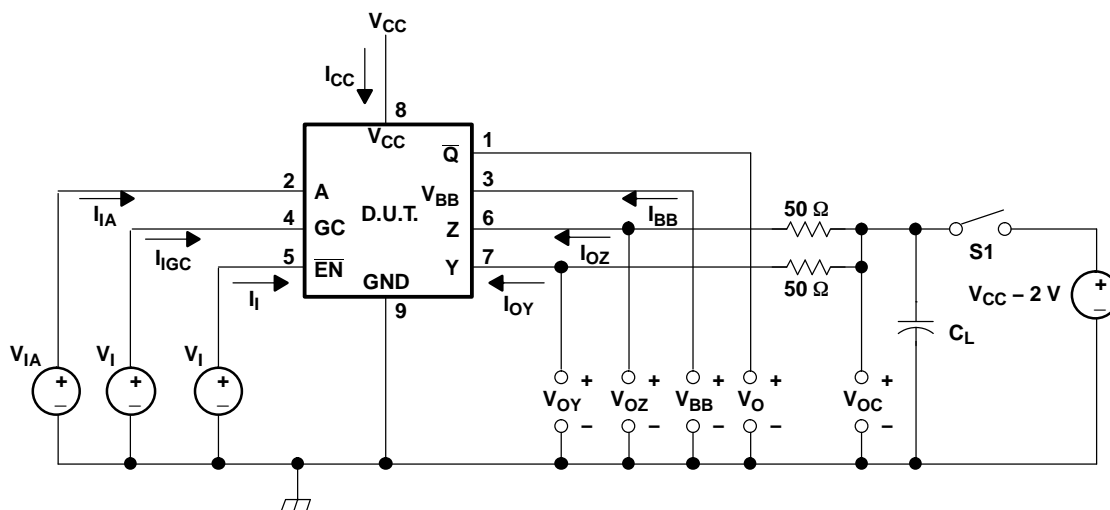
(1) Typical values are at room temperature and with a V<sub>CC</sub> of 3.3 V.

(2) Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.

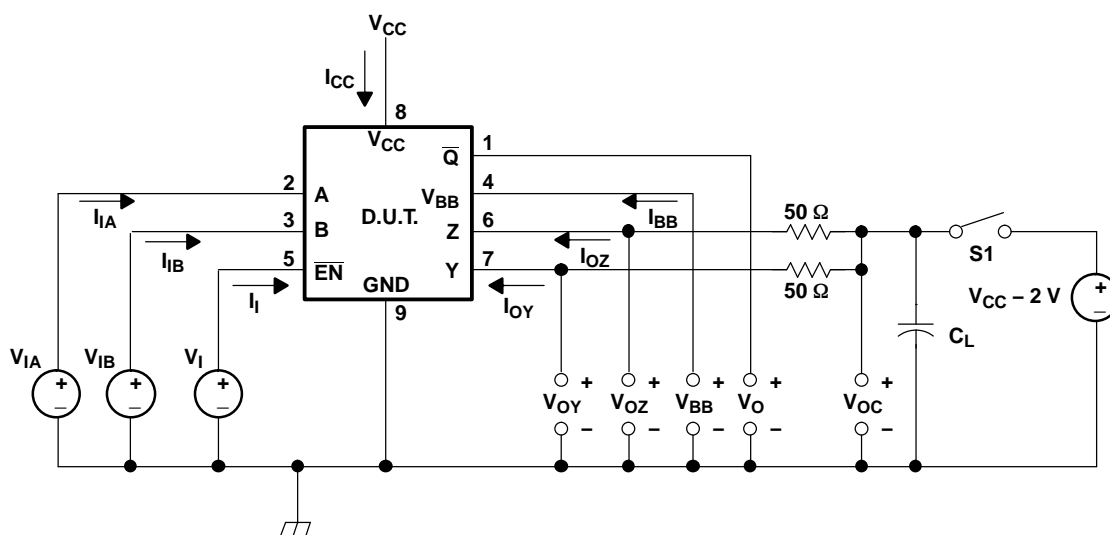
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.

## PARAMETER MEASUREMENT INFORMATION



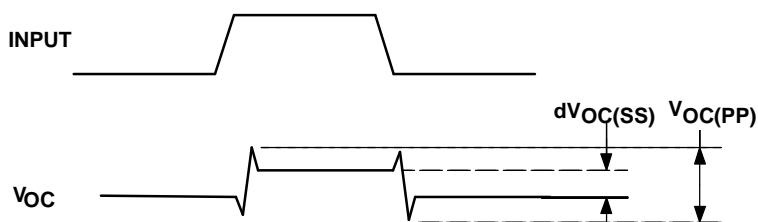
- (1)  $C_L$  is the instrumentation and test fixture capacitance.
- (2) S1 is open for the SN65LVDS16 and closed for the SN65LVP16.

**Figure 1. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP16**



- (1)  $C_L$  is the instrumentation and test fixture capacitance.
- (2) S1 is open for the SN65LVDS17 and closed for the SN65LVP17.

**Figure 2. Output Voltage Test Circuit and Voltage and Current Definitions for LVDS/LVP17**



**Figure 3.  $V_{OC}$  Definitions**

## PARAMETER MEASUREMENT INFORMATION (continued)

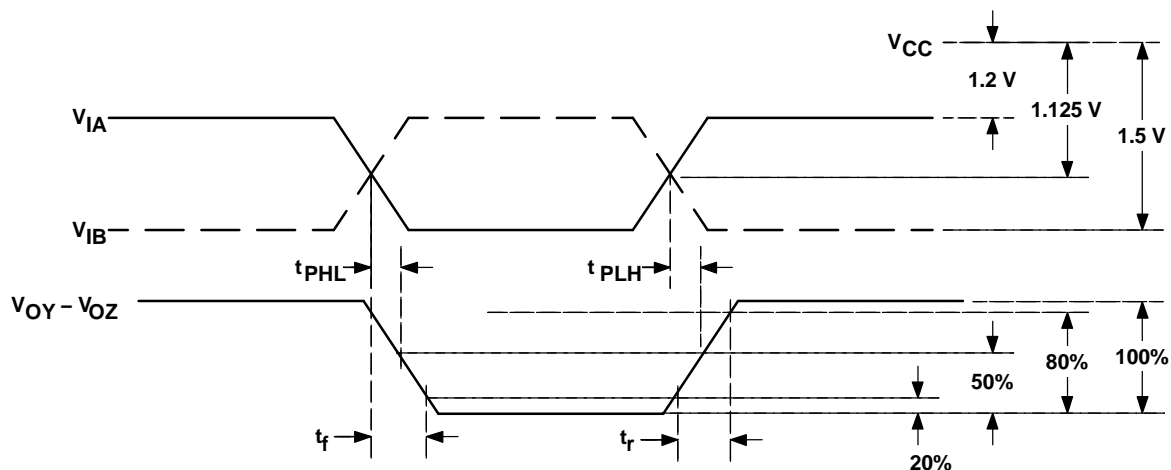


Figure 4. Propagation Delay and Transition Time Test Waveforms

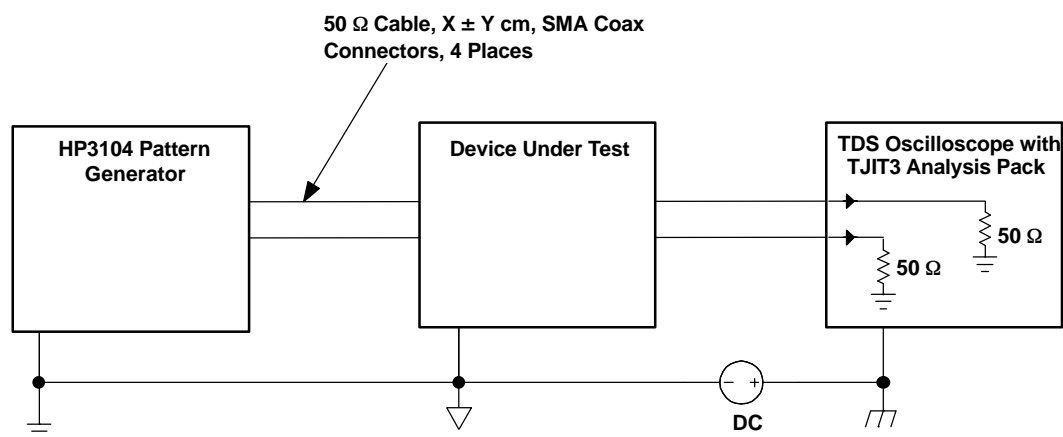


Figure 5. Jitter Measurement Setup

PARAMETER MEASUREMENT INFORMATION (continued)

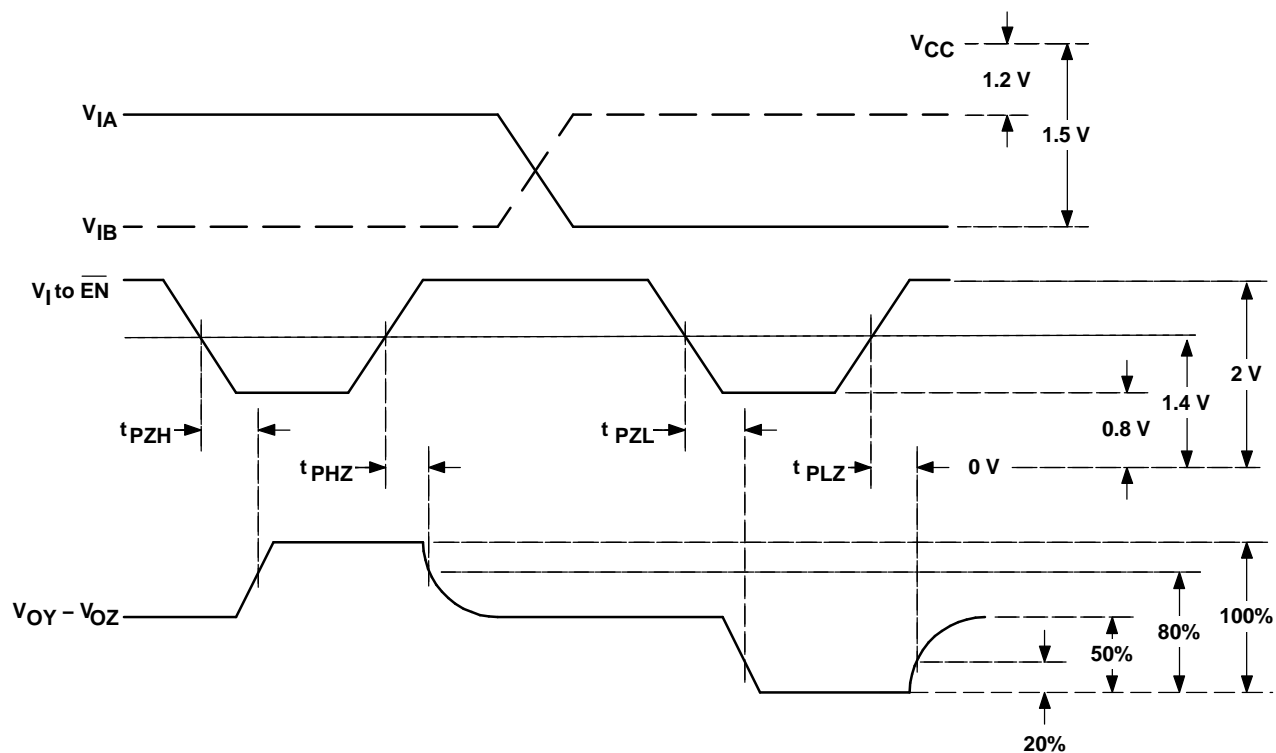


Figure 6. Enable and Disable Time Test Waveforms

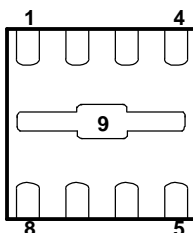
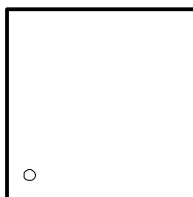
## DEVICE INFORMATION

### FUNCTION TABLE

SN65LVDS16, SN65LVP16 <sup>(1)</sup>					SN65LVDS17, SN65LVP17 <sup>(1)</sup>					
A	$\overline{\text{EN}}$	$\overline{\text{Q}}$	Y	Z	A	B	$\overline{\text{EN}}$	$\overline{\text{Q}}$	Y	Z
H	L	L	H	L	H	H	L	?	?	?
L	L	H	L	H	L	H	L	H	L	H
X	H	?	Z	Z	H	L	L	L	H	L
Open	L	?	?	?	L	L	L	?	?	?
X	Open	?	?	?	X	X	H	?	Z	Z
					Open	Open	L	?	?	?
					X	X	Open	?	?	?

(1) H = high, L = low, Z = high impedance, ? = indeterminate

### DRF PACKAGE TOP VIEW



### BOTTOM VIEW

### Package Pin Assignments - Numerical Listing

SN65LVDS16, SN65LVP16		SN65LVDS17, SN65LVP17	
PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{Q}}$	1	$\overline{\text{Q}}$
2	A	2	A
3	$V_{\text{BB}}$	3	B
4	GC	4	$V_{\text{BB}}$
5	$\overline{\text{EN}}$	5	$\overline{\text{EN}}$
6	Z	6	Z
7	Y	7	Y
8	$V_{\text{CC}}$	8	$V_{\text{CC}}$
9	GND	9	GND



## TYPICAL CHARACTERISTICS

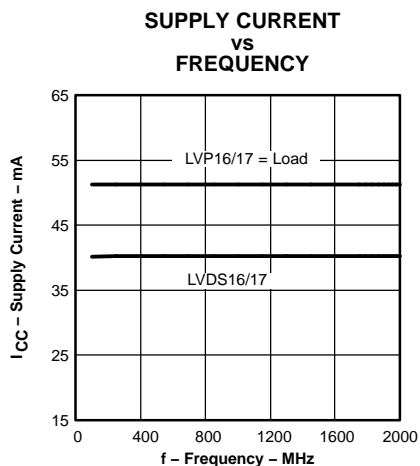


Figure 7.

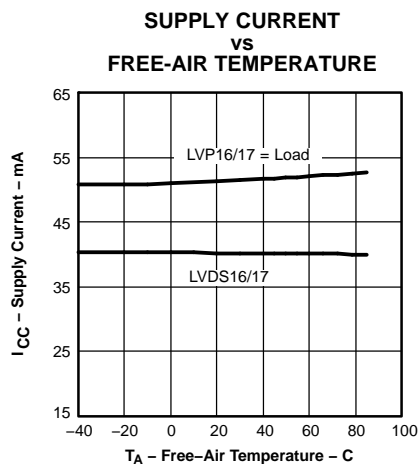


Figure 8.

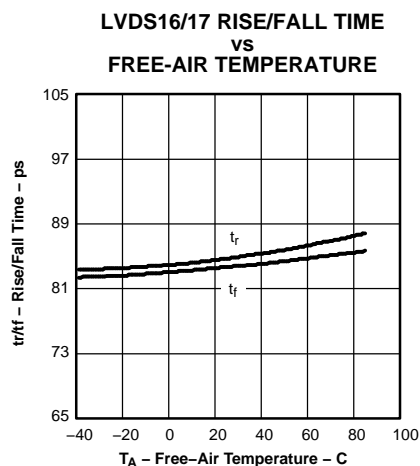


Figure 9.

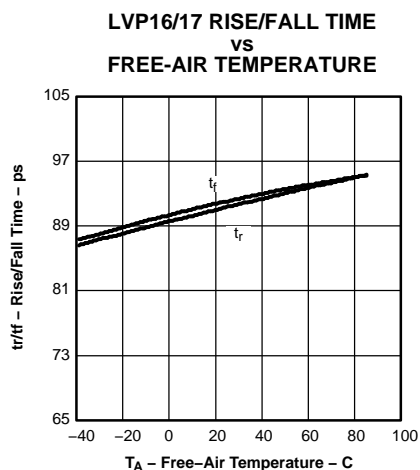


Figure 10.

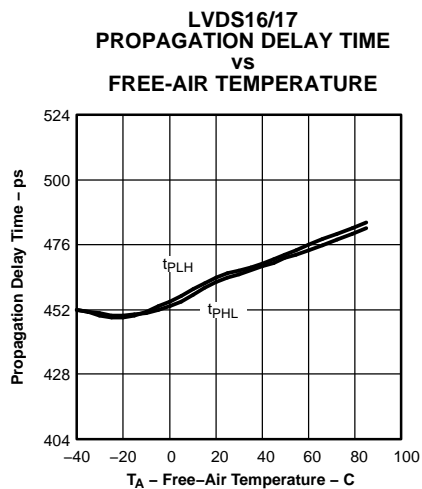


Figure 11.

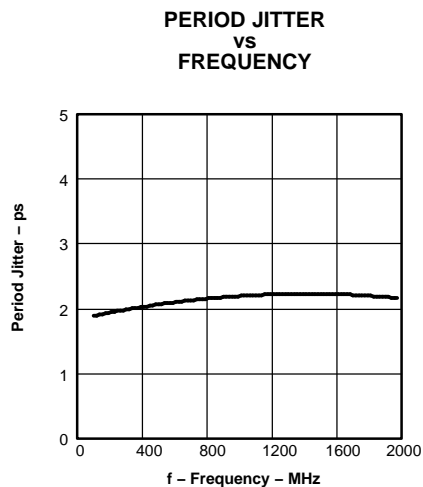


Figure 12.

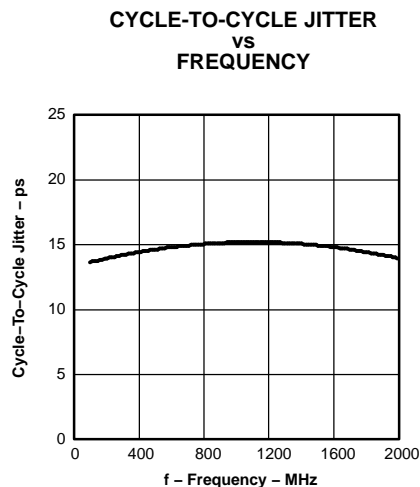
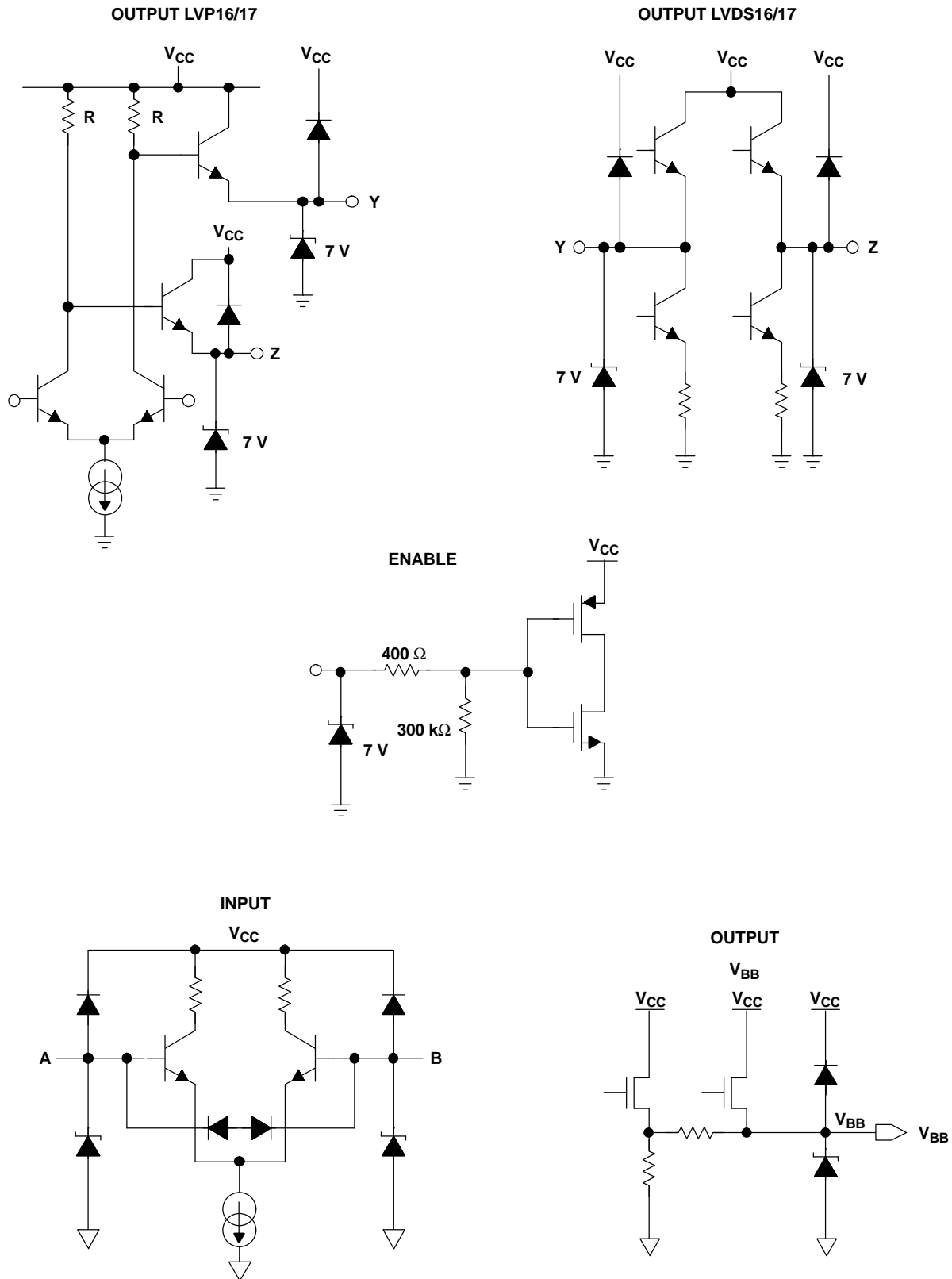


Figure 13.

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

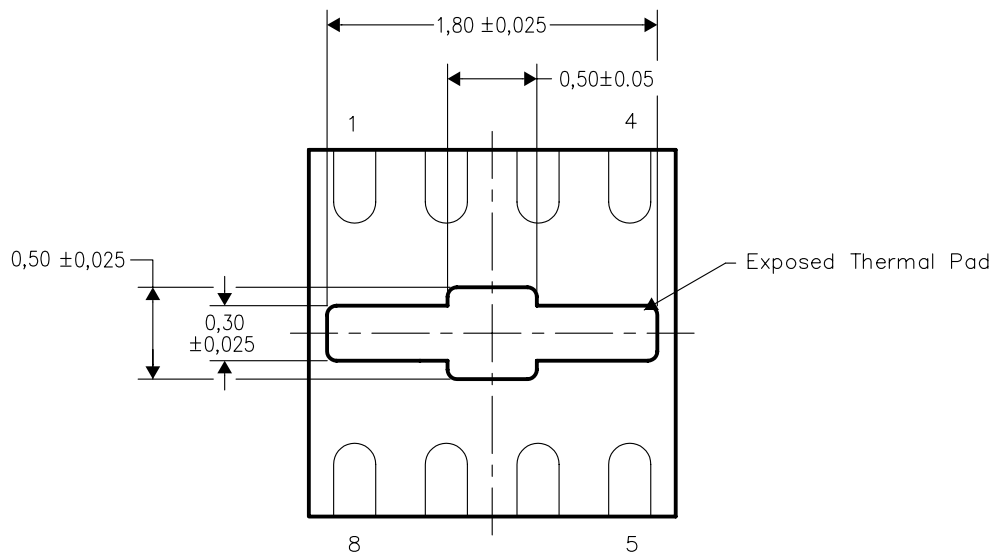


## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

## Exposed Thermal Pad Dimensions

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65LVDS16DRFR	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS16DRFRG4	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS16DRFT	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS16DRFTG4	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS17DRFR	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS17DRFRG4	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS17DRFT	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS17DRFTG4	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP16DRFR	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP16DRFRG4	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP16DRFT	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP16DRFTG4	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP17DRFR	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP17DRFRG4	ACTIVE	WSO	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP17DRFT	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVP17DRFTG4	ACTIVE	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS16DRFR	WSO	DRF	8	3000	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVDS16DRFT	WSO	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVDS17DRFR	WSO	DRF	8	3000	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVDS17DRFT	WSO	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP16DRFR	WSO	DRF	8	3000	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP16DRFT	WSO	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP17DRFR	WSO	DRF	8	3000	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2
SN65LVP17DRFT	WSO	DRF	8	250	330.0	8.8	2.3	2.3	1.0	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

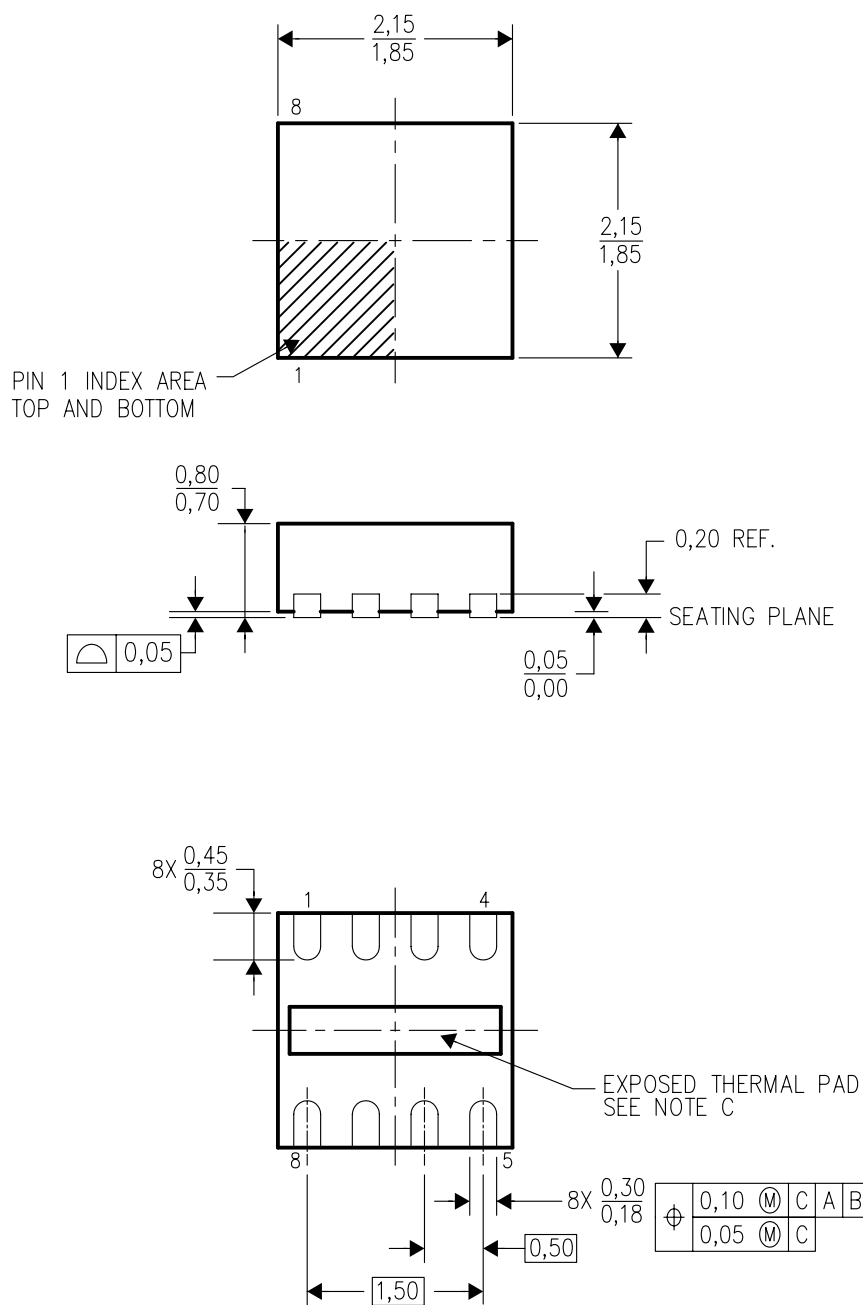


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS16DRFR	WSON	DRF	8	3000	337.0	343.0	29.0
SN65LVDS16DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVDS17DRFR	WSON	DRF	8	3000	337.0	343.0	29.0
SN65LVDS17DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP16DRFR	WSON	DRF	8	3000	337.0	343.0	29.0
SN65LVP16DRFT	WSON	DRF	8	250	337.0	343.0	29.0
SN65LVP17DRFR	WSON	DRF	8	3000	337.0	343.0	29.0
SN65LVP17DRFT	WSON	DRF	8	250	337.0	343.0	29.0

DRF (S-PDSO-N8)

PLASTIC SMALL OUTLINE



4205287/D 07/05

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
  - D. Falls within JEDEC MO-229.

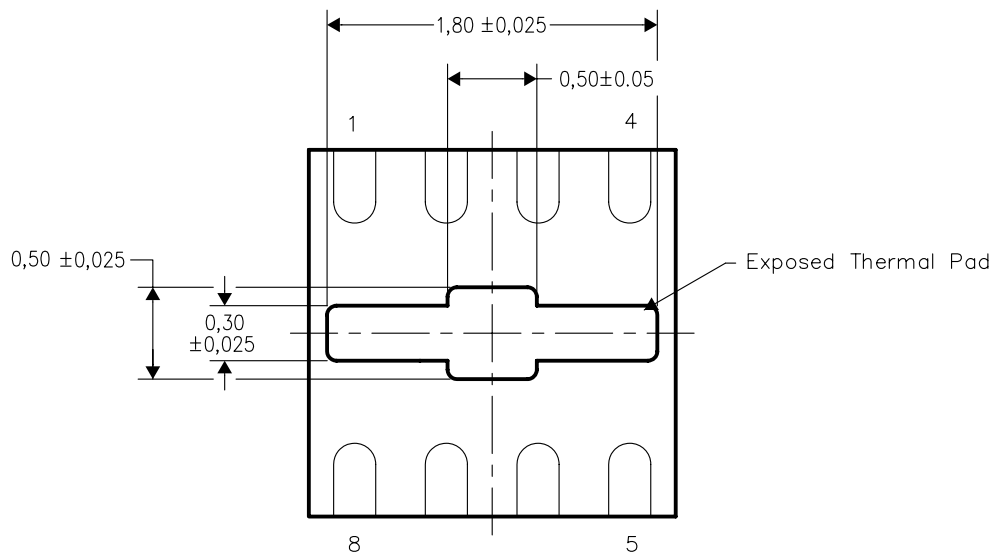


## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

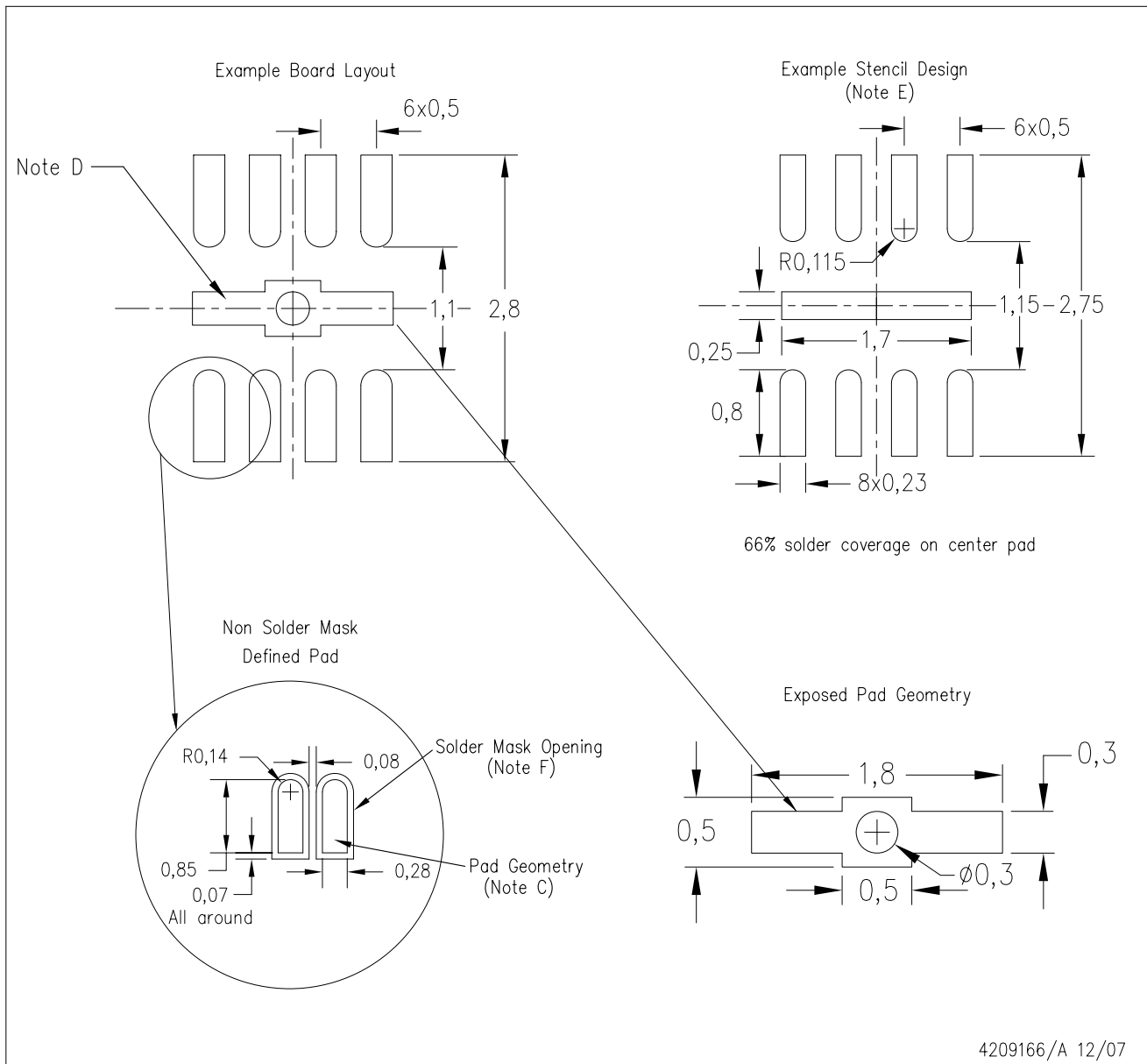


Bottom View

NOTE: All linear dimensions are in millimeters

## Exposed Thermal Pad Dimensions

DRF (S-PDSO-N8)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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