

3.3 V, 32K/64K × 16/18 Dual-Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- 32K × 16 organization (CY7C027V/027AV^[1])
- 64K × 16 organization (CY7C028V/028AV^[1])
- 32K × 18 organization (CY7C037AV)
- 64K × 18 organization (CY7C038V)
- 0.35 micron Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- High speed access: 15, 20, and 25 ns
- Low operating power
- Active: $I_{CC} = 115$ mA (typical)
- Standby: $I_{SB3} = 10$ μ A (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 32/36 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- INT flag for port-to-port communication
- Separate upper-byte and lower-byte control
- Dual chip enables
- Pin select for Master or Slave
- Commercial and Industrial temperature ranges
- 100-pin Pb-free Thin quad plastic flatpack (TQFP) and 100-pin TQFP

Functional Description

The CY7C027V/027AV/028V/028AV and CY7C037AV/038V are low power CMOS 32K, 64K × 16/18 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as stand-alone 16/18-bit dual-port static RAMs or multiple devices can be combined to function as a 32/36-bit or wider master/slave dual-port static RAM. An M/S pin is provided for implementing 32/36-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable (\overline{CE}), Read or Write Enable ($\overline{R/W}$), and Output Enable (\overline{OE}). Two flags are provided on each port (BUSY and INT). BUSY signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag (INT) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power down feature is controlled independently on each port by a chip select (\overline{CE}) pin.

The CY7C027V/027AV/028V/028AV and CY7C037AV/038V are available in 100-pin Thin Quad Plastic Flatpacks (TQFP).

For a complete list of related documentation, [click here](#).

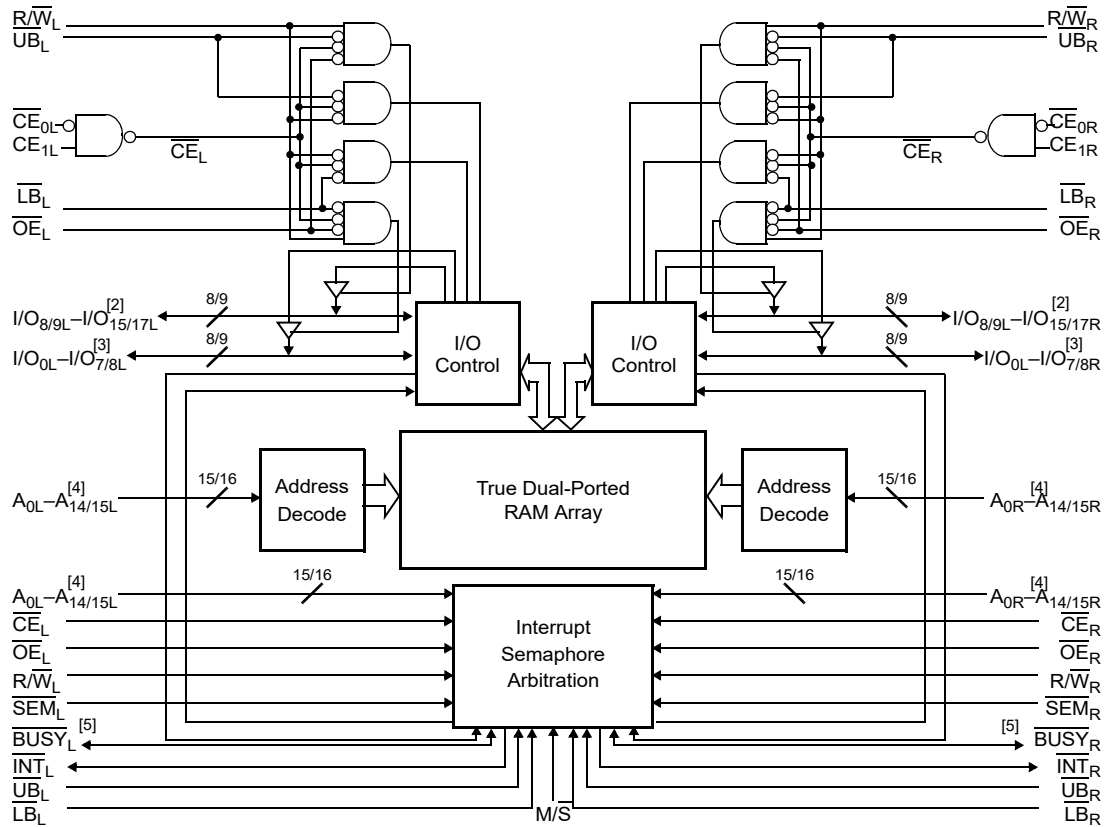
Selection Guide

| Parameter | -15 | -20 | -25 | Unit |
|---|-----|-----|-----|---------|
| Maximum access time | 15 | 20 | 25 | ns |
| Typical operating current | 125 | 120 | 115 | mA |
| Typical standby current for I_{SB1} (Both ports TTL level) | 35 | 35 | 30 | mA |
| Typical standby current for I_{SB3} (Both ports CMOS level) | 10 | 10 | 10 | μ A |

Note

1. CY7C027V, and CY7C027AV are functionally identical. CY7C028V and CY7C028AV are functionally identical.

Logic Block Diagram



Notes

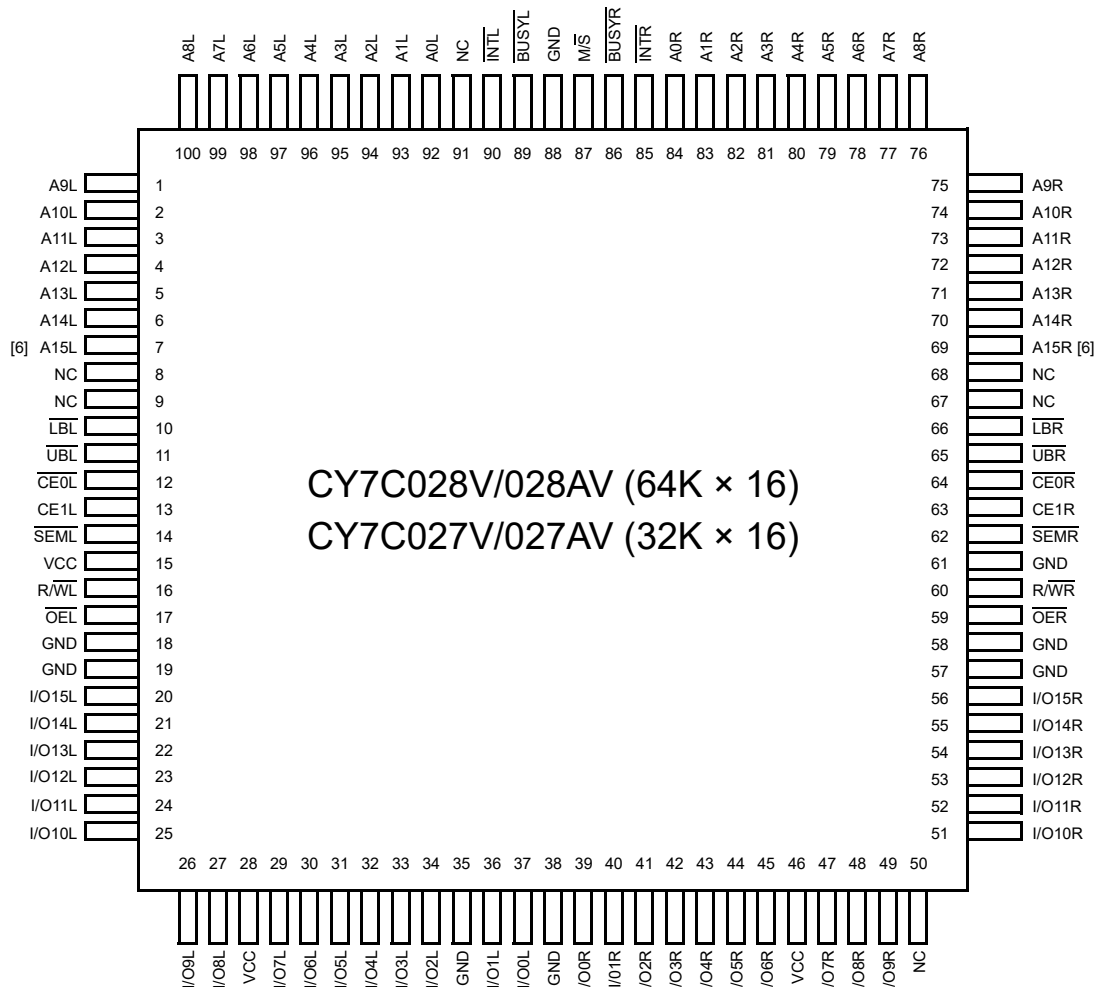
2. $I/O_8-I/O_{15}$ for x16 devices; $I/O_9-I/O_{17}$ for x18 devices.
3. $I/O_0-I/O_7$ for x16 devices; $I/O_0-I/O_8$ for x18 devices.
4. A_0-A_{14} for 32K; A_0-A_{15} for 64K devices.
5. $BUSY$ is an output in master mode and an input in slave mode.

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Pin Configurations

Figure 1. 100-pin TQFP pinout (Top View)

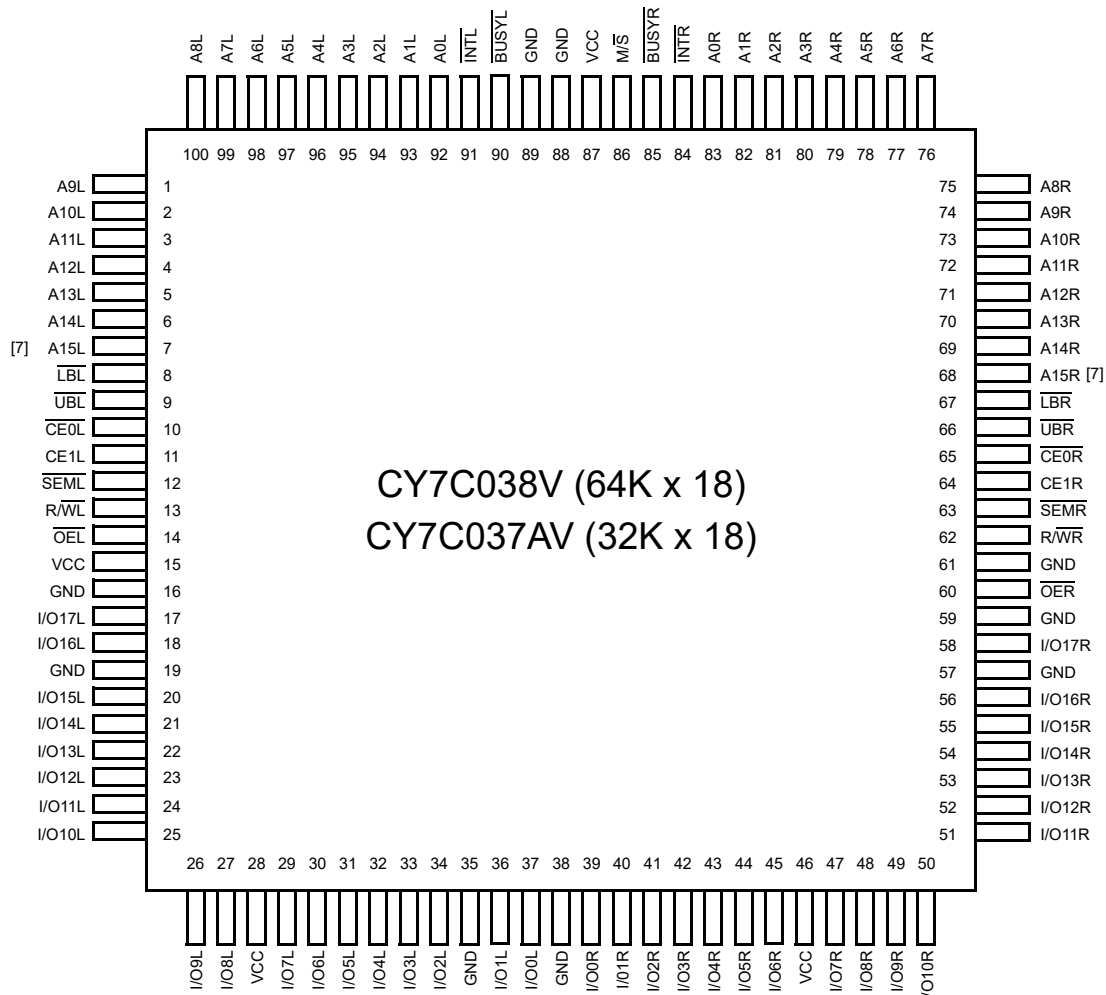


Note

6. This pin is NC for CY7C027V/027AV.

Pin Configurations(continued)

Figure 2. 100-pin TQFP pinout (Top View)



Note

7. This pin is NC for CY7C037AV.

Pin Definitions

| Left Port | Right Port | Description |
|-------------------------------|-------------------------------|---|
| $\overline{CE}_{0L}, CE_{1L}$ | $\overline{CE}_{0R}, CE_{1R}$ | Chip Enable (\overline{CE} is LOW when $\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$) |
| R/W_L | R/W_R | Read/Write Enable |
| \overline{OE}_L | \overline{OE}_R | Output Enable |
| $A_{0L}-A_{15L}$ | $A_{0R}-A_{15R}$ | Address (A_0-A_{14} for 32K; A_0-A_{15} for 64K devices) |
| $I/O_{0L}-I/O_{17L}$ | $I/O_{0R}-I/O_{17R}$ | Data bus input/output ($I/O_0-I/O_{15}$ for $\times 16$ devices; $I/O_0-I/O_{17}$ for $\times 18$) |
| SEM_L | SEM_R | Semaphore Enable |
| \overline{UB}_L | \overline{UB}_R | Upper byte select ($I/O_8-I/O_{15}$ for $\times 16$ devices; $I/O_9-I/O_{17}$ for $\times 18$ devices) |
| \overline{LB}_L | \overline{LB}_R | Lower byte select ($I/O_0-I/O_7$ for $\times 16$ devices; $I/O_0-I/O_8$ for $\times 18$ devices) |
| \overline{INT}_L | \overline{INT}_R | Interrupt flag |
| $BUSY_L$ | $BUSY_R$ | Busy flag |
| M/\overline{S} | | Master or Slave select |
| V_{CC} | | Power |
| GND | | Ground |
| NC | | No connect |

Architecture

The CY7C027V/027AV/028V/028AV and CY7037AV/038V consist of an array of 32K and 64K words of 16 and 18 bits each of dual-port RAM cells, I/O and address lines, and control signals (\overline{CE} , \overline{OE} , R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $BUSY$ pin is provided on each port. Two interrupt (\overline{INT}) pins can be utilized for port-to-port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/\overline{S} pin, the devices can function as a master ($BUSY$ pins are outputs) or as a slave ($BUSY$ pins are inputs). The devices also have an automatic power down feature controlled by \overline{CE} . Each port is provided with its own output enable control (\overline{OE}), which allows data to be read from the device.

Functional Overview

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W to guarantee a valid write. A write operation is controlled by either the R/W pin (see Figure 7) or the \overline{CE} pin (see Figure 8). Required inputs for non-contention operations are summarized in [Non-Contending Read/Write on page 18](#).

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port t_{DD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the \overline{OE} and \overline{CE} pins. Data is available t_{ACE} after \overline{CE} or t_{DOE} after \overline{OE} is asserted. If

the user wishes to access a semaphore flag, then the SEM pin must be asserted instead of the \overline{CE} pin, and \overline{OE} must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (7FFF for the CY7C027V/037AV/027AV, FFFF for the CY7C028V/028AV/38V) is the mailbox for the right port and the second-highest memory location (7FFE for the CY7C027V/027AV/037AV, FFFE for the CY7C028V/028AV/38V) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in [Interrupt Operation Example on page 18](#).

Busy

The CY7C027V/027AV/028V/028AV and CY7037AV/038V provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' \overline{CE} s are asserted and an address match occurs within t_{PS} of each other, the busy logic determines which port has access. If t_{PS} is violated, one port definitely gains permission to the location, but it is not predictable which port gets that permission. $BUSY$ is asserted t_{BLA} after an address match or t_{BLC} after \overline{CE} is taken LOW.

Master/Slave

A $\overline{M/\overline{S}}$ pin is provided to expand the word width by configuring the device as either a master or a slave. The \overline{BUSY} output of the master is connected to the \overline{BUSY} input of the slave. This allows the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the \overline{BUSY} input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the $\overline{M/\overline{S}}$ pin allows the device to be used as a master and, therefore, the \overline{BUSY} line is an output. \overline{BUSY} can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C027V/027AV/028V/028AV and CY7C037AV/038V provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, \overline{SEM} or \overline{OE} must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side

succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting \overline{SEM} LOW. The \overline{SEM} pin functions as a chip select for the semaphore latches (\overline{CE} must remain HIGH during \overline{SEM} LOW). A_{0-2} represents the semaphore address. \overline{OE} and \overline{RW} are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. [Semaphore Operation Example on page 19](#) shows sample semaphore operations.

When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage to ground potential -0.5 V to +4.6 V

DC voltage applied to outputs
in High Z state -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[8] -0.5 V to $V_{CC} + 0.5$ V

Output current into outputs (LOW) 20 mA

Static discharge voltage > 1100 V

Latch-up current > 200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|---------------------------|---------------------|----------------|
| Commercial | 0 °C to +70 °C | 3.3 V ± 300 mV |
| Industrial ^[9] | -40 °C to +85 °C | 3.3 V ± 300 mV |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | | CY7C027V/027AV/028V/028AV/CY7C037AV/CY7C038V | | | | | | | | | Unit |
|------------------|--|---------------------------|--|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | | -15 | | | -20 | | | -25 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V _{OH} | Output HIGH voltage (V _{CC} = Min., I _{OH} = −4.0 mA) | | 2.4 | – | | 2.4 | – | – | 2.4 | – | – | V |
| V _{OL} | Output LOW voltage (V _{CC} = Min., I _{OH} = +4.0 mA) | | – | | 0.4 | – | | 0.4 | – | | 0.4 | V |
| V _{IH} | Input HIGH voltage | | 2.2 | | – | 2.2 | | – | 2.2 | | – | V |
| V _{IL} | Input LOW voltage | | – | | 0.8 | – | | 0.8 | – | | 0.8 | V |
| I _{IX} | Input leakage current | | −5 | | 5 | −5 | | 5 | −5 | | 5 | μA |
| I _{OZ} | Output leakage current | | −10 | 10 | −10 | 10 | −10 | 10 | μA | | | |
| I _{CC} | Operating current (V _{CC} = Max., I _{OUT} = 0 mA) outputs disabled | Commercial | – | 125 | 185 | – | 120 | 175 | – | 115 | 165 | mA |
| | | Industrial ^[9] | | – | | | 140 | 195 | | – | | mA |
| I _{SB1} | Commercial | 35 | | 50 | 35 | | 45 | 30 | | 40 | mA | |
| | Industrial ^[9] | – | | 45 | 55 | | – | | | mA | | |
| I _{SB2} | Commercial | 80 | | 120 | 75 | | 110 | 65 | | 95 | mA | |
| | Industrial ^[9] | – | | 85 | 120 | | – | | | mA | | |
| I _{SB3} | Commercial | 10 | | 250 | 10 | | 250 | 10 | | 250 | μA | |
| | Industrial ^[9] | – | | 10 | 250 | | – | | | μA | | |
| I _{SB4} | Commercial | 75 | | 105 | 70 | | 95 | 60 | | 80 | mA | |
| | Industrial ^[9] | – | | 80 | 105 | | – | | | mA | | |

Capacitance

| Parameter ^[11] | Description | Test Conditions | Max | Unit |
|---------------------------|--------------------|--|-----|------|
| C_{IN} | Input capacitance | $T_A = 25$ °C, $f = 1$ MHz, $V_{CC} = 3.3$ V | 10 | pF |
| C_{OUT} | Output capacitance | | 10 | pF |

Notes

8. Pulse width < 20 ns.

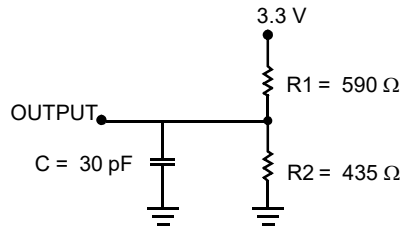
9. Industrial parts are available in CY7C028V and CY7C038V, CY7C027V/027AV only.

10. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at $f = 1/t_{RC}$ (except output enable). $f = 0$ means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3} .

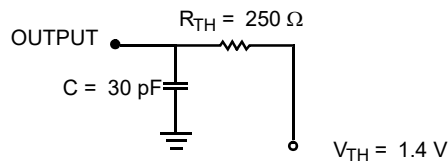
11. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

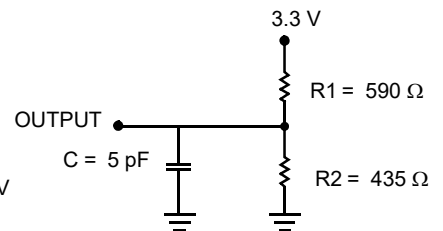
Figure 3. AC Test Loads and Waveforms



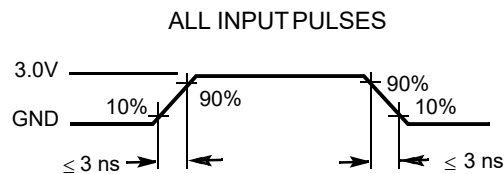
(a) Normal Load (Load 1)



(b) Thévenin Equivalent (Load 1)



(c) Three-State Delay (Load 2)
 (Used for t_{LZ} , t_{HZ} , t_{HZWE} , & t_{LZWE} including scope and jig)

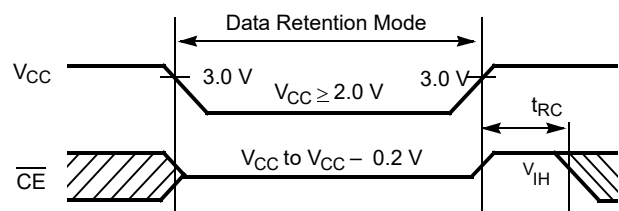


Data Retention Mode

The CY7C027V/027AV/028V/028AV and CY7037AV/038V are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable (\overline{CE}) must be held HIGH during data retention, within V_{CC} to $V_{CC} - 0.2$ V
2. \overline{CE} must be kept between $V_{CC} - 0.2$ V and 70% of V_{CC} during the power up and power down transitions
3. The RAM can begin operation $>t_{RC}$ after V_{CC} reaches the minimum operating voltage (3.0 V)

Timing



| Parameter | Test Conditions ^[12] | Max | Unit |
|-------------|---------------------------------|-----|---------|
| I_{CCDR1} | At $V_{CCDR} = 2$ V | 50 | μ A |

Note

12. $\overline{CE} = V_{CC}$, $V_{in} = GND$ to V_{CC} , $T_A = 25^\circ$ C. This parameter is guaranteed but not tested.

Switching Characteristics

Over the Operating Range

| Parameter ^[13] | Description | CY7C027V/027AV/028V/028AV/ CY7C037AV/CY7C038V | | | | | | Unit |
|---|---|--|-----|-----|-----|-----|-----|------|
| | | -15 | | -20 | | -25 | | |
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle | | | | | | | | |
| t _{RC} | Read cycle time | 15 | – | 20 | – | 25 | – | ns |
| t _{AA} | Address to data valid | – | 15 | – | 20 | – | 25 | ns |
| t _{OHA} | Output hold from address change | 3 | – | 3 | – | 3 | – | ns |
| t _{ACE} ^[14] | $\overline{\text{CE}}$ LOW to data valid | – | 15 | – | 20 | – | 25 | ns |
| t _{DOE} | $\overline{\text{OE}}$ LOW to data valid | – | 10 | – | 12 | – | 13 | ns |
| t _{LZOE} ^[15, 16, 17] | $\overline{\text{OE}}$ LOW to Low Z | 3 | – | 3 | – | 3 | – | ns |
| t _{HZOE} ^[15, 16, 17] | $\overline{\text{OE}}$ HIGH to High Z | – | 10 | – | 12 | – | 15 | ns |
| t _{LZCE} ^[15, 16, 17] | $\overline{\text{CE}}$ LOW to Low Z | 3 | – | 3 | – | 3 | – | ns |
| t _{HZCE} ^[15, 16, 17] | $\overline{\text{CE}}$ HIGH to High Z | – | 10 | – | 12 | – | 15 | ns |
| t _{PU} ^[17] | $\overline{\text{CE}}$ LOW to power-up | 0 | – | 0 | – | 0 | – | ns |
| t _{PD} ^[17] | $\overline{\text{CE}}$ HIGH to power-down | – | 15 | – | 20 | – | 25 | ns |
| t _{ABE} ^[14] | Byte enable access time | – | 15 | – | 20 | – | 25 | ns |
| Write Cycle | | | | | | | | |
| t _{WC} | Write cycle time | 15 | – | 20 | – | 25 | – | ns |
| t _{SCE} ^[14] | $\overline{\text{CE}}$ LOW to write end | 12 | – | 16 | – | 20 | – | ns |
| t _{AW} | Address valid to write end | 12 | – | 16 | – | 20 | – | ns |
| t _{HA} | Address hold from write end | 0 | – | 0 | – | 0 | – | ns |
| t _{SA} ^[14] | Address setup to write start | 0 | – | 0 | – | 0 | – | ns |
| t _{PWE} | Write pulse width | 12 | – | 17 | – | 22 | – | ns |
| t _{SD} | Data setup to write end | 10 | – | 12 | – | 15 | – | ns |
| t _{HD} | Data hold from write end | 0 | – | 0 | – | 0 | – | ns |
| t _{HZWE} ^[16, 17] | R/ $\overline{\text{W}}$ LOW to High Z | – | 10 | – | 12 | – | 15 | ns |
| t _{LZWE} ^[16, 17] | R/ $\overline{\text{W}}$ HIGH to Low Z | 3 | – | 3 | – | 3 | – | ns |
| t _{WDD} ^[18] | Write pulse to data delay | – | 30 | – | 40 | – | 50 | ns |
| t _{DDD} ^[18] | Write data valid to read data valid | – | 25 | – | 30 | – | 35 | ns |

Notes

13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.

14. To access RAM, $\overline{CE}=L$, $\overline{UB}=L$, $\overline{SEM}=H$. To access semaphore, $\overline{CE}=H$ and $\overline{SEM}=L$. Either condition must be valid for the entire t_{SCE} time.

15. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE} .

16. Test conditions used are Load 2.

17. This parameter is guaranteed by design, but it is not production tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 11 on page 15.

18. t_{DDD} is a calculated parameter and is the greater of $t_{WDD}-t_{PWE}$ (actual) or $t_{DDD}-t_{SD}$ (actual).

Switching Characteristics(continued)

Over the Operating Range

| Parameter ^[13] | Description | CY7C027V/027AV/028V/028AV/ CY7C037AV/CY7C038V | | | | | | Unit |
|----------------------------------|-----------------------------------|--|-----|-----|-----|-----|-----|------|
| | | -15 | | -20 | | -25 | | |
| | | Min | Max | Min | Max | Min | Max | |
| Busy Timing ^[19] | | | | | | | | |
| t _{BLA} | BUSY LOW from address match | – | 15 | – | 20 | – | 20 | ns |
| t _{BHA} | BUSY HIGH from address mismatch | – | 15 | – | 20 | – | 20 | ns |
| t _{BLC} | BUSY LOW from CE LOW | – | 15 | – | 20 | – | 20 | ns |
| t _{BHC} | BUSY HIGH from CE HIGH | – | 15 | – | 16 | – | 17 | ns |
| t _{PS} | Port setup for priority | 5 | – | 5 | – | 5 | – | ns |
| t _{WB} | R/W HIGH after BUSY (Slave) | 0 | – | 0 | – | 0 | – | ns |
| t _{WH} | R/W HIGH after BUSY HIGH (Slave) | 13 | – | 15 | – | 17 | – | ns |
| t _{BDD} ^[20] | BUSY HIGH to data valid | – | 15 | – | 20 | – | 25 | ns |
| Interrupt Timing ^[19] | | | | | | | | |
| t _{INS} | INT set time | – | 15 | – | 20 | – | 20 | ns |
| t _{INR} | INT reset time | – | 15 | – | 20 | – | 20 | ns |
| Semaphore Timing | | | | | | | | |
| t _{SOP} | SEM flag update pulse (OE or SEM) | 10 | – | 10 | – | 12 | – | ns |
| t _{SWRD} | SEM flag write to read time | 5 | – | 5 | – | 5 | – | ns |
| t _{SPS} | SEM flag contention window | 5 | – | 5 | – | 5 | – | ns |
| t _{SAA} | SEM address access time | – | 15 | – | 20 | – | 25 | ns |

Notes

19. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 11 on page 15.

20. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{BDD}–t_{SD} (actual).

Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port Address Access) [21, 22, 23]

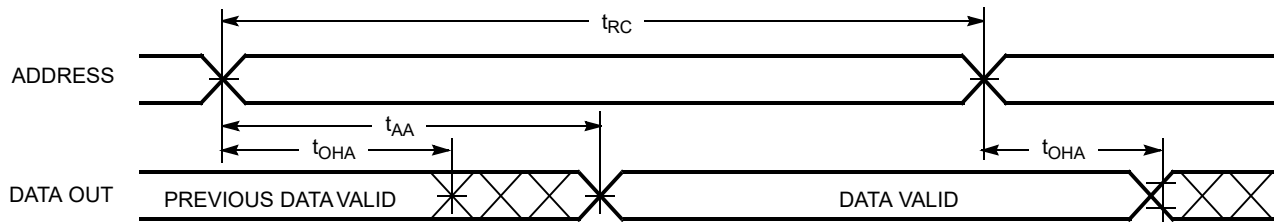


Figure 5. Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access) [21, 24, 25]

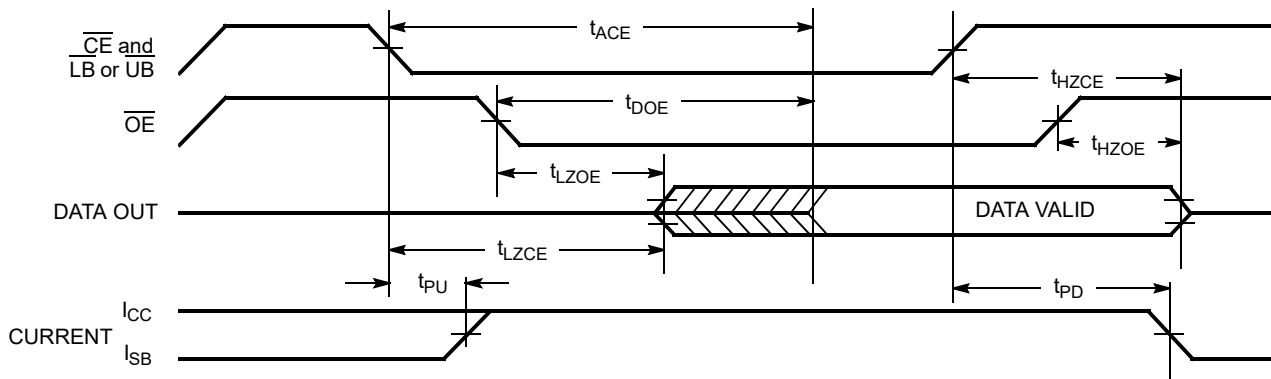
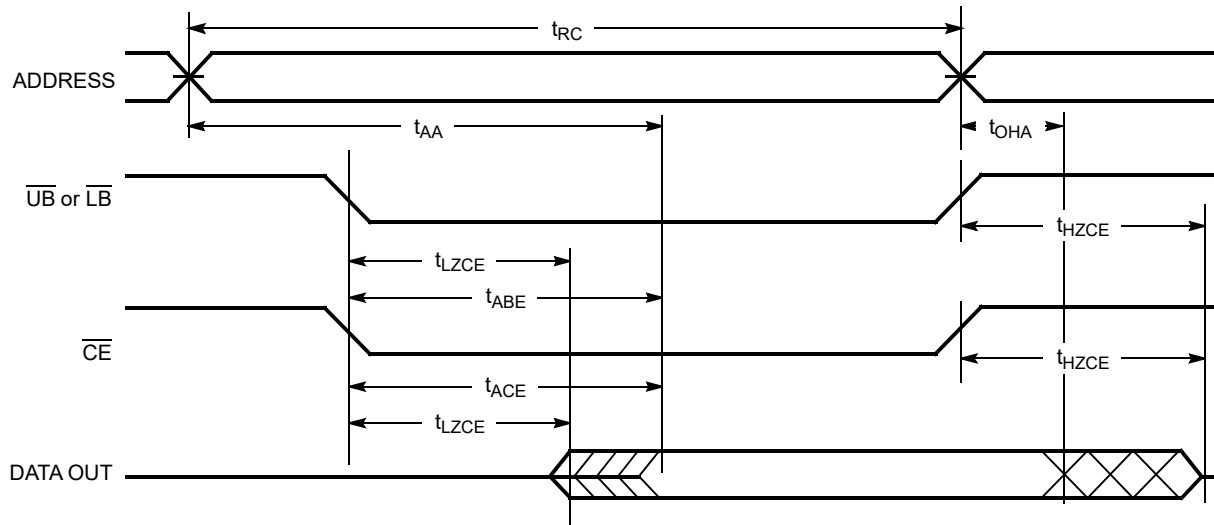


Figure 6. Read Cycle No. 3 (Either Port) [21, 23, 24, 25]



Notes

21. R/W is HIGH for read cycles.
22. Device is continuously selected $\overline{CE} = V_{IL}$ and \overline{UB} or $\overline{LB} = V_{IL}$. This waveform cannot be used for semaphore reads.
23. $\overline{OE} = V_{IL}$.
24. Address valid prior to or coincident with \overline{CE} transition LOW.
25. To access RAM, $\overline{CE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

Switching Waveforms(continued)

Figure 7. Write Cycle No. 1: R/W Controlled Timing [26, 27, 28, 29]

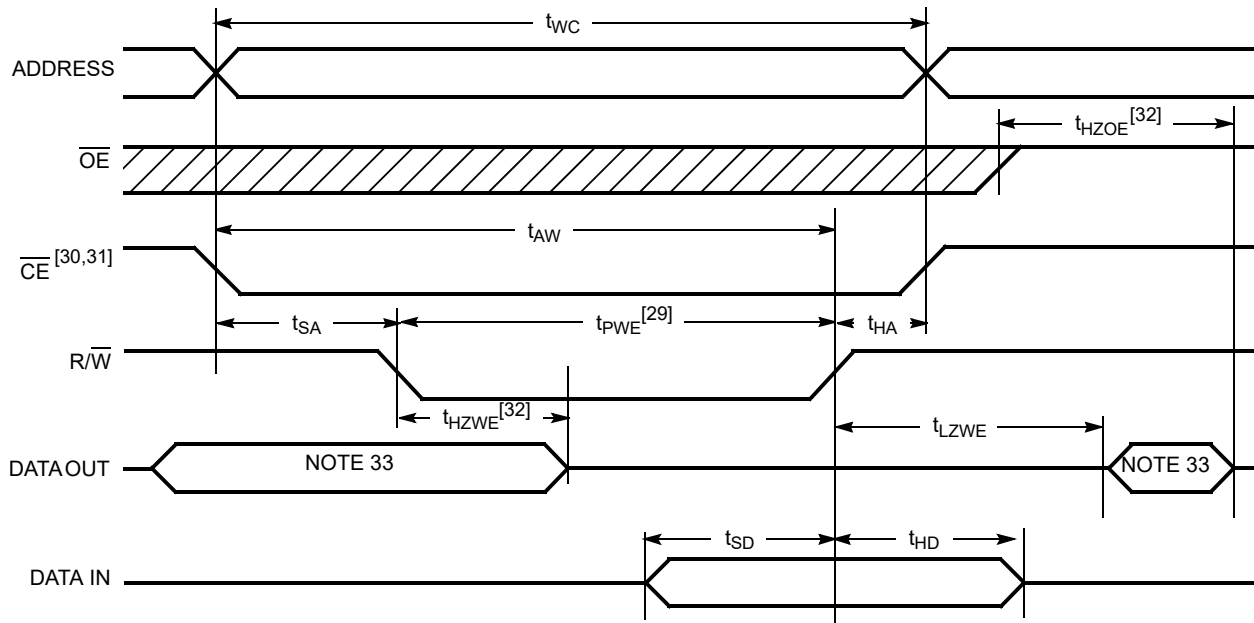
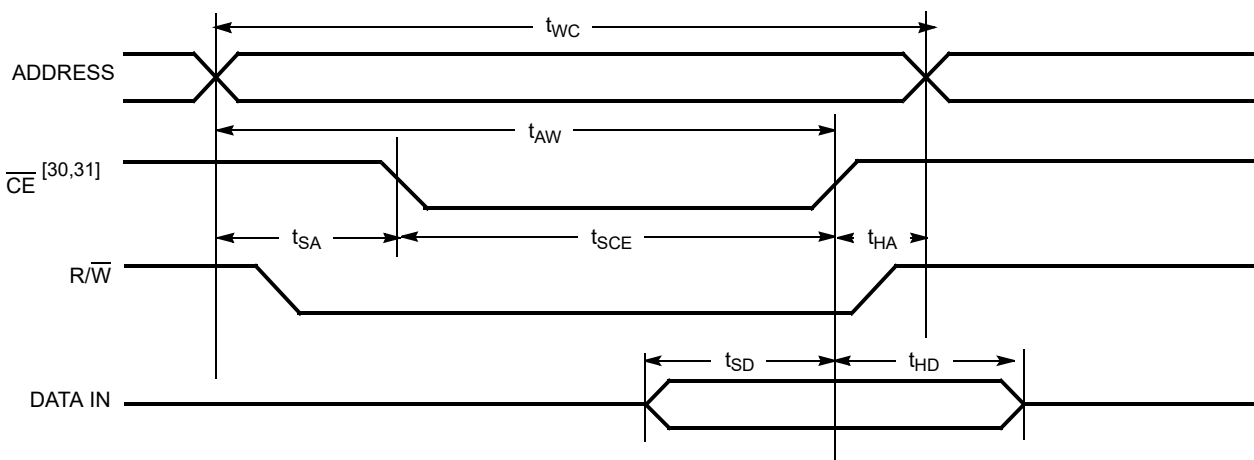


Figure 8. Write Cycle No. 2: CE Controlled Timing [26, 27, 28, 34]



Notes

26. R/W must be HIGH during all address transitions.
27. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW \overline{CE} or \overline{SEM} and a LOW \overline{UB} or \overline{LB} .
28. t_{HA} is measured from the earlier of CE or R/W or (SEM or R/W) going HIGH at the end of write cycle.
29. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD} . If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE} .
30. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$.
31. To access upper byte, $\overline{CE} = V_{IL}$, $\overline{UB} = V_{IL}$, $\overline{SEM} = V_{IH}$.
- To access lower byte, $\overline{CE} = V_{IL}$, $\overline{LB} = V_{IL}$, $\overline{SEM} = V_{IH}$.
32. Transition is measured ± 500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.
33. During this period, the I/O pins are in the output state, and input signals must not be applied.
34. If the CE or SEM LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high impedance state.

Switching Waveforms(continued)

Figure 9. Semaphore Read After Write Timing, Either Side [35]

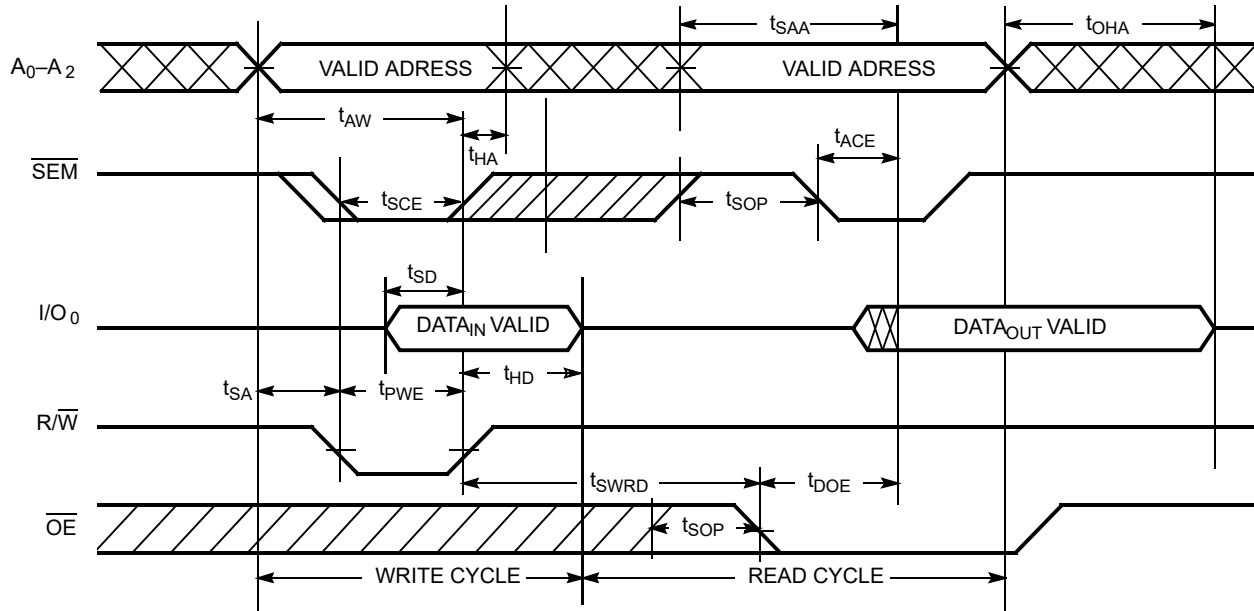
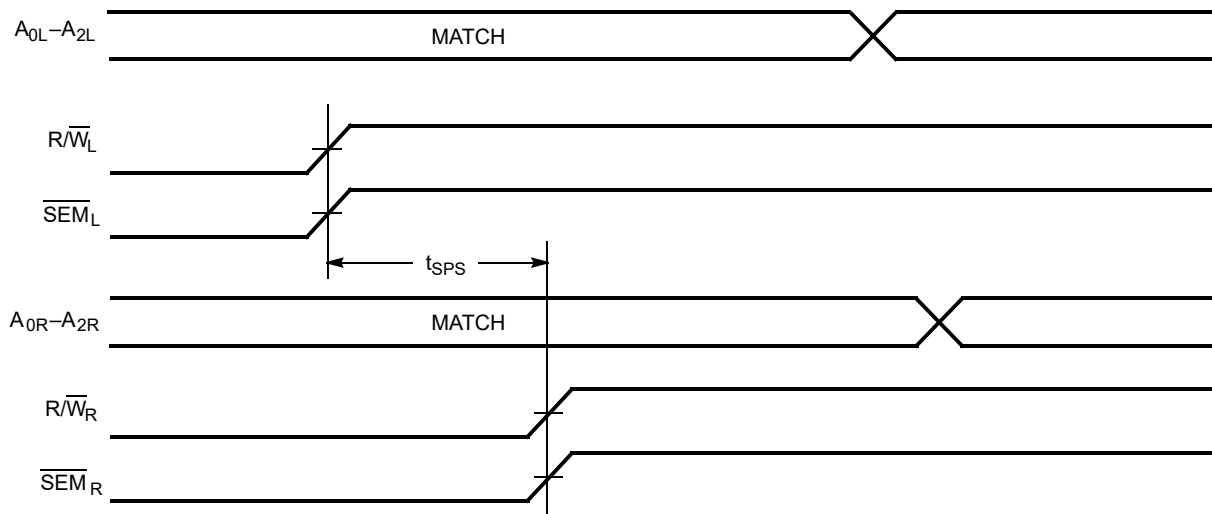


Figure 10. Timing Diagram of Semaphore Contention [36, 37, 38]



Notes

35. CE = HIGH for the duration of the above timing (both write and read cycle).
36. I/O_{0R} = I/O_{0L} = LOW (request semaphore); CE_R = CE_L = HIGH.
37. Semaphores are reset (available to both ports) at cycle start.
38. If t_{SPS} is violated, the semaphore is definitely obtained by one side or the other, but which side gets the semaphore is unpredictable.

Switching Waveforms(continued)

Figure 11. Timing Diagram of Read with $\overline{\text{BUSY}}$ ($\text{M}/\overline{\text{S}} = \text{HIGH}$) ^[39]

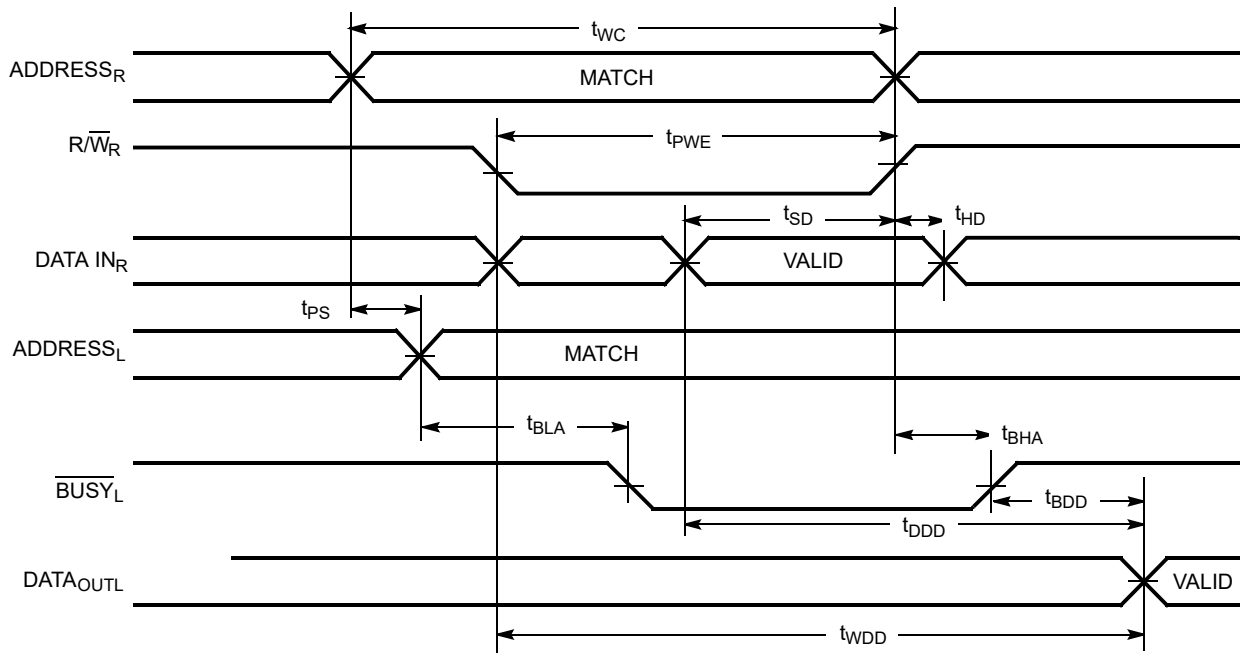
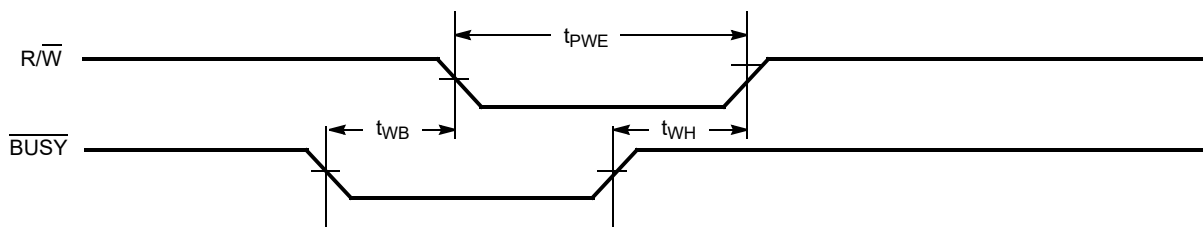


Figure 12. Write Timing with Busy Input ($\text{M}/\overline{\text{S}} = \text{LOW}$)

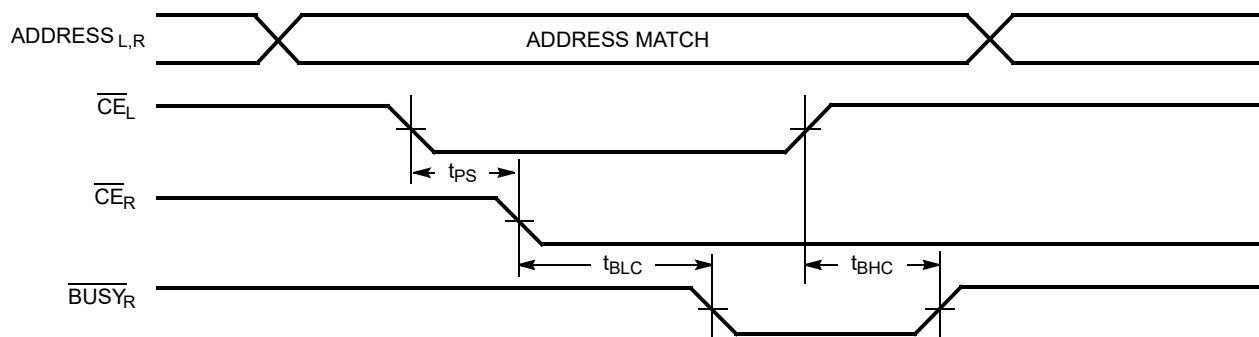


Note
 39. $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{LOW}$.

Switching Waveforms(continued)

Figure 13. Busy Timing Diagram No. 1 (\overline{CE} Arbitration) [40]

\overline{CE}_L Valid First:



\overline{CE}_R Valid First:

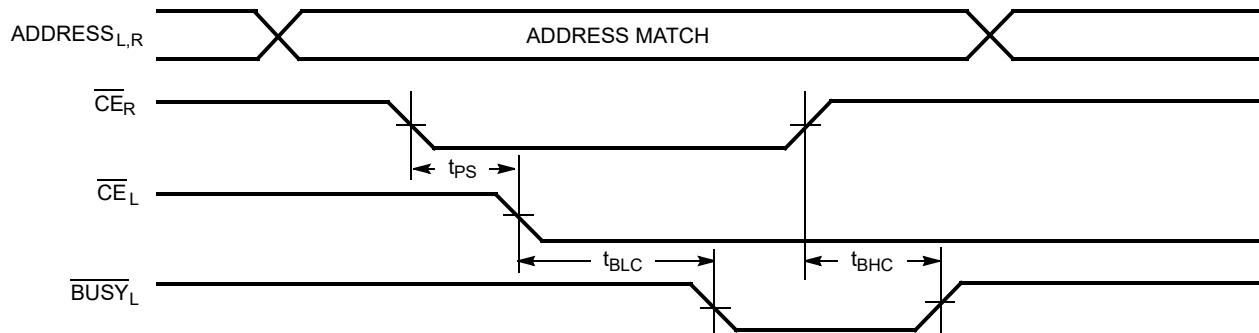
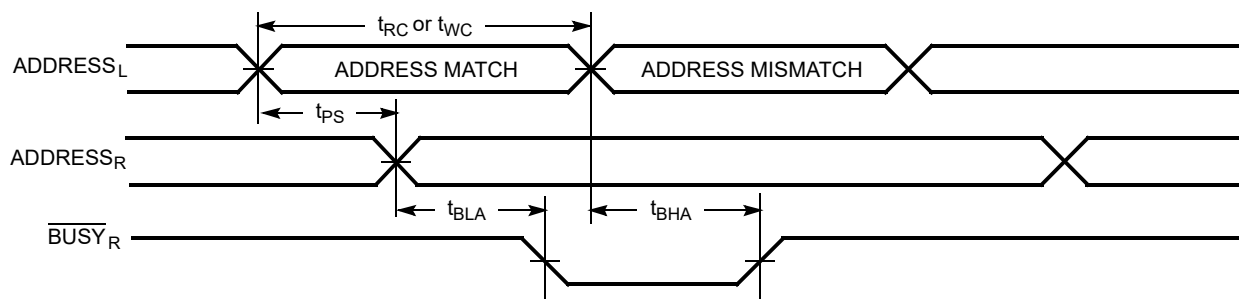
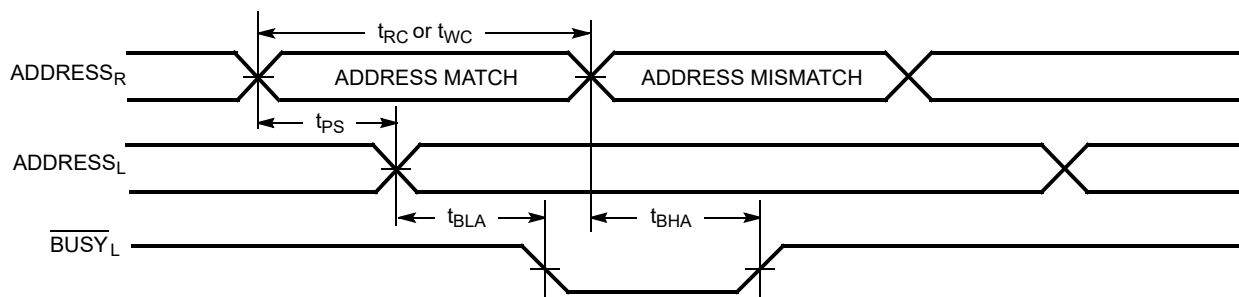


Figure 14. Busy Timing Diagram No. 2 (Address Arbitration) [40]

Left Address Valid First:



Right Address Valid First:



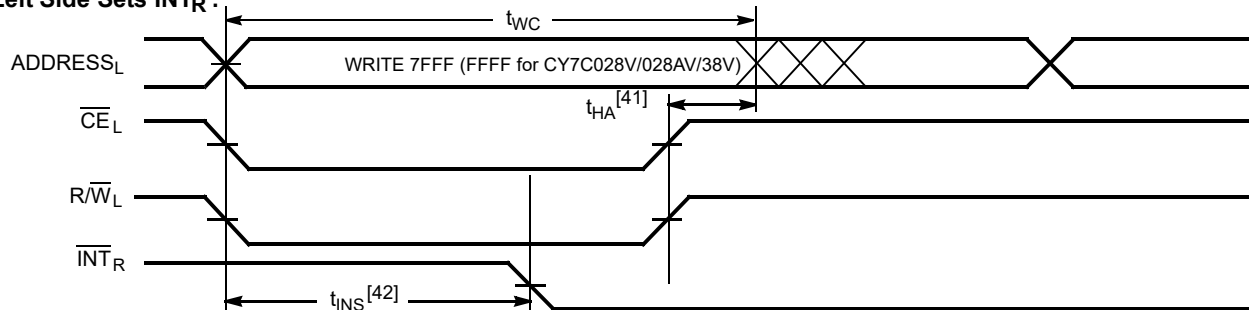
Note

40. If t_{PS} is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side \overline{BUSY} is asserted.

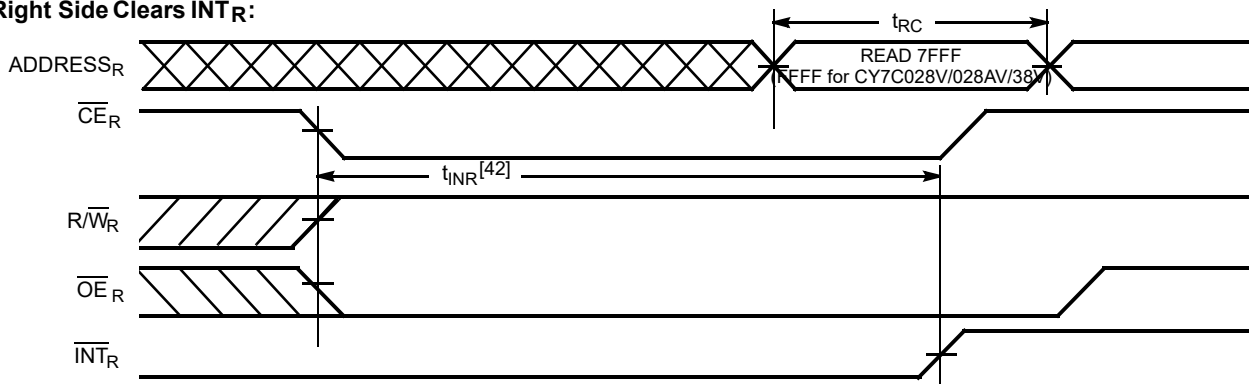
Switching Waveforms(continued)

Figure 15. Interrupt Timing Diagrams

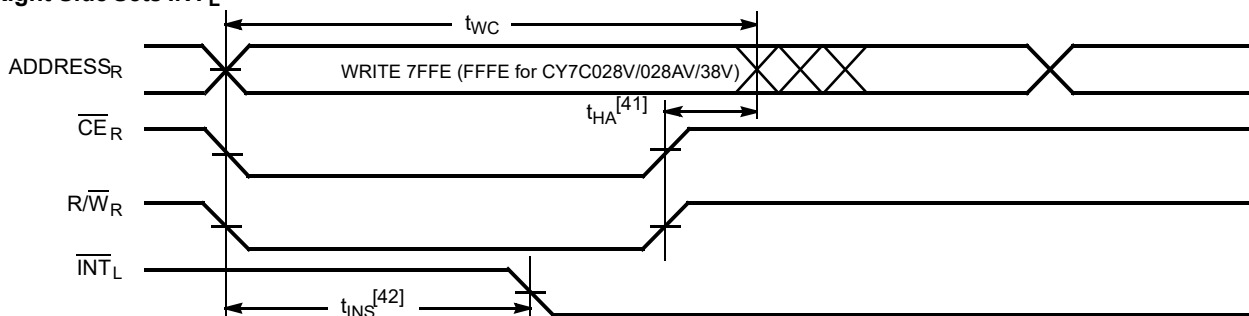
Left Side Sets $\overline{\text{INT}}_R$:



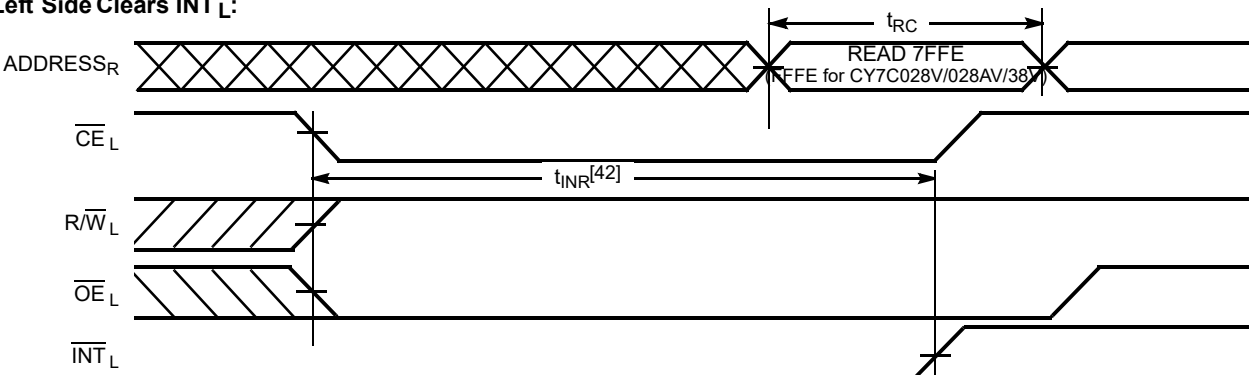
Right Side Clears $\overline{\text{INT}}_R$:



Right Side Sets $\overline{\text{INT}}_L$:





Left Side Clears $\overline{\text{INT}}_L$:



Notes

41. t_{HA} depends on which enable pin ($\overline{\text{CE}}_L$ or $\overline{\text{R}}/\overline{\text{W}}_L$) is deasserted first.
42. t_{INS} or t_{INR} depends on which enable pin ($\overline{\text{CE}}_L$ or $\overline{\text{R}}/\overline{\text{W}}_L$) is asserted last.

Non-Contending Read/Write

| Inputs | | | | | | Outputs | | Operation |
|--------|--|----|----|----|-----|-------------------------------------|------------------------------------|--|
| CE | R/W | OE | UB | LB | SEM | I/O ₉ –I/O ₁₇ | I/O ₀ –I/O ₈ | |
| H | X | X | X | X | H | High Z | High Z | Deselected: Power-down |
| X | X | X | H | H | H | High Z | High Z | Deselected: Power-down |
| L | L | X | L | H | H | Data in | High Z | Write to upper byte only |
| L | L | X | H | L | H | High Z | Data in | Write to lower byte only |
| L | L | X | L | L | H | Data in | Data in | Write to both bytes |
| L | H | L | L | H | H | Data out | High Z | Read upper byte only |
| L | H | L | H | L | H | High Z | Data out | Read lower byte only |
| L | H | L | L | L | H | Data out | Data out | Read both bytes |
| X | X | H | X | X | X | High Z | High Z | Outputs disabled |
| H | H | L | X | X | L | Data out | Data out | Read data in semaphore flag |
| X | H | L | H | H | L | Data out | Data out | Read data in semaphore flag |
| H |  | X | X | X | L | Data in | Data in | Write D _{IN0} into semaphore flag |
| X |  | X | H | H | L | Data in | Data in | Write D _{IN0} into semaphore flag |
| L | X | X | L | X | L | | | Not allowed |
| L | X | X | X | L | L | | | Not allowed |

Interrupt Operation Example

(Assumes $\overline{\text{BUSY}}_L = \overline{\text{BUSY}}_R = \text{HIGH}$)^[43]

| Function | Left Port | | | | | Right Port | | | | |
|--|------------------|-----------------|-----------------|---------------------|-------------------|------------------|-----------------|-----------------|---------------------|-------------------|
| | R/W _L | CE _L | OE _L | A _{0L–14L} | INT _L | R/W _R | CE _R | OE _R | A _{0R–14R} | INT _R |
| Set right $\overline{\text{INT}}_R$ flag | L | L | X | 7FFF | X | X | X | X | X | L ^[44] |
| Reset right $\overline{\text{INT}}_R$ flag | X | X | X | X | X | X | L | L | 7FFF | H ^[45] |
| Set left $\overline{\text{INT}}_L$ flag | X | X | X | X | L ^[45] | L | L | X | 7FFE | X |
| Reset left $\overline{\text{INT}}_L$ flag | X | L | L | 7FFE | H ^[44] | X | X | X | X | X |

Notes

43. A_{0L–15L} and A_{0R–15R}, FFFF/FFFE for the CY7C028V/038V.

44. If $\overline{\text{BUSY}}_L = \text{L}$, then no change.

45. If $\overline{\text{BUSY}}_R = \text{L}$, then no change.

Semaphore Operation Example

| Function | I/O ₀ –I/O ₁₇ Left | I/O ₀ –I/O ₁₇ Right | Status |
|----------------------------------|--|---|--|
| No action | 1 | 1 | Semaphore free |
| Left port writes 0 to semaphore | 0 | 1 | Left port has semaphore token |
| Right port writes 0 to semaphore | 0 | 1 | No change. Right side has no write access to semaphore |
| Left port writes 1 to semaphore | 1 | 0 | Right port obtains semaphore token |
| Left port writes 0 to semaphore | 1 | 0 | No change. Left port has no write access to semaphore |
| Right port writes 1 to semaphore | 0 | 1 | Left port obtains semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore free |
| Right port writes 0 to semaphore | 1 | 0 | Right port has semaphore token |
| Right port writes 1 to semaphore | 1 | 1 | Semaphore free |
| Left port writes 0 to semaphore | 0 | 1 | Left port has semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore free |

Ordering Information

32K × 16 3.3 V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|----------------|--------------|------------------------|-----------------|
| 15 | CY7C027V-15AXC | A100 | 100-pin TQFP (Pb-free) | Commercial |
| | CY7C027V-15AXI | A100 | 100-pin TQFP (Pb-free) | Industrial |
| 20 | CY7C027V-20AXC | A100 | 100-pin TQFP (Pb-free) | Commercial |
| 25 | CY7C027V-25AXC | A100 | 100-pin TQFP (Pb-free) | Commercial |

64K × 16 3.3 V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|-----------------|--------------|------------------------|-----------------|
| 15 | CY7C028V-15AXC | A100 | 100-pin TQFP (Pb-free) | Commercial |
| | CY7C028V-15AXI | A100 | 100-pin TQFP (Pb-free) | Industrial |
| 20 | CY7C028V-20AXC | A100 | 100-pin TQFP (Pb-free) | Commercial |
| | CY7C028V-20AI | A100 | 100-pin TQFP | Industrial |
| | CY7C028V-20AXI | A100 | 100-pin TQFP (Pb-free) | Industrial |
| 25 | CY7C028V-25AXC | A100 | 100-pin TQFP (Pb-free) | Commercial |
| | CY7C028AV-25AXC | A100 | 100-pin TQFP (Pb-free) | Commercial |

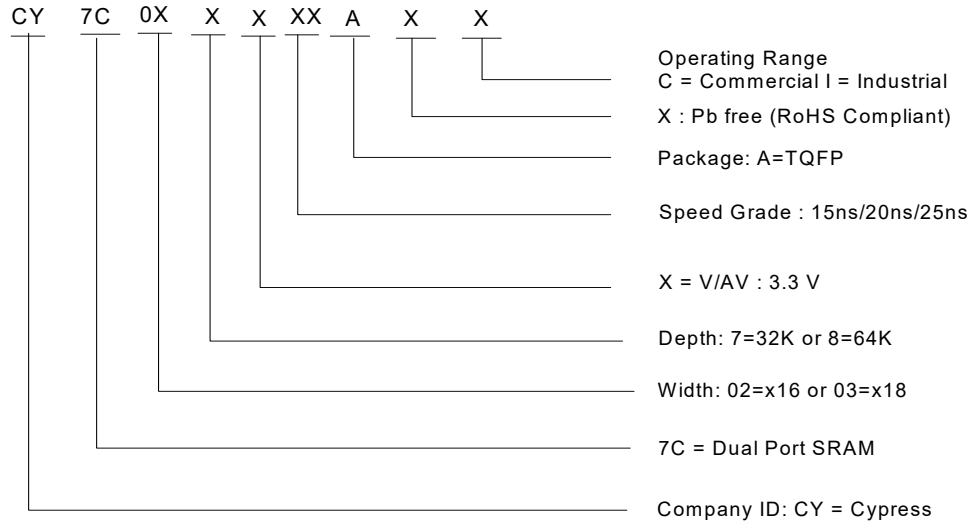
32K × 18 3.3 V Asynchronous Dual-Port SRAM

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|-----------------|--------------|------------------------|-----------------|
| 20 | CY7C037AV-20AXI | A100 | 100-pin TQFP (Pb-free) | Industrial |

64K × 18 3.3 V Asynchronous Dual-Port SRAM

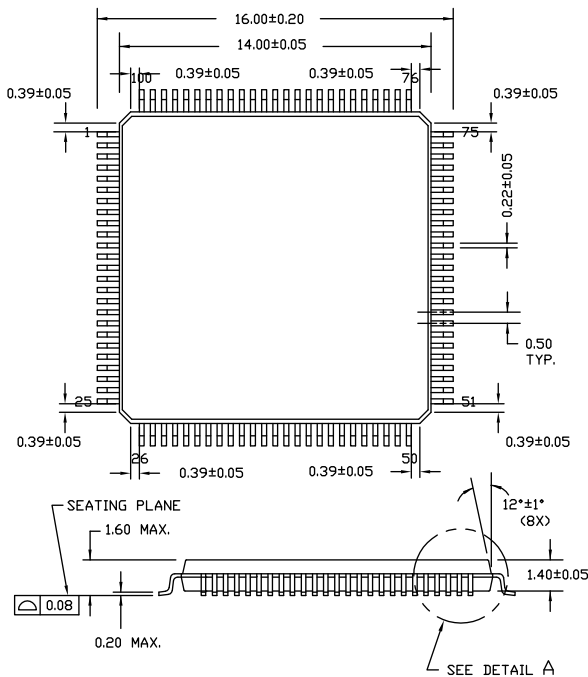
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|----------------|--------------|------------------------|-----------------|
| 20 | CY7C038V-20AXI | A100 | 100-pin TQFP (Pb-free) | Industrial |

Ordering Code Definitions



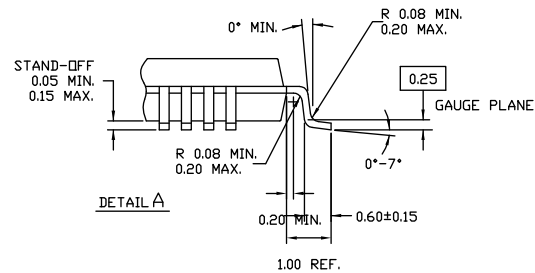
Package Diagram

Figure 16. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048

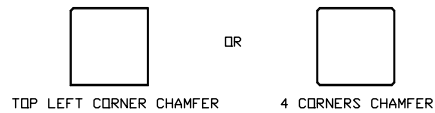


NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.009 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



NOTE: PKG. CAN HAVE



51-85048 *J

Acronyms

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| SRAM | Static Random Access Memory |
| TQFP | Thin Quad Flat Pack |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY7C027V/027AV/028V/028AV/CY7C037AV/038V, 3.3 V, 32K/64K × 16/18 Dual-Port Static RAM Document Number: 38-06078 | | | | |
|--|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 237626 | YDT | 06/30/2004 | Converted data sheet from old spec 38-00670 to conform with new data sheet. Updated Features (Removed cross information). |
| *A | 259110 | JHX | 09/01/2004 | Added Pb-Free logo in top of first page. Updated Ordering Information (Updated part numbers). |
| *B | 2623540 | VKN / PYRS | 12/17/2008 | Updated Document Title to read as "CY7C027V/027VN/027AV/ CY7C028V/037V/037AV/038V 3.3V 32K/64K x 16/18 Dual Port Static RAM". Added CY7C027VN, CY7C027AV and CY7C037AV parts related information in all instances across the document. Updated Ordering Information (Updated part numbers). Updated to new template. |
| *C | 2897217 | RAME | 03/22/2010 | Updated Ordering Information (Updated part numbers). Updated Package Diagram : spec 51-85048 – Changed revision from *C to *D. |
| *D | 3093542 | ADMU | 11/25/2010 | Updated Document Title to read as "CY7C027V/027AV/ CY7C028V/037AV/038V 3.3 V 32K/64K X 16/18 Dual Port Static RAM". Removed CY7C027VN and CY7C037V parts related information in all instances across the document. Updated Ordering Information : No change in part numbers. Added Ordering Code Definitions . Added Acronyms and Units of Measure . Updated to new template. Completing Sunset Review. |
| *E | 3403652 | ADMU | 10/14/2011 | Updated Ordering Information (Updated part numbers). Updated Package Diagram : spec 51-85048 – Changed revision from *D to *E. Completing Sunset Review. |
| *F | 3845411 | ADMU | 01/29/2013 | Updated Ordering Information (Updated part numbers). Updated Package Diagram : spec 51-85048 – Changed revision from *E to *G. |
| *G | 3896090 | ADMU | 02/05/2013 | Updated Ordering Information (Updated part numbers). |
| *H | 4103305 | ADMU | 08/23/2013 | Updated Document Title to read as "CY7C027V/027AV/028V/028AV/ CY7C037AV/038V, 3.3 V 32 K / 64 K × 16 / 18 Dual-Port Static RAM". Included CY7C028AV related information in all instances across the document. Updated Ordering Information (Updated part numbers). Updated Package Diagram : spec 51-85048 – Changed revision from *G to *H. Updated to new template. |
| *I | 4575241 | ADMU | 11/20/2014 | Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Ordering Information : Updated part numbers. Updated Package Diagram : spec 51-85048 – Changed revision from *H to *I. Completing Sunset Review. |

Document History Page(continued)

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|--|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| *J | 6043656 | VINI | 01/24/2018 | Updated Ordering Information : Updated part numbers. Updated Package Diagram : spec 51-85048 – Changed revision from *I to *J. Updated to new template. Completing Sunset Review. |

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