

8Mb ZBT® SRAM

FEATURES

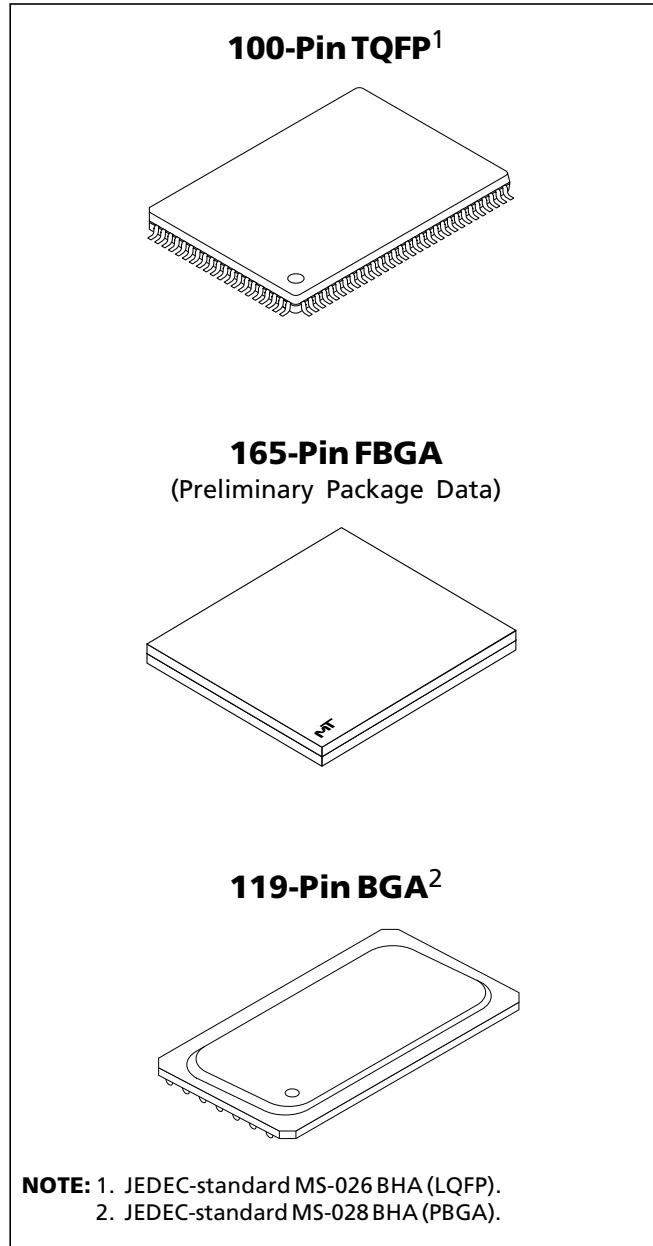
- High frequency and 100 percent bus utilization
- Fast cycle times: 10ns, 11ns and 12ns
- Single +3.3V \pm 5% power supply (V_{DD})
- Separate +3.3V or +2.5V isolated output buffer supply (V_{DDQ})
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs to eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 4Mb, and 18Mb ZBT SRAM
- 100-pin TQFP
- 165-pin FBGA
- 119-pin BGA package
- Automatic power-down

OPTIONS

| MARKING* | |
|-------------------------------|--------------|
| • Timing (Access/Cycle/MHz) | |
| 7.5ns/10ns/100 MHz | -10 |
| 8.5ns/11ns/90 MHz | -11 |
| 9ns/12ns/83 MHz | -12 |
| • Configurations | |
| 3.3V I/O | |
| 512K x 18 | MT55L512L18F |
| 256K x 32 | MT55L256L32F |
| 256K x 36 | MT55L256L36F |
| 2.5V I/O | |
| 512K x 18 | MT55L512V18F |
| 256K x 32 | MT55L256V32F |
| 256K x 36 | MT55L256V36F |
| • Package | |
| 100-pin TQFP | T |
| 165-pin FBGA | F |
| 119-pin, 14mm x 22mm BGA | B |
| • Operating Temperature Range | |
| Commercial (0°C to +70°C) | None |
| Industrial (-40°C to +85°C)** | IT |

MT55L512L18F, MT55L512V18F,
MT55L256L32F, MT55L256V32F,
MT55L256L36F, MT55L256V36F

3.3V V_{DD}, 3.3V or 2.5V I/O

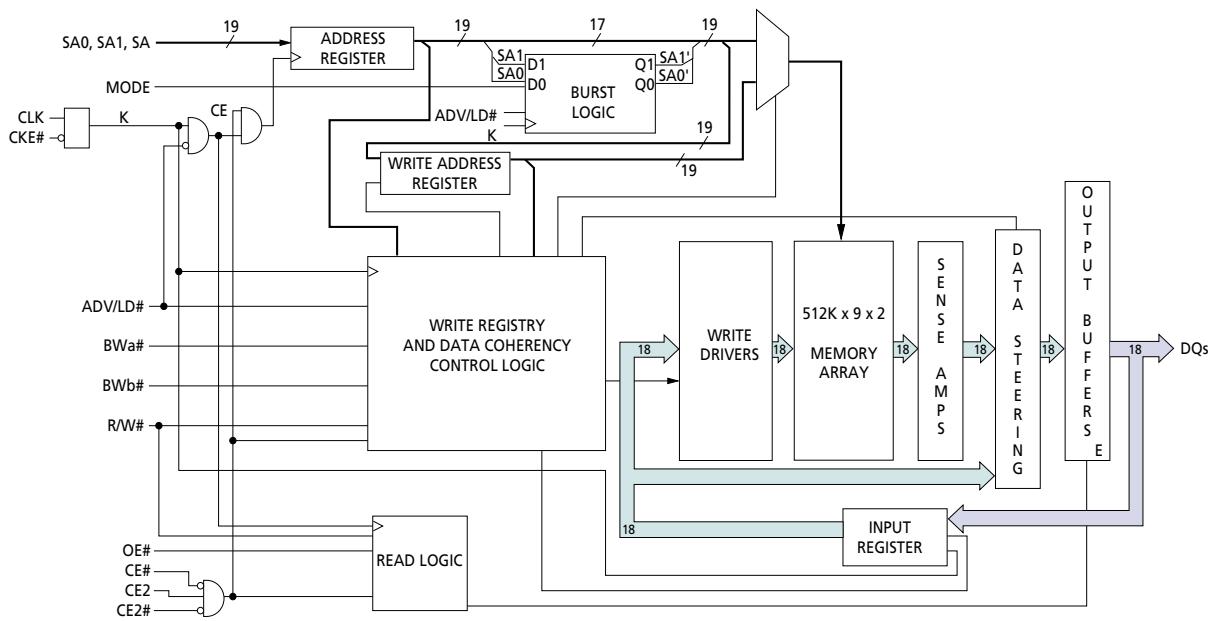
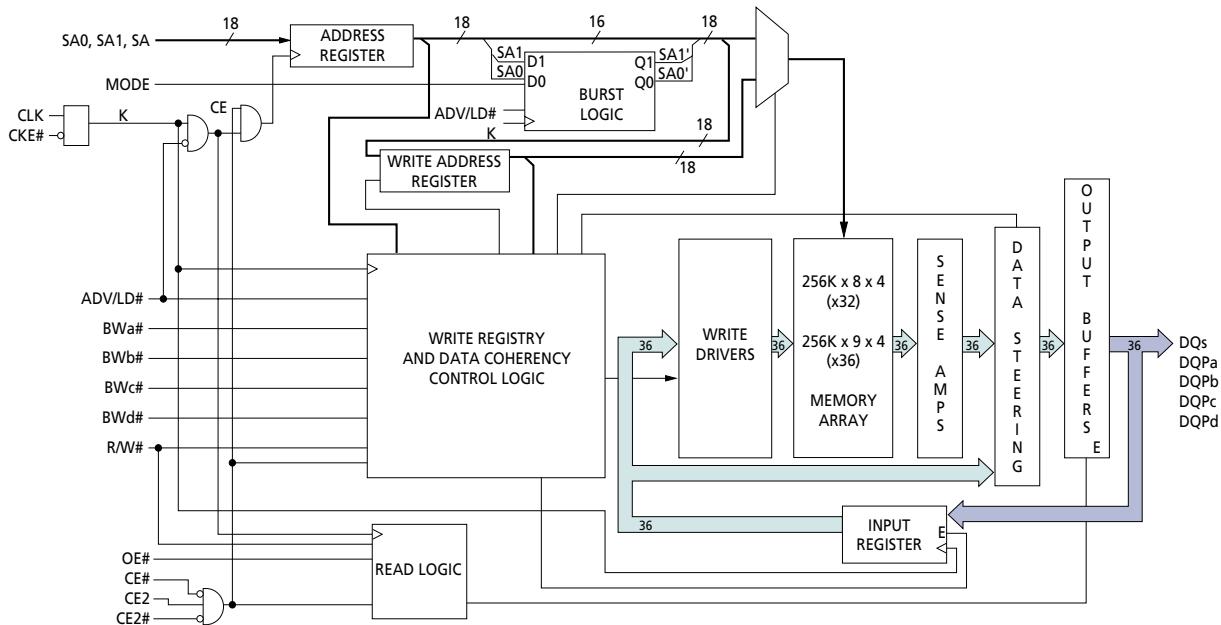


NOTE: 1. JEDEC-standard MS-026 BHA (LQFP).
2. JEDEC-standard MS-028 BHA (PBGA).

Part Number Example:
MT55L256L32FT-11

* A Part Marking Guide for the FBGA devices can be found on Micron's Web site—<http://www.micron.com/support/index.html>.

** Industrial temperature range offered in specific speed grades and configurations. Contact factory for more information.

**FUNCTIONAL BLOCK DIAGRAM
512K x 18**

**FUNCTIONAL BLOCK DIAGRAM
256K x 32/36**


NOTE: Functional block diagrams illustrate simplified device operation. See truth table, pin descriptions, and timing diagrams for detailed information.

GENERAL DESCRIPTION

The Micron® Zero Bus Turnaround™ (ZBT®) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

Micron's 8Mb ZBT SRAMs integrate a 512K x 18, 256K x 32, or 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles for READ to WRITE, or WRITE to READ, transitions. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc#, and BWd#), and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal minimization), clock (CLK), and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW, or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE, and DESELECT cycles are initiated by the ADV/LD# input. Subsequent burst ad-

resses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the flow-through ZBT SRAM uses a LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need to be asserted on the same cycle as the address. The write data associated with the address is required one cycle later, or on the rising edge of clock cycle two.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are available only on the x18 and x36 versions.

Micron's 8Mb ZBT SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are LVTTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for systems requiring high bandwidth and zero bus turnaround delays.

Please refer to the Micron Web site (www.micron.com/datasheets) for the latest data sheet.

TQFP PIN ASSIGNMENT TABLE

| PIN # | x18 | x32 | x36 |
|-------|-----|------------------|------|
| 1 | NC | NF | DQPC |
| 2 | NC | DQC | DQC |
| 3 | NC | DQC | DQC |
| 4 | | VDDQ | |
| 5 | | VSS | |
| 6 | NC | DQC | DQC |
| 7 | NC | DQC | DQC |
| 8 | DQB | DQC | DQC |
| 9 | DQB | DQC | DQC |
| 10 | | VSS | |
| 11 | | VDDQ | |
| 12 | DQB | DQC | DQC |
| 13 | DQB | DQC | DQC |
| 14 | | VSS ¹ | |
| 15 | | VDD | |
| 16 | | VDD ² | |
| 17 | | VSS | |
| 18 | DQB | DQD | DQD |
| 19 | DQB | DQD | DQD |
| 20 | | VDDQ | |
| 21 | | VSS | |
| 22 | DQB | DQD | DQD |
| 23 | DQB | DQD | DQD |
| 24 | DQB | DQD | DQD |
| 25 | NC | DQD | DQD |

| PIN # | x18 | x32 | x36 |
|-------|-----|-------------|------|
| 26 | | VSS | |
| 27 | | VDDQ | |
| 28 | NC | DQD | DQD |
| 29 | NC | DQD | DQD |
| 30 | NC | NF | DQPD |
| 31 | | MODE (LBO#) | |
| 32 | | SA | |
| 33 | | SA | |
| 34 | | SA | |
| 35 | | SA | |
| 36 | | SA1 | |
| 37 | | SA0 | |
| 38 | | DNU | |
| 39 | | DNU | |
| 40 | | VSS | |
| 41 | | VDD | |
| 42 | | DNU | |
| 43 | | DNU | |
| 44 | | SA | |
| 45 | | SA | |
| 46 | | SA | |
| 47 | | SA | |
| 48 | | SA | |
| 49 | | SA | |
| 50 | | SA | |

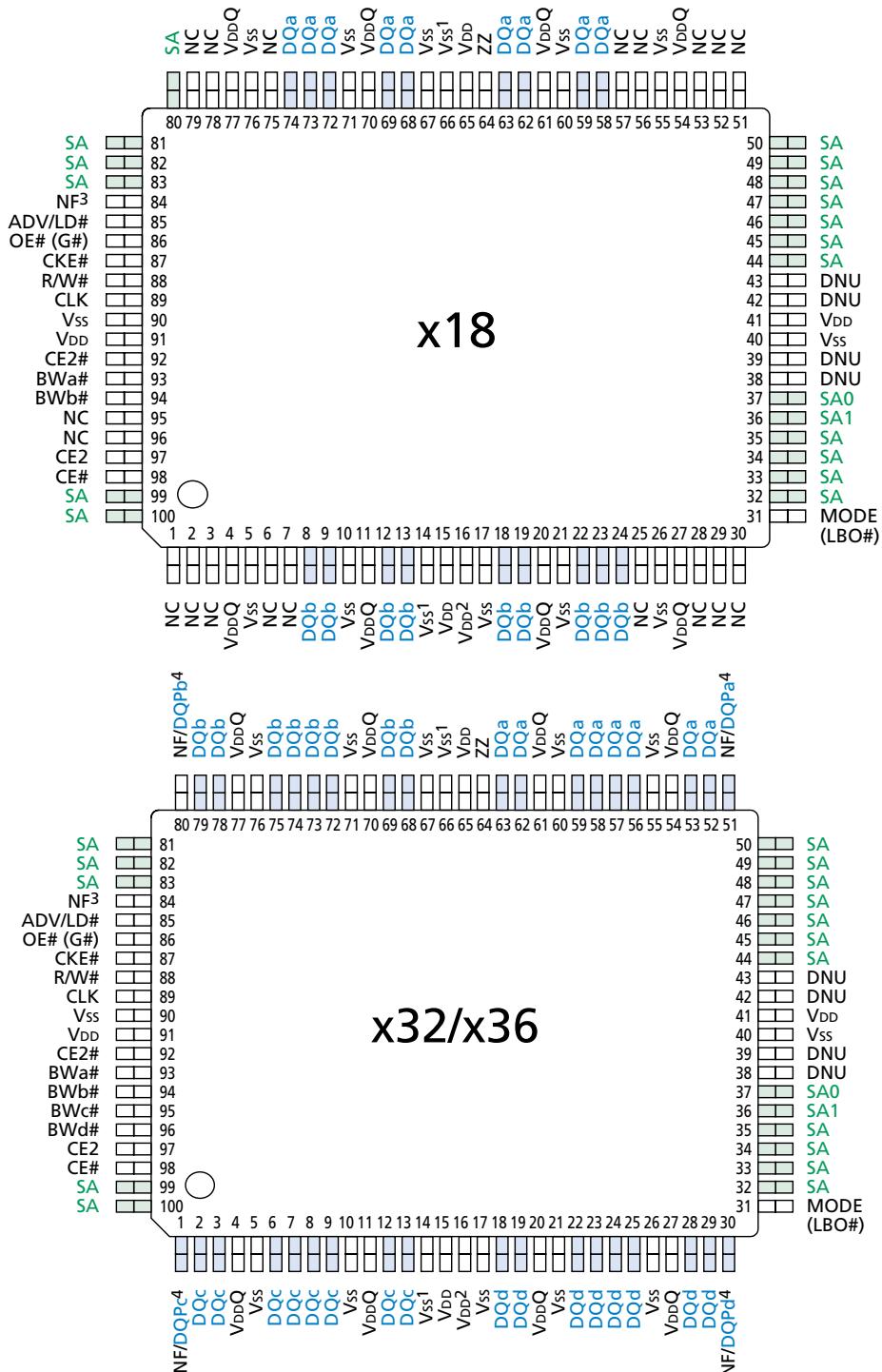
| PIN # | x18 | x32 | x36 |
|-------|-----|------|------|
| 51 | NC | NF | DQPA |
| 52 | NC | DQA | DQA |
| 53 | NC | DQA | DQA |
| 54 | | VDDQ | |
| 55 | | VSS | |
| 56 | NC | DQA | DQA |
| 57 | NC | DQA | DQA |
| 58 | | DQA | |
| 59 | | DQA | |
| 60 | | VSS | |
| 61 | | VDDQ | |
| 62 | | DQA | |
| 63 | | DQA | |
| 64 | | ZZ | |
| 65 | | VDD | |
| 66 | | VSS | |
| 67 | | VSS | |
| 68 | DQA | DQB | DQB |
| 69 | DQA | DQB | DQB |
| 70 | | VDDQ | |
| 71 | | VSS | |
| 72 | DQA | DQB | DQB |
| 73 | DQA | DQB | DQB |
| 74 | DQA | DQB | DQB |
| 75 | NC | DQB | DQB |

| PIN # | x18 | x32 | x36 |
|-------|-----|-----------------|------|
| 76 | | VSS | |
| 77 | | VDDQ | |
| 78 | NC | DQB | DQB |
| 79 | NC | DQB | DQB |
| 80 | SA | NF | DQPB |
| 81 | | SA | |
| 82 | | SA | |
| 83 | | SA | |
| 84 | | NF ³ | |
| 85 | | ADV/LD# | |
| 86 | | OE# (G#) | |
| 87 | | CKE# | |
| 88 | | R/W# | |
| 89 | | CLK | |
| 90 | | VSS | |
| 91 | | VDD | |
| 92 | | CE2# | |
| 93 | | BWA# | |
| 94 | | BWB# | |
| 95 | NC | BWC# | BWC# |
| 96 | NC | BWD# | BWD# |
| 97 | | CE2 | |
| 98 | | CE# | |
| 99 | | SA | |
| 100 | | SA | |

NOTE: 1. Pins 14 and 66 do not have to be connected directly to VSS if the input voltage is $\leq V_{IL}$.
 2. Pins 16 does not have to be connected directly to VDD if the input voltage is $\geq V_{IH}$.
 3. Pin 84 is reserved for address expansion to 18Mb device.

PIN ASSIGNMENT (TOP VIEW)

100-PIN TQFP



NOTE:

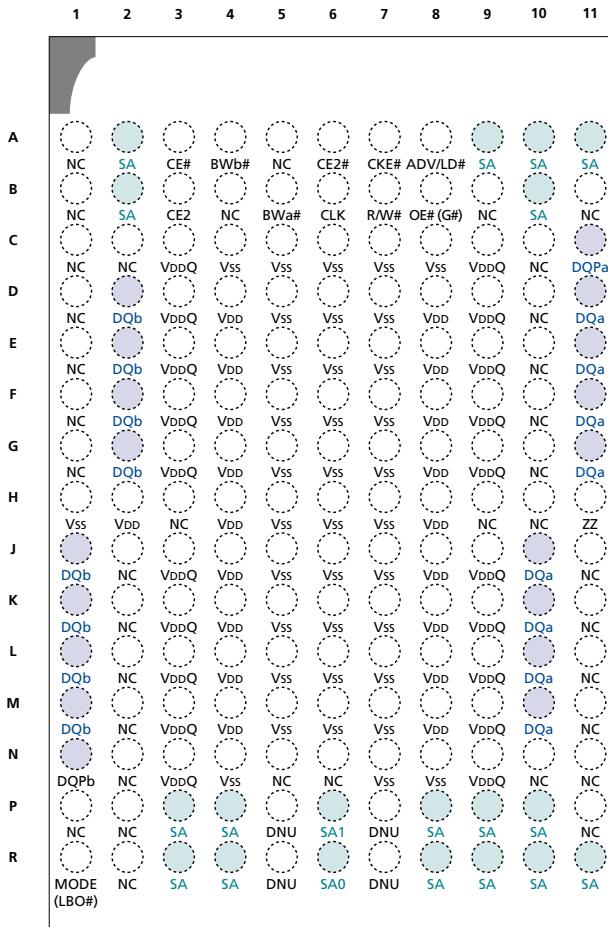
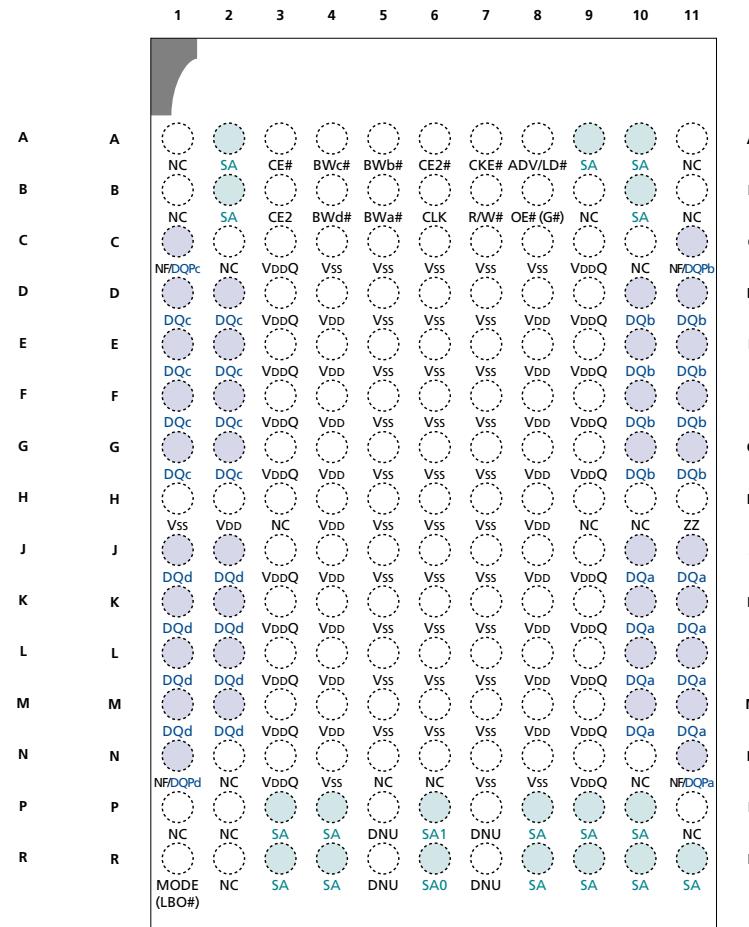
1. Pins 14 and 66 do not have to be connected directly to V_{SS} if the input voltage is $\leq V_{IL}$.
2. Pins 16 does not have to be connected directly to V_{DD} if the input voltage is $\geq V_{IH}$.
3. Pin 84 is reserved for address expansion to 18Mb device.
4. NF for x32 version, DQPx for x36 version.

TQFP PIN DESCRIPTIONS

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|--|------------------------------|-------------|---|
| 37 36 32-35, 44-50, 80-83, 99, 100 | 37 36 32-35, 44-50, 81-83, 99, 100 | SA0 SA1 SA | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pin 84 is reserved as an address bit for the higher-density 18Mb ZBT SRAM. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired. |
| 93 94 – – | 93 94 95 96 | BWa# BWb# BWc# BWd# | Input | Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITES need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins. |
| 89 | 89 | CLK | Input | Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| 98 | 98 | CE# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# is LOW). |
| 92 | 92 | CE2# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# is LOW). This input can be used for memory depth expansion. |
| 97 | 97 | CE2 | Input | Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# is LOW). This input can be used for memory depth expansion. |
| 86 | 86 | OE# (G#) | Input | Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#. |
| 85 | 85 | ADV/LD# | Input | Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge. |
| 87 | 87 | CKE# | Input | Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK. |
| 64 | 64 | ZZ | Input | Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. |

TQFP PIN DESCRIPTIONS (CONTINUED)

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|--|--|--------------|--|
| 88 | 88 | R/W# | Input | Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW. |
| 31 | 31 | MODE (LBO#) | Input | Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE. |
| (a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24 | (a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29 | DQa DQb DQc DQd | Input/Output | SRAM Data I/Os: Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge CLK. |
| n/a | 51 80 1 30 | NF/DQPa NF/DQPb NF/DQPC NF/DQPd | NF/I/O | No Function/Data Bits: On the x32 version, these pins are No Function (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs. |
| 15, 16, 41, 65, 91 | 15, 16, 41, 65, 91 | VDD | Supply | Power Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 4, 11, 20, 27, 54, 61, 70, 77 | 4, 11, 20, 27, 54, 61, 70, 77 | VDDQ | Supply | Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90 | 5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90 | Vss | Supply | Ground: GND. |
| 1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96 | n/a | NC | - | No Connect: These pins can be left floating or connected to GND to minimize thermal impedance. |
| 38, 39, 42, 43 | 38, 39, 42, 43 | DNU | - | Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance. |
| 84 | 84 | NF | - | No Function: This pin is internally connected to the die and will have the capacitance of an input pin. It is allowable to leave this pin unconnected or driven by signals. Pin 84 is reserved as an address pin for the 18Mb ZBT SRAM. |

**PIN LAYOUT (TOP VIEW)
165-PIN FBGA**
x18

TOP VIEW
x32/x36

TOP VIEW

*No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.

NOTE: Pin 9B is reserved for address expansion to 18Mb.

FBGA PIN DESCRIPTIONS

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|---|------------------------------|-------------|---|
| 6R 6P 2A, 9A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 10A, 10B, 10P, 10R, 11A, 11R | 6R 6P 2A, 9A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11R | SA0 SA1 SA | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. |
| 5B 4A — — | 5B 5A 4A 4B | BWa# BWb# BWc# BWd# | Input | Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. For the x32 and x36 versions, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPC; BWd# controls DQd's and DQPD. Parity is only available on the x18 and x36 versions. |
| 7A | 7A | CKE# | Input | Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet the setup and hold times around the rising edge of CLK. |
| 7B | 7B | R/W# | Input | Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations to meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW. |
| 6B | 6B | CLK | Input | Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| 3A | 3A | CE# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device. CE# is sampled only when a new external address is loaded. (ADV/LD# is LOW) |
| 6A | 6A | CE2# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded. |
| 11H | 11H | ZZ | Input | Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. |
| 3B | 3B | CE2 | Input | Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded. |
| 8B | 8B | OE#(G#) | Input | Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. |

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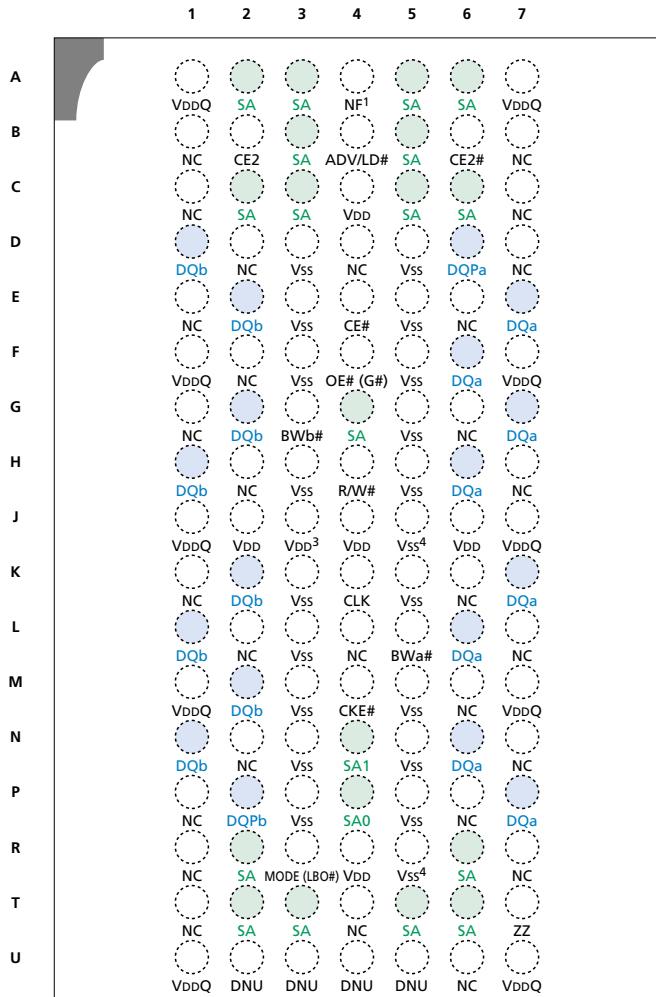
FBGA PIN DESCRIPTIONS (continued)

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|--|--|--------------|--|
| 8A | 8A | ADV/LD# | Input | Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge. |
| 1R | 1R | MODE (LB0#) | Input | Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating. |
| (a) 10J, 10K, 10L, 10M, 11D, 11E, 11F, 11G (b) 1J, 1K, 1L, 1M, 2D, 2E, 2F, 2G | (a) 10J, 10K, 10L, 10M, 11J, 11K, 11L, 11M (b) 10D, 10E, 10F, 10G, 11D, 11E, 11F, 11G (c) 1D, 1E, 1F, 1G, 2D, 2E, 2F, 2G (d) 1J, 1K, 1L, 1M, 2J, 2K, 2L, 2M | DQa DQb DQc DQd | Input/Output | SRAM Data I/Os: For the x18 version, Byte "a" is associated DQas; Byte "b" is associated with DQbs. For the x32 and x36 versions, Byte "a" is associated with DQas; Byte "b" is associated with DQbs; Byte "c" is associated with DQcs; Byte "d" is associated with DQds. Input data must meet setup and hold times around the rising edge of CLK. |
| 11C 1N - - | 11N 11C 1C 1N | NF/DQPa NF/DQPB NF/DQPC NF/DQPD | NF/I/O | No Function/Parity Data I/Os: On the x32 version, these are No Function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPB. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPB; Byte "c" parity is DQPC; Byte "d" parity is DQPD. |
| 2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M | 2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M | V _{DD} | Supply | Power Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N | 3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N | V _{DDQ} | Supply | Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range. |

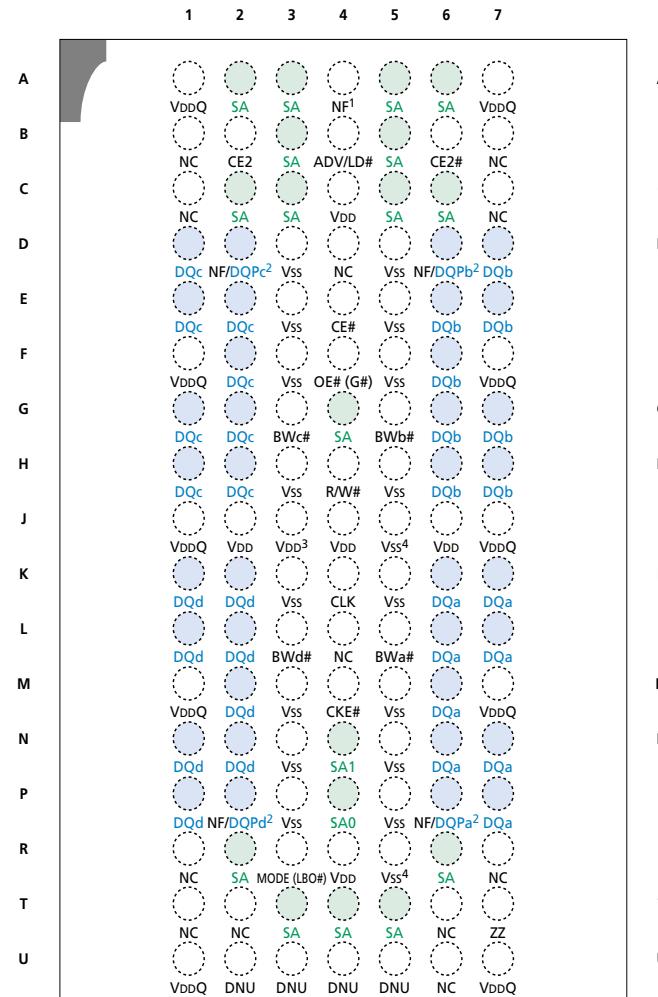
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FBGA PIN DESCRIPTIONS (continued)

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|--|---------------|-------------|---|
| 1H, 4C, 4N, 5C, 5D, 5E, 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N | 1H, 4C, 4N, 5C, 5D, 5E, 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N | Vss | Supply | Ground: GND. |
| 5P, 5R, 7P, 7R | 5P, 5R, 7P, 7R | DNU | — | Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation. |
| 1A, 1B, 1C, 1D, 1E, 1F, 1G, 1P, 2C, 2J, 2K, 2L, 2M, 2N, 2P, 2R, 3H, 4B, 9B, 5A, 5N, 6N, 9H, 10C, 10D, 10E, 10F, 10G, 10H, 10N, 11B, 11J, 11K, 11L, 11M, 11N, 11P | 1A, 1B, 1P, 2C, 2N, 2P, 2R, 3H, 5N, 6N, 9B, 9H, 10C, 10H, 10N, 11A, 11B, 11P | NC | — | No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. Pin 9B is reserved for 16MB address expansion. |
| | | NF | — | No Function: These pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals. |

**PIN LAYOUT (TOP VIEW)
119-PIN BGA**
x18


TOP VIEW

x32/x36


TOP VIEW

NOTE:

1. Pin 4A is reserved for address expansion to 18Mb.
2. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
3. Pin 3J does not have to be connected directly to Vdd if the input voltage is $\geq V_{IH}$.
4. Pins 5J and 5R do not have to be connected directly to Vss if the input voltage is $\leq V_{IH}$.

BGA PIN DESCRIPTIONS

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|--|------------------------------|-------------|---|
| 4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T | 4P 4N 2A, 2C, 2R, 3A, 3B, 3C, 3T, 4T, 5A, 5B, 5C, 5T, 6A, 6C, 6R | SA0 SA1 SA | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. |
| 5L 3G - - | 5L 5G 3G 3L | BWa# BWb# BWc# BWd# | Input | Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQNb. For the x32 and x36 versions, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQNb; BWc# controls DQc's and DQNc; BWd# controls DQd's and DQNd. Parity is only available on the x18 and x36 versions. |
| 4M | 4M | CKE# | Input | Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CK input and effectively internally extends the previous CLK cycle. This input must meet the setup and hold times around the rising edge of CLK. |
| 4H | 4H | R/W# | Input | Read/Write: This input determines the cycle type when ADV/LD# is IOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW. |
| 4K | 4K | CLK | Input | Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| 4E | 4E | CE# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device. CE# is sampled only when a new external address is loaded. |
| 6B | 6B | CE2# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded. |
| 7T | 7T | ZZ | Input | Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. |
| 2B | 2B | CE2 | Input | Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded. |

(continued on next page)

BGA PIN DESCRIPTIONS (continued)

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|--|--|--------------|---|
| 4F | 4F | OE# | Input | Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. |
| 4B | 4B | ADV#/LD# | Input | Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV#/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge. |
| 3R | 3R | MODE | Input | Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating. |
| 4A | 4A | NF | Input | No Function: These pins are internally connected to the die and will have the capacitance of input pins. It is allowable to leave these pins unconnected or driven by signals. These pins are reserved for address expansion; 4A becomes an SA at 18Mb density. |
| (a) 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b) 1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M | (a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H, 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N | DQa DQb DQc DQd | Input/Output | SRAM Data I/Os: For the x18 version, Byte "a" is DQa's; Byte "b" is DQb's. For the x32 and x36 versions, Byte "a" is DQa's; Byte "b" is DQb's; Byte "c" is DQc's; Byte "d" is DQd's. Input data must meet setup and hold times around the rising edge of CLK. |
| 6D 2P - - | 6P 6D 2D 2P | NF/DQPa NF/DQPB NF/DQPC NF/DQPD | NF/I/O | No Function/Parity Data I/Os: On the x32 version, these are No Function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPB. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPB; Byte "c" parity is DQPC; Byte "d" parity is DQPD. |
| 2J, 4C, 4J, 4R, 5R, 6J | 2J, 4C, 4J, 4R, 5R, 6J | V _{DD} | Supply | Power Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U | 1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U | V _{DDQ} | Supply | Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range. |

(continued on next page)

BGA PIN DESCRIPTIONS (continued)

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|---|-----------------|-------------|---|
| 3D, 3E, 3F, 3H, 3K, 3L, 3M, 3N, 3P, 5D, 5E, 5F, 5G, 5H, 5K, 5M, 5N, 5P | 3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P | V _{ss} | Supply | Ground: GND. |
| 2U, 3U, 4U, 5U | 2U, 3U, 4U, 5U | DNU | - | Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation. |
| 1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2D, 2F, 2H, 2L, 2N, 3J, 4D, 4L, 4T, 5J, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R | 1B, 1C, 1R, 1T, 2T, 3J, 4D, 4L, 5J, 6T, 6U, 7B, 7C, 7R | NC | - | No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. |
| | | NF | I/O | No Function: These pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals. |

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

| FIRST ADDRESS (EXTERNAL) | SECOND ADDRESS (INTERNAL) | THIRD ADDRESS (INTERNAL) | FOURTH ADDRESS (INTERNAL) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X00 | X...X11 | X...X10 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X10 | X...X01 | X...X00 |

LINEAR BURST ADDRESS TABLE (MODE = LOW)

| FIRST ADDRESS (EXTERNAL) | SECOND ADDRESS (INTERNAL) | THIRD ADDRESS (INTERNAL) | FOURTH ADDRESS (INTERNAL) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X10 | X...X11 | X...X00 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X00 | X...X01 | X...X10 |

PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x18)

| FUNCTION | R/W# | BWa# | BWb# |
|-----------------|------|------|------|
| READ | H | X | X |
| WRITE Byte "a" | L | L | H |
| WRITE Byte "b" | L | H | L |
| WRITE All Bytes | L | L | L |
| WRITE ABORT/NOP | L | H | H |

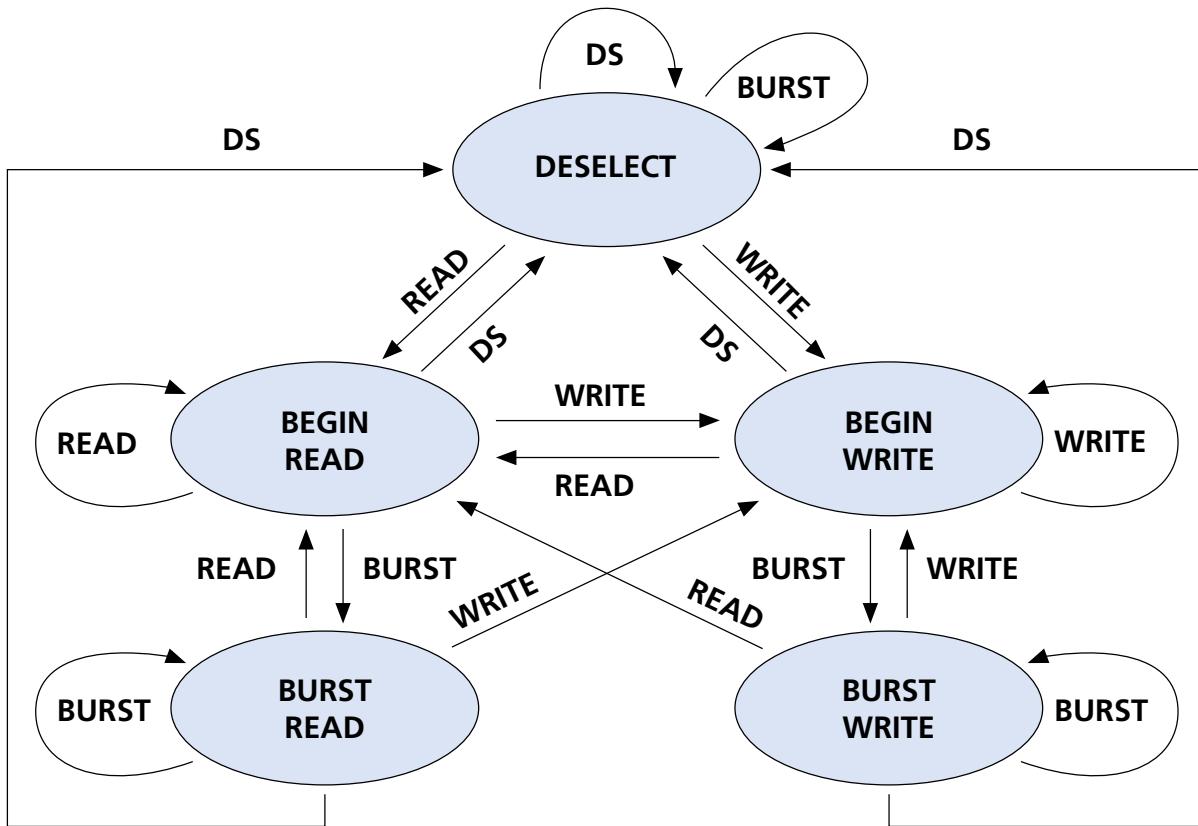
NOTE: Using R/W# and byte write(s), any one or more bytes may be written.

PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x32/x36)

| FUNCTION | R/W# | BWa# | BWb# | BWc# | BWd# |
|-----------------|------|------|------|------|------|
| READ | H | X | X | X | X |
| WRITE Byte "a" | L | L | H | H | H |
| WRITE Byte "b" | L | H | L | H | H |
| WRITE Byte "c" | L | H | H | L | H |
| WRITE Byte "d" | L | H | H | H | L |
| WRITE All Bytes | L | L | L | L | L |
| WRITE ABORT/NOP | L | H | H | H | H |

NOTE: Using R/W# and byte write(s), any one or more bytes may be written.

STATE DIAGRAM FOR ZBT SRAM



KEY:

| COMMAND | OPERATION |
|---------|--|
| DS | DESELECT |
| READ | New READ |
| WRITE | New WRITE |
| BURST | BURST READ, BURST WRITE or CONTINUE DESELECT |

NOTE: 1. A STALL or IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE# HIGH only blocks the clock (CLK) input and does not change the state of the device.
 2. States change on the rising edge of the clock (CLK).

TRUTH TABLE

(Notes 5-10)

| OPERATION | ADDRESS USED | CE# | CE2# | CE2 | ZZ | ADV/ LD# | R/W# | BWx | OE# | CKE# | CLK | DQ | NOTES |
|----------------------------------|--------------|-----|------|-----|----|----------|------|-----|-----|------|-----|--------|----------------|
| DESELECT Cycle | None | H | X | X | L | L | X | X | X | L | L-H | High-Z | |
| DESELECT Cycle | None | X | H | X | L | L | X | X | X | L | L-H | High-Z | |
| DESELECT Cycle | None | X | X | L | L | L | X | X | X | L | L-H | High-Z | |
| CONTINUE DESELECT Cycle | None | X | X | X | L | H | X | X | X | L | L-H | High-Z | 1 |
| READ Cycle (Begin Burst) | External | L | L | H | L | L | H | X | L | L | L-H | Q | |
| READ Cycle (Continue Burst) | Next | X | X | X | L | H | X | X | L | L | L-H | Q | 1, 11 |
| NOP/DUMMYREAD (Begin Burst) | External | L | L | H | L | L | H | X | H | L | L-H | High-Z | 2 |
| DUMMYREAD (Continue Burst) | Next | X | X | X | L | H | X | X | H | L | L-H | High-Z | 1, 2, 11 |
| WRITE Cycle (Begin Burst) | External | L | L | H | L | L | L | L | X | L | L-H | D | 3 |
| WRITE Cycle (Continue Burst) | Next | X | X | X | L | H | X | L | X | L | L-H | D | 1, 3, 11 |
| NOP/WRITE ABORT (Begin Burst) | None | L | L | H | L | L | L | H | X | L | L-H | High-Z | 2, 3 |
| WRITE ABORT (Continue Burst) | Next | X | X | X | L | H | X | H | X | L | L-H | High-Z | 1, 2, 3, 11 |
| IGNORE CLOCK EDGE (Stall) | Current | X | X | X | L | X | X | X | X | H | L-H | - | 4 |
| SNOOZE MODE | None | X | X | X | H | X | X | X | X | X | X | High-Z | |

NOTE:

1. CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is executed first.
2. DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.
3. OE# may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. OE# may be used when the bus turn-on and turn-off times do not meet an application's requirements.
4. If an IGNORE CLOCK EDGE command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the IGNORE CLOCK EDGE cycle.
5. X means "Don't Care." H means logic HIGH. L means logic LOW. BWx = H means all byte write signals (BWa#, BWb#, BWc# and BWd#) are HIGH. BWx = L means one or more byte write signals are LOW.
6. BWa# enables WRITES to Byte "a" (DQa pins); BWb# enables WRITES to Byte "b" (DQb pins); BWc# enables WRITES to Byte "c" (DQc pins); BWd# enables WRITES to Byte "d" (DQd pins).
7. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
8. Wait states are inserted by setting CKE# HIGH.
9. This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.
10. The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST cycle.
11. The address counter is incremented for all CONTINUE BURST cycles.

ABSOLUTE MAXIMUM RATINGS*

| | |
|------------------------------|----------------------------|
| Voltage on VDD Supply | |
| Relative to Vss | -0.5V to +4.6V |
| Voltage on VDDQ Supply | |
| Relative to Vss | -0.5V to VDD |
| VIN | -0.5V to VDDQ + 0.5V |
| Storage Temperature (TQFP) | -55°C to +150°C |
| Storage Temperature (FBGA) | -55°C to +125°C |
| Junction Temperature** | +150°C |
| Short Circuit Output Current | 100mA |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ TA ≤ +70°C; VDD, VDDQ = +3.3V ± 0.165V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|-------------------------------|---------------------------------------|--------|-------|-----------|-------|-------|
| Input High (Logic 1) Voltage | | VIH | 2.0 | VDD + 0.3 | V | 1, 2 |
| Input High (Logic 1) Voltage | DQ pins | VIH | 2.0 | VDD + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | | VIL | -0.3 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ VIN ≤ VDD | ILI | -1.0 | 1.0 | µA | 3 |
| Output Leakage Current | Output(s) disabled, 0V ≤ VIN ≤ VDD | ILo | -1.0 | 1.0 | µA | |
| Output High Voltage | IOH = -4.0mA | VOH | 2.4 | | V | 1, 4 |
| Output Low Voltage | IOL = 8.0mA | VOI | | 0.4 | V | 1, 4 |
| Supply Voltage | | VDD | 3.135 | 3.465 | V | 1 |
| Isolated Output Buffer Supply | | VDDQ | 3.135 | VDD | V | 1, 5 |

NOTE:

1. All voltages referenced to Vss (GND).
2. Overshoot: $VIH \leq +4.6V$ for $t \leq t_{KHKH}/2$ for $I \leq 20mA$
Undershoot: $VIL \geq -0.7V$ for $t \leq t_{KHKH}/2$ for $I \leq 20mA$
Power-up: $VIH \leq +3.465V$ and $VDD \leq +3.135V$ for $t \leq 200ms$
3. MODE pin has an internal pull-up, and input leakage = $\pm 10\mu A$.
4. The load used for VOH, VOI testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
5. VDDQ should never exceed VDD. VDD and VDDQ can be externally wired together to the same power supply.

2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; $V_{DD} = +3.3V \pm 0.165V$; $V_{DDQ} = +2.5V \pm 0.4V/-0.125V$ unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|-------------------------------|--|-----------|-------|-----------------|---------|-------|
| Input High (Logic 1) Voltage | Data bus (DQx) | V_{IHQ} | 1.7 | $V_{DDQ} + 0.3$ | V | 1, 2 |
| | Inputs | V_{IH} | 1.7 | $V_{DD} + 0.3$ | V | 1, 2 |
| Input Low (Logic 0) Voltage | | V_{IL} | -0.3 | 0.7 | V | 1, 2 |
| Input Leakage Current | $0V \leq V_{IN} \leq V_{DD}$ | I_{LI} | -1.0 | 1.0 | μA | 3 |
| Output Leakage Current | Output(s) disabled, $0V \leq V_{IN} \leq V_{DDQ}$ (DQx) | I_{LO} | -1.0 | 1.0 | μA | |
| Output High Voltage | $I_{OH} = -2.0mA$ | V_{OH} | 1.7 | – | V | 1 |
| | $I_{OH} = -1.0mA$ | V_{OH} | 2.0 | – | V | 1 |
| Output Low Voltage | $I_{OL} = 2.0mA$ | V_{OL} | – | 0.7 | V | 1 |
| | $I_{OL} = 1.0mA$ | V_{OL} | – | 0.4 | V | 1 |
| Supply Voltage | | V_{DD} | 3.135 | 3.465 | V | 1 |
| Isolated Output Buffer Supply | | V_{DDQ} | 2.375 | 2.9 | V | 1 |

TQFP CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS | NOTES |
|-------------------------------|--|----------|-----|-----|-------|-------|
| Control Input Capacitance | $T_A = +25^\circ C$; $f = 1$ MHz $V_{DD} = 3.3V$ | C_I | 3 | 4 | pF | 1 |
| Input/Output Capacitance (DQ) | | C_O | 4 | 5 | pF | 1 |
| Address Capacitance | | C_A | 3 | 3.5 | pF | 1 |
| Clock Capacitance | | C_{CK} | 3 | 3.5 | pF | 1 |

BGA CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS | NOTES |
|-----------------------------------|---|----------|-----|-----|-------|-------|
| Address/Control Input Capacitance | $T_A = 25^\circ C$; $f = 1$ MHz $V_{DD} = 3.3V$ | C_I | 4 | 7 | pF | 1 |
| Input/Output Capacitance (DQ) | | C_O | 4.5 | 5.5 | pF | 1 |
| Address Capacitance | | C_A | 4 | 7 | pF | 1 |
| Clock Capacitance | | C_{CK} | 4.5 | 5.5 | pF | 1 |

FBGA CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS | NOTES |
|-----------------------------------|----------------------------------|----------|-----|-----|-------|-------|
| Address/Control Input Capacitance | $T_A = 25^\circ C$; $f = 1$ MHz | C_I | 2.5 | 3.5 | pF | 4 |
| Output Capacitance (Q) | | C_O | 4 | 5 | pF | 4 |
| Clock Capacitance | | C_{CK} | 2.5 | 3.5 | pF | 4 |

NOTE:

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +4.6V$ for $t \leq t_{KHKH}/2$ for $I \leq 20mA$
Undershoot: $V_{IL} \geq -0.7V$ for $t \leq t_{KHKH}/2$ for $I \leq 20mA$
Power-up: $V_{IH} \leq +3.465V$ and $V_{DD} \leq +3.135V$ for $t \leq 200ms$
3. MODE pin has an internal pull-up, and input leakage = $\pm 10\mu A$.
4. This parameter is sampled.

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Note 1) (0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | | | UNITS | NOTES |
|---------------------------------|---|-------------------|-----|-----|-----|-----|-------|---------|
| | | | | -10 | -11 | -12 | | |
| Power Supply Current: Operating | Device selected; All inputs ≤ V _{IL} or ≥ V _{IH} ; Cycle time ≥ ^t KC (MIN); V _{DD} = MAX; Outputs open | I _{DD} | 165 | 300 | 275 | 250 | mA | 2, 3, 4 |
| Power Supply Current: Idle | Device selected; V _{DD} = MAX; CKE# ≥ V _{IH} ; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; Cycle time ≥ ^t KC (MIN) | I _{DD1} | 10 | 28 | 22 | 20 | mA | 2, 3, 4 |
| CMOS Standby | Device deselected; V _{DD} = MAX; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; All inputs static; CLK frequency = 0 | I _{SB2} | 0.5 | 10 | 10 | 10 | mA | 3, 4 |
| TTL Standby | Device deselected; V _{DD} = MAX; All inputs ≤ V _{IL} or ≥ V _{IH} ; All inputs static; CLK frequency = 0 | I _{SB3} | 6 | 25 | 25 | 25 | mA | 3, 4 |
| Clock Running | Device deselected; V _{DD} = MAX; ADV/LD# ≥ V _{IH} ; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; Cycle time ≥ ^t KC (MIN) | I _{SB4} | 37 | 65 | 65 | 60 | mA | 3, 4 |
| SnoozeMode | ZZ ≥ V _{IH} | I _{SB2Z} | 0.5 | 10 | 10 | 10 | mA | 4 |

TQFP THERMAL RESISTANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | UNITS | NOTES |
|--|--|-----------------|-----|-------|-------|
| Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | θ _{JA} | 40 | °C/W | 5 |
| Thermal Resistance (Junction to Top of Case) | | θ _{JC} | 8 | °C/W | 5 |

BGA THERMAL RESISTANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | UNITS | NOTES |
|---------------------------------------|--|-----------------|-----|-------|-------|
| Junction to Ambient (Airflow of 1m/s) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | θ _{JA} | 40 | °C/W | 5 |
| Junction to Case (Top) | | θ _{JC} | 9 | °C/W | 5 |

NOTE:

1. V_{DDQ} = +3.3V ±0.165V for 3.3V I/O configuration; V_{DDQ} = +2.5V +0.4V/-0.125V for 2.5V I/O configuration.
2. I_{DD} is specified with no output current and increases with faster cycle times. I_{DDQ} increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in a deselected cycle as defined in the truth table. "Device selected" means device is active (not in deselected mode).
4. Typical values are measured at +3.3V, +25°C and 12ns cycle time.
5. This parameter is sampled.

FBGA THERMAL RESISTANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | UNITS | NOTES |
|---------------------------------------|--|---------------|-----|-------|-------|
| Junction to Ambient (Airflow of 1m/s) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | θ_{JA} | 40 | °C/W | 1, 11 |
| Junction to Case (Top) | | θ_{JC} | 9 | °C/W | 1, 11 |
| Junction to Pins (Bottom) | | θ_{JB} | 17 | °C/W | 1, 11 |

AC ELECTRICAL CHARACTERISTICS

(Notes 2, 3, 4) (0°C ≤ T_A ≤ +70°C; $V_{DD} = +3.3V \pm 0.165V$ unless otherwise noted)

| DESCRIPTION | SYMBOL | -10 | | -11 | | -12 | | UNITS | NOTES |
|---------------------------|-------------|-----|-----|-----|-----|-----|-----|-------|------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Clock | | | | | | | | | |
| Clock cycle time | t_{KHKH} | 10 | | 11 | | 12 | | ns | |
| Clock frequency | f_{KF} | | 100 | | 90 | | 83 | MHz | |
| Clock HIGH time | t_{KHKL} | 2.5 | | 3.0 | | 3.0 | | ns | 5 |
| Clock LOW time | t_{KLKH} | 2.5 | | 3.0 | | 3.0 | | ns | 5 |
| Output Times | | | | | | | | | |
| Clock to output valid | t_{KHQV} | | 7.5 | | 8.5 | | 9.0 | ns | |
| Clock to output invalid | t_{KHQX} | 3.0 | | 3.0 | | 3.0 | | ns | 6 |
| Clock to output in Low-Z | t_{KHQX1} | 3.0 | | 3.0 | | 3.0 | | ns | 6, 7, 8, 9 |
| Clock to output in High-Z | t_{KHZQ} | | 5.0 | | 5.0 | | 5.0 | ns | 6, 7, 8, 9 |
| OE# to output valid | t_{GLQV} | | 5.0 | | 5.0 | | 5.0 | ns | 2 |
| OE# to output in Low-Z | t_{GLQX} | 0 | | 0 | | 0 | | ns | 6, 7, 8, 9 |
| OE# to output in High-Z | t_{GHQZ} | | 5.0 | | 5.0 | | 5.0 | ns | 6, 7, 8, 9 |
| Setup Times | | | | | | | | | |
| Address | t_{AVKH} | 2.0 | | 2.2 | | 2.5 | | ns | 10 |
| Clock enable (CKE#) | t_{EVKH} | 2.0 | | 2.2 | | 2.5 | | ns | 10 |
| Control signals | t_{CVKH} | 2.0 | | 2.2 | | 2.5 | | ns | 10 |
| Data-in | t_{DVKH} | 2.0 | | 2.2 | | 2.5 | | ns | 10 |
| Hold Times | | | | | | | | | |
| Address | t_{KHAX} | 0.5 | | 0.5 | | 0.5 | | ns | 10 |
| Clock enable (CKE#) | t_{KHEX} | 0.5 | | 0.5 | | 0.5 | | ns | 10 |
| Control signals | t_{KHCX} | 0.5 | | 0.5 | | 0.5 | | ns | 10 |
| Data-in | t_{KHDX} | 0.5 | | 0.5 | | 0.5 | | ns | 10 |

NOTE:

1. This parameter is sampled.
2. OE# can be considered a "Don't Care" during WRITEs; however, controlling OE# can help fine-tune a system for turnaround timing.
3. Test conditions as specified with output loading as shown in Figure 1 for 3.3V I/O ($V_{DDQ} = +3.3V \pm 0.165V$) and Figure 3 for 2.5V I/O ($V_{DDQ} = +2.5V \pm 0.4V/-0.125V$).
4. A WRITE cycle is defined by R/W# LOW having been registered into the device at ADV/LD# LOW. A READ cycle is defined by R/W# HIGH with ADV/LD# LOW. Both cases must meet setup and hold times.
5. Measured as HIGH above V_{IH} and LOW below V_{IL} .
6. Refer to Technical Note TN-55-01, "Designing with ZBT SRAMs," for a more thorough discussion on these parameters.
7. This parameter is sampled.
8. This parameter is measured with output loading as shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O.
9. Transition is measured $\pm 200mV$ from steady state voltage.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when they are being registered into the device. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when ADV/LD# is LOW to remain enabled.
11. Preliminary package data.

3.3V I/O AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input pulse levels | Vss to 3.3V |
| Input rise and fall times | 1ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

2.5V I/O AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input pulse levels | Vss to 2.5V |
| Input rise and fall times | 1ns |
| Input timing reference levels | 1.25V |
| Output reference levels | 1.25V |
| Output load | See Figures 3 and 4 |

3.3V I/O Output Load Equivalents

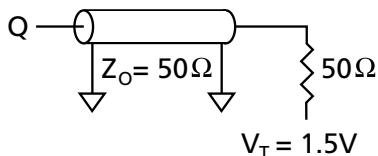


Figure 1

2.5V I/O Output Load Equivalents

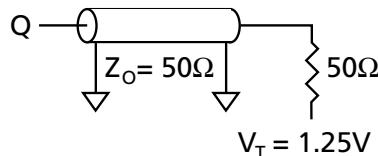


Figure 3

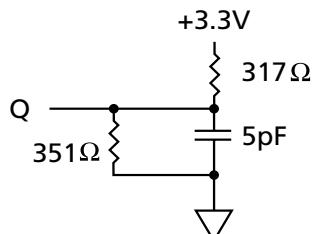


Figure 2

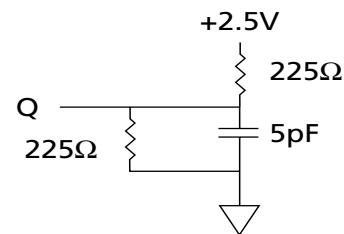


Figure 4

LOAD DERATING CURVES

The Micron 512K x 18, 256K x 32, and 256K x 36 ZBT SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

SNOOZE MODE

SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to I_{SB2Z} . The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When

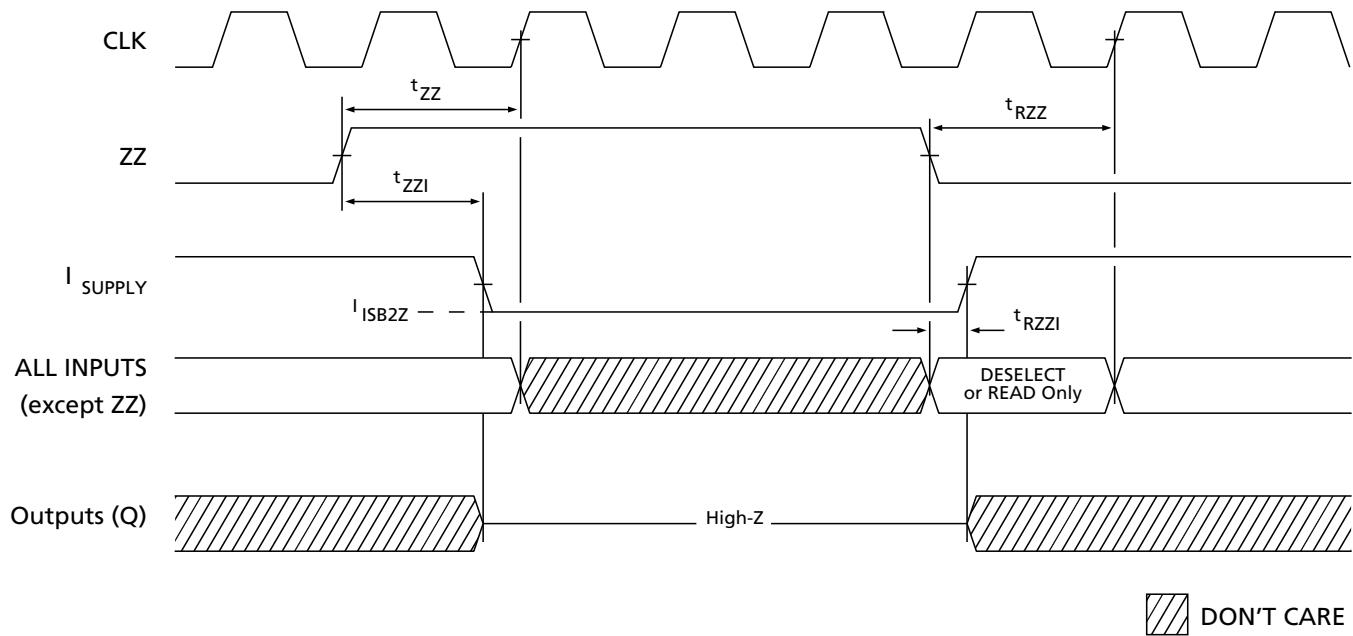
the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the time t_{ZZI} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during t_{RZZ} , only a DESELECT or READ cycle should be given.

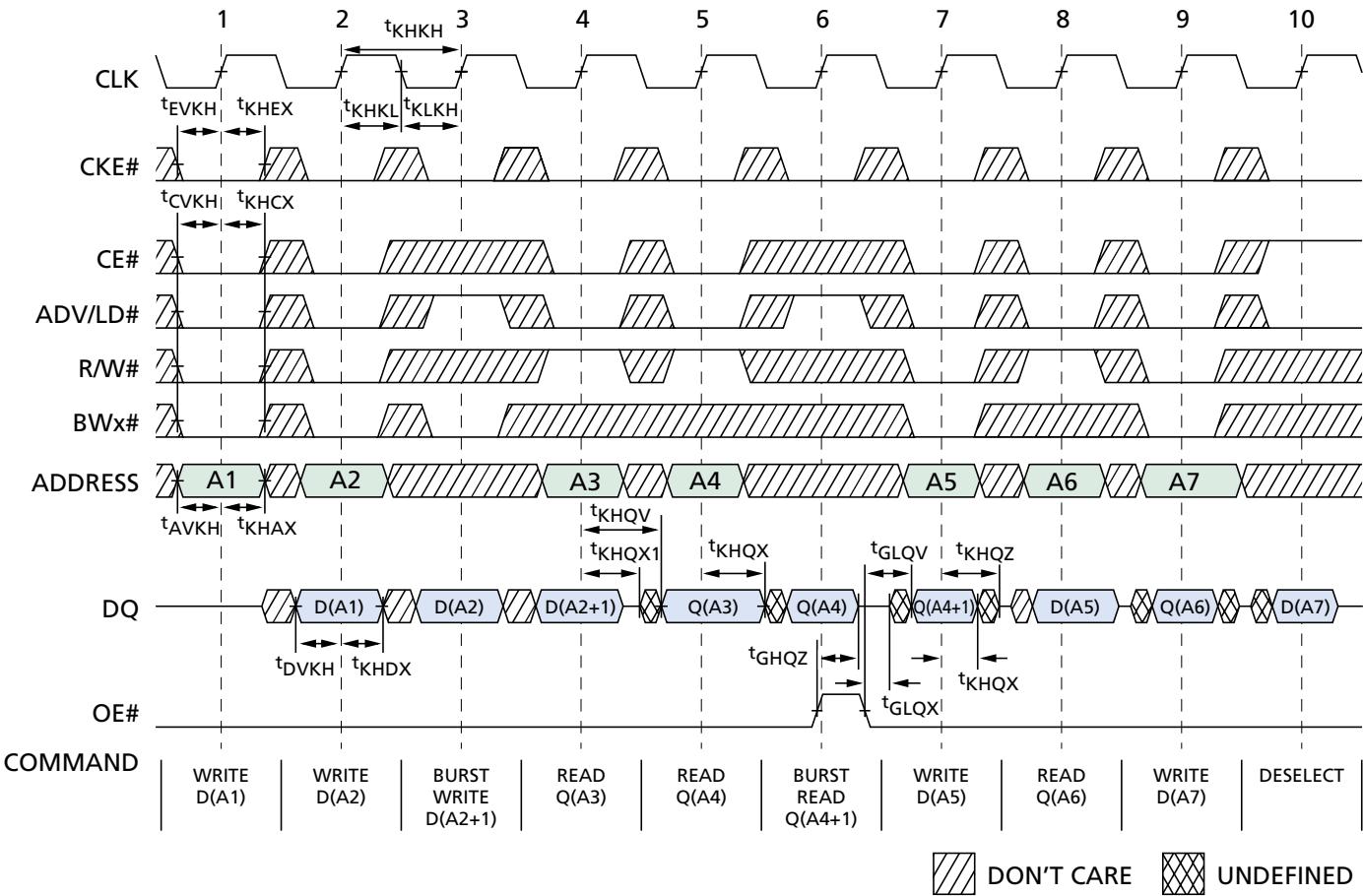
SNOOZE MODE ELECTRICAL CHARACTERISTICS

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------------|------------------|------------|-----|-----------|-------|-------|
| Current during SNOOZE MODE | $ZZ \geq V_{IH}$ | I_{SB2Z} | | 10 | mA | |
| ZZ active to input ignored | | t_{ZZ} | 0 | t_{KHH} | ns | 1 |
| ZZ inactive to input sampled | | t_{RZZ} | 0 | t_{KHH} | ns | 1 |
| ZZ active to snooze current | | t_{ZZI} | | t_{KHH} | ns | 1 |
| ZZ inactive to exit snooze current | | t_{RZZI} | 0 | | ns | 1 |

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



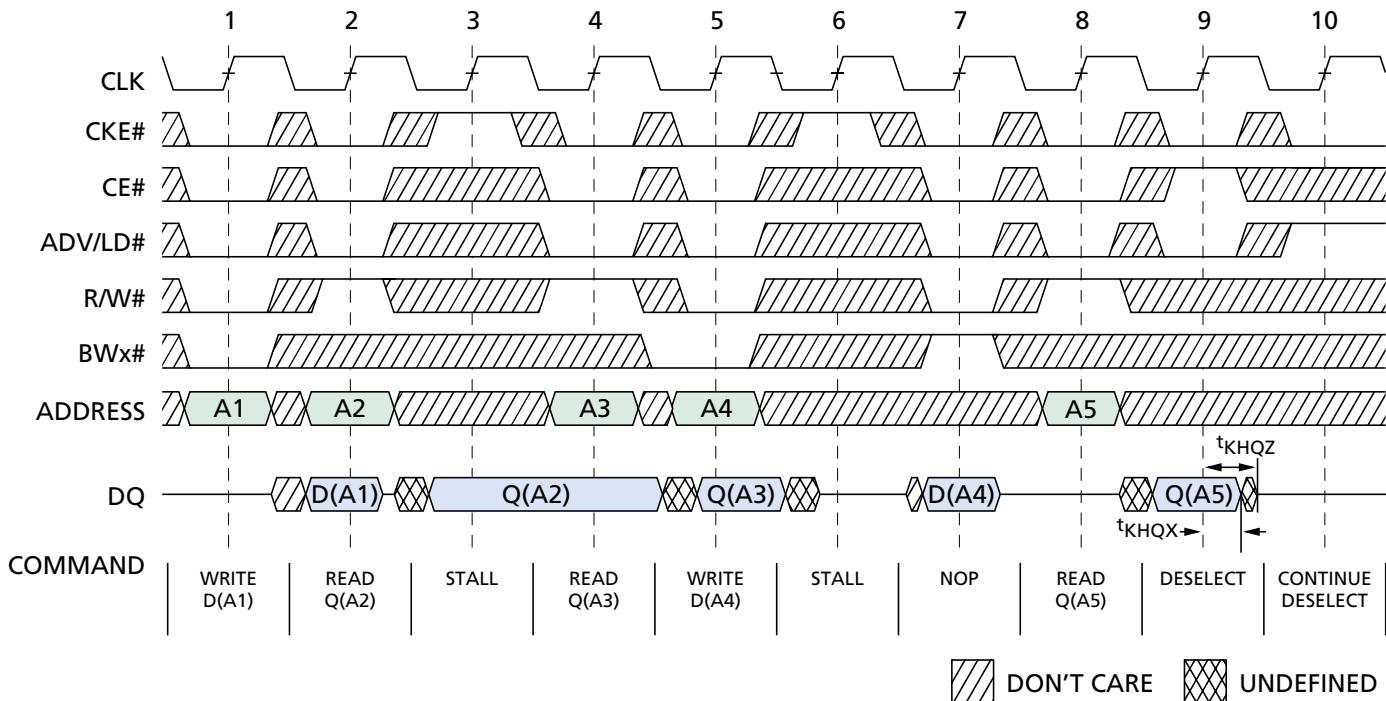
READ/WRITE TIMING

READ/WRITE TIMING PARAMETERS

| SYM | -10 | | -11 | | -12 | | UNITS |
|--------|-----|-----|-----|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| tKHKH | 10 | | 11 | | 12 | | ns |
| fKF | | 100 | | 90 | | 83 | MHz |
| tKHKL | 2.5 | | 3.0 | | 3.0 | | ns |
| tKLKH | 2.5 | | 3.0 | | 3.0 | | ns |
| tKHQV | | 7.5 | | 8.5 | | 9.0 | ns |
| tKHQX | 3.0 | | 3.0 | | 3.0 | | ns |
| tKHQX1 | 3.0 | | 3.0 | | 3.0 | | ns |
| tKHQZ | | 5.0 | | 5.0 | | 5.0 | ns |
| tGLQV | | 5.0 | | 5.0 | | 5.0 | ns |
| tGLQX | 0 | | 0 | | 0 | | ns |

| SYM | -10 | | -11 | | -12 | | UNITS | |
|-------|-----|-----|-----|-----|-----|-----|-------|----|
| | MIN | MAX | MIN | MAX | MIN | MAX | | |
| tGHOZ | | | 5.0 | | 5.0 | | 5.0 | ns |
| tAVKH | 2.0 | | 2.2 | | 2.5 | | ns | |
| tEVKH | 2.0 | | 2.2 | | 2.5 | | ns | |
| tCVKH | 2.0 | | 2.2 | | 2.5 | | ns | |
| tDVKH | 2.0 | | 2.2 | | 2.5 | | ns | |
| tKHAX | 0.5 | | 0.5 | | 0.5 | | ns | |
| tKHEX | 0.5 | | 0.5 | | 0.5 | | ns | |
| tKHGX | 0.5 | | 0.5 | | 0.5 | | ns | |
| tKHDX | 0.5 | | 0.5 | | 0.5 | | ns | |

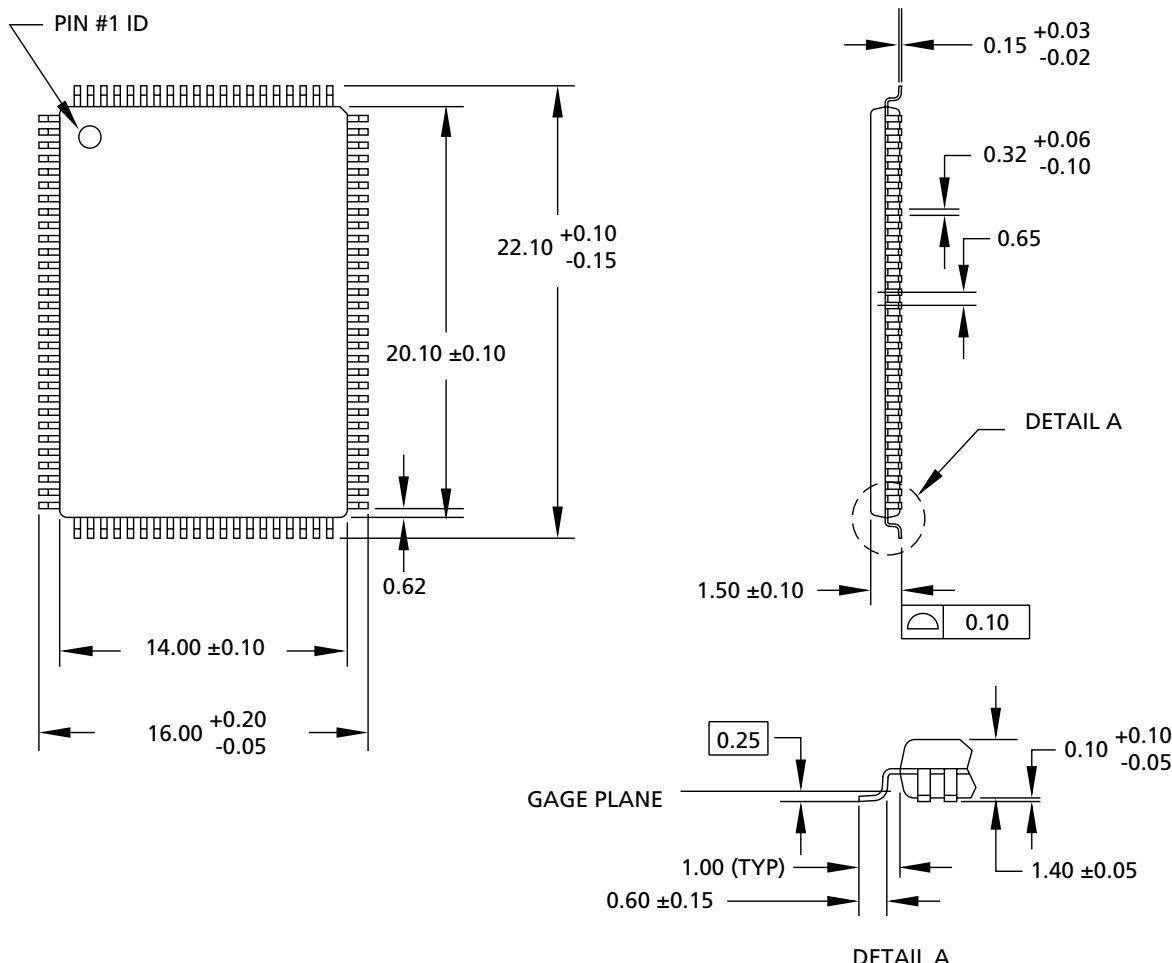
NOTE:

1. For this waveform, ZZ is tied LOW.
2. Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BURST operations are optional.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

NOP, STALL, AND DESELECT CYCLES

NOP, STALL, AND DESELECT TIMING PARAMETERS

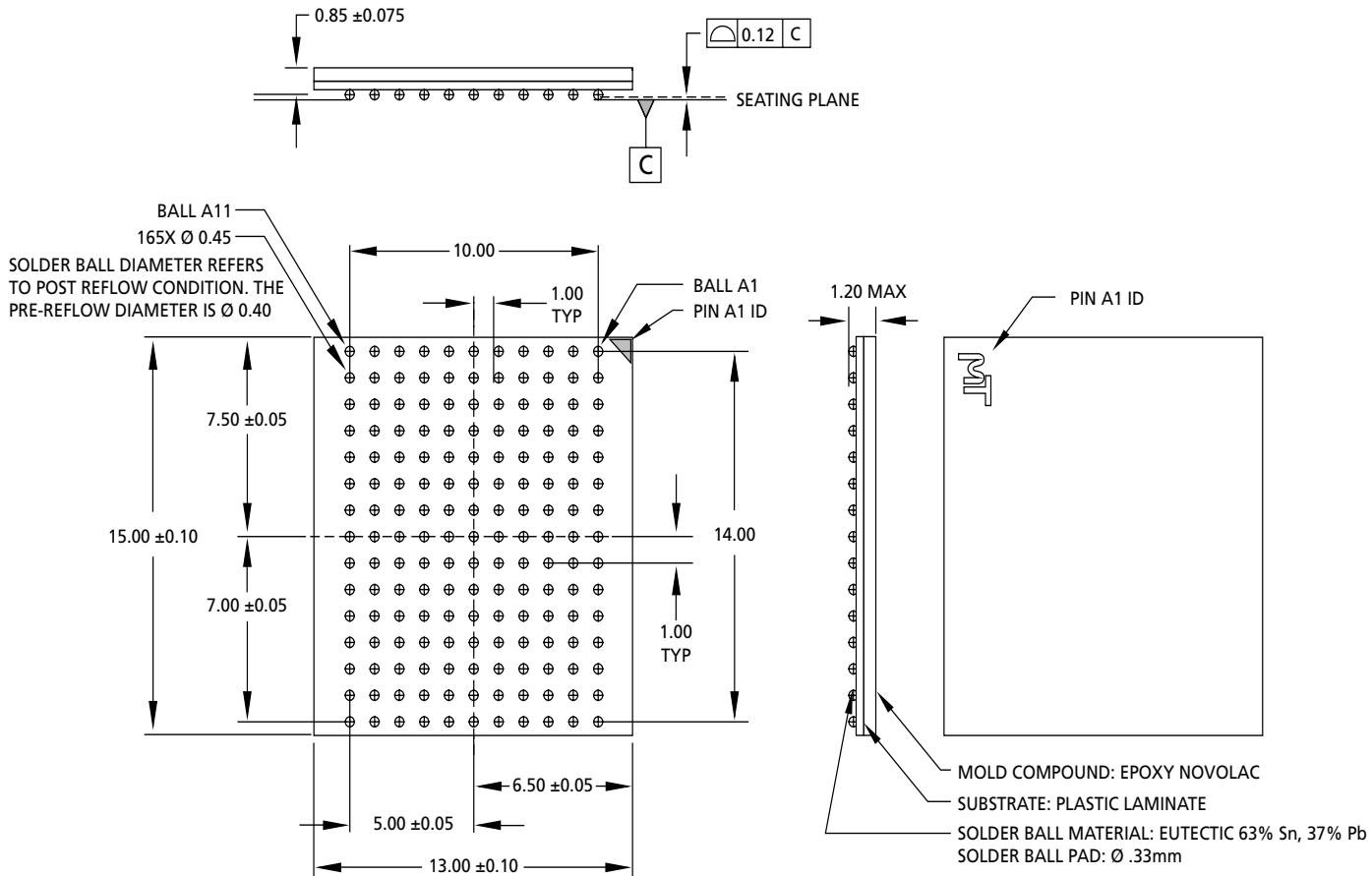
| SYM | -10 | | -11 | | -12 | | UNITS |
|------------|-----|-----|-----|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{KHQX} | 3.0 | | 3.0 | | 3.0 | | ns |
| t_{KHQZ} | | 5.0 | | 5.0 | | 5.0 | ns |

NOTE: 1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates CKE# being used to create a "pause." A WRITE is not performed during this cycle.
 2. For this waveform, ZZ and OE# are tied LOW.
 3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
 4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

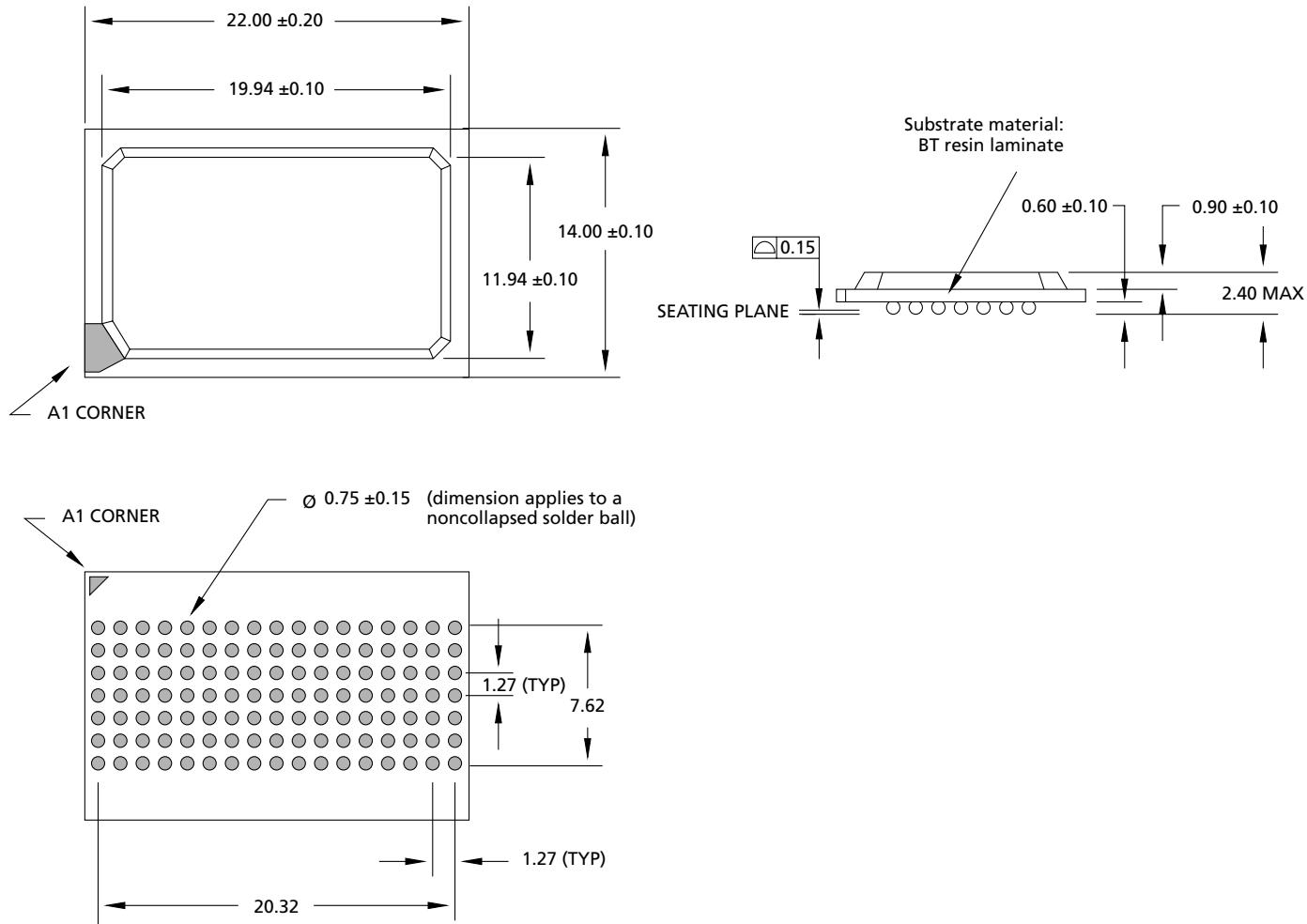
100-PIN PLASTIC TQFP (JEDEC LQFP)


NOTE:

1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

165-PIN FBGA


NOTE: 1. All dimensions in millimeters **MAX** or typical where noted.
MIN

119-PIN BGA


NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Solder ball pad is 0.6mm.



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REVISION HISTORY

Removed note "Not Recommended for New Designs," Rev. 6/01 June 7/01

Added industrial temperature references and notes, Rev. 3/01 March 19/01
Changed 16Mb references to 18Mb
Changed NC/DQPx to NF/DQPx

Added 119-pin PBGA package, Rev. 1/01, FINAL January 10/01

Removed FBGA Part Marking Guide, Rev. 8/00, FINAL August 1/00

Added FBGA Part Marking Guide, Rev 7/00 7/21/00
Added Revision History
Removed 119-Pin PBGA packages and references

Added 165-pin FBGA Package 6/13/00