Specification

BTHQ 96040AV2-FSTF-12-12C-COG

Doc. No. COG-BT96040A-08

Version July 2008

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2008.07.30	First Release. Based on a.) Test Specification: VL-TS-COG-BT96040A-XX REV.C 2008.07.07 b.) VL-QUA-012B REV.X 2008.02.18 According to VL-QUA-012B, for positive mode, LCD size is small because Unit Per Laminate=28 which is more than 6pcs/Laminate.	LINDA ZHU	TAN XIAO DI

CONTENTS

Specification
of
LCD Module Type
Item No.: COG-BT96040A-08

1. General Description

- 96 x 40 dots FSTN B&W Positive Transflective Dot Matrix LCD module.
- Viewing angle: 12 O'clock.
- Driving scheme: 1/68 duty, 1/9 bias.
- Driving IC: 'SITRONIX' ST7549Ti (COG) LCD controller/driver or equivalent.
- Logic voltage: 3V.
- "RoHS" compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	46.0(W) x 36.2(H) x 1.98(D) (Excluded pins and EPOXY)	mm
Viewing area	40.00(W) x 23.00(H)	mm
Active area	35.217(W) x 18.225(H)	mm
Display format	96 x 40	dots
Dot size	0.352(W) x 0.441(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.367 (W) x 0.456(H)	mm
Weight:	Approx: 6.5	gram

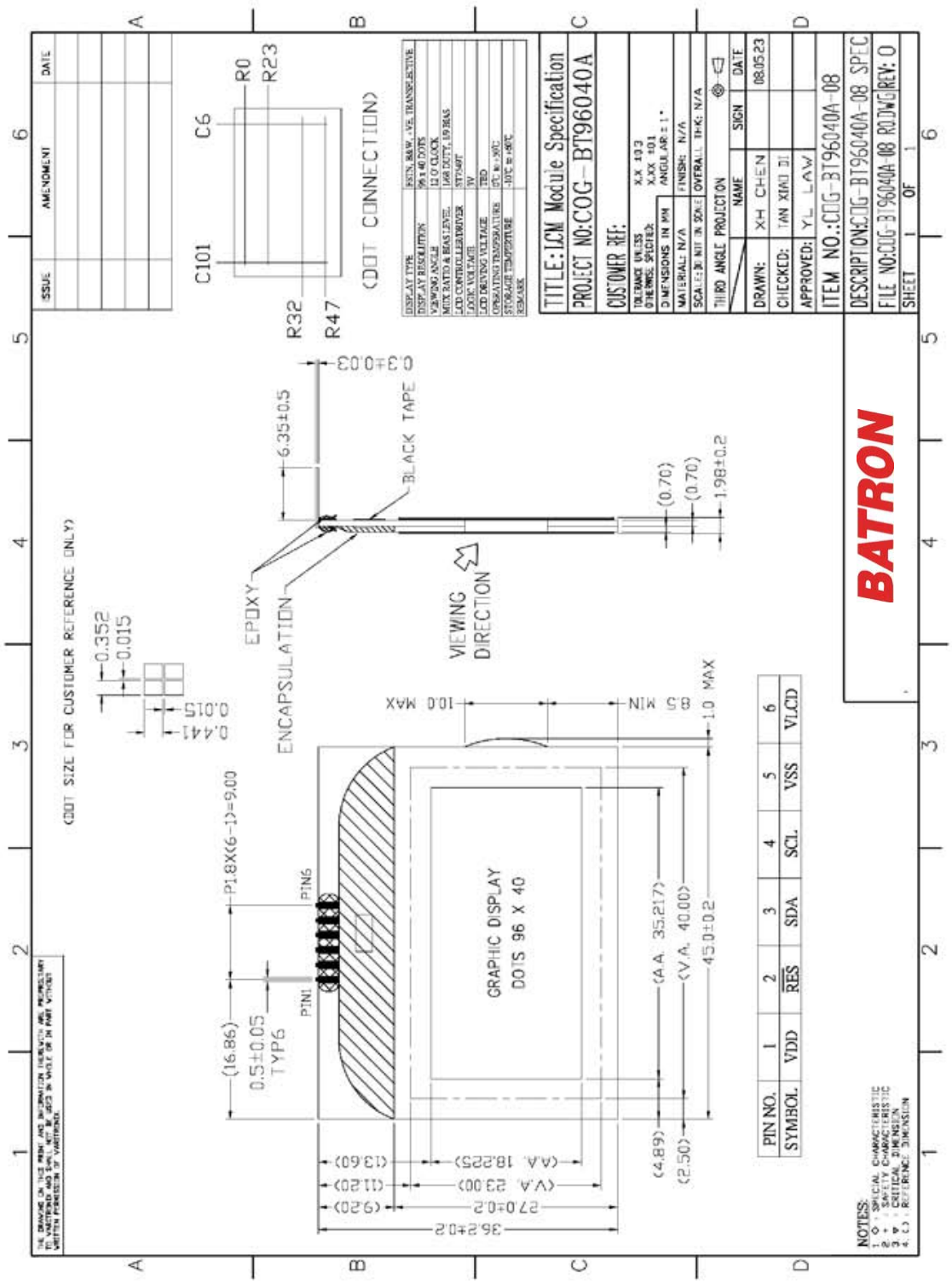


Figure 1: Module Specification

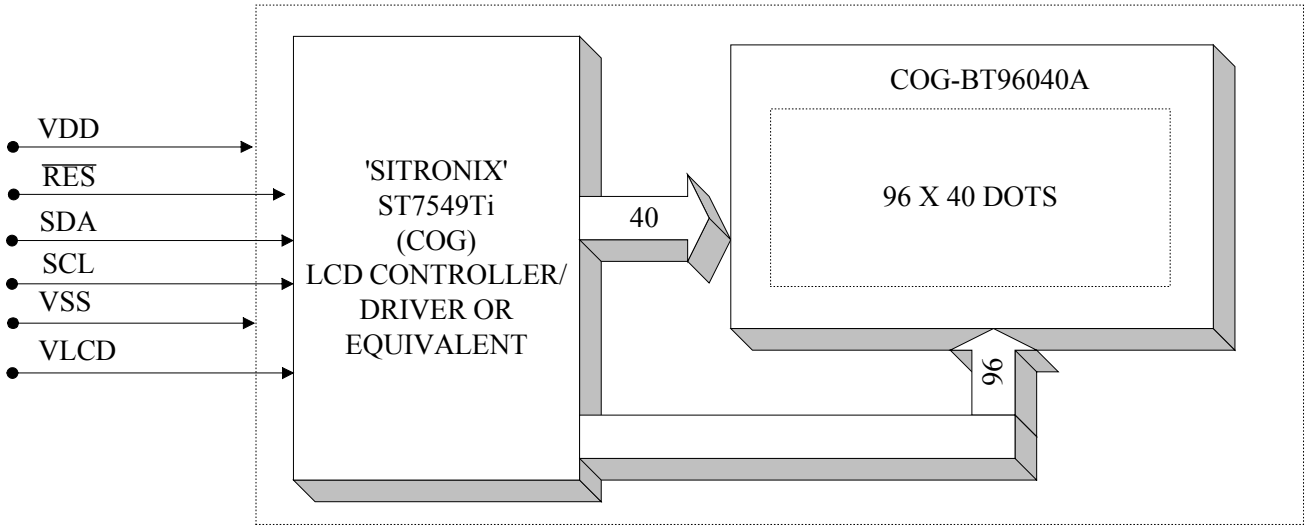


Figure 2: Block Diagram

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VDD	Power supply for logic (+3V).
2	$\overline{RES}$	Reset Input Pin. When $\overline{RES}$ is " L ", initialization is executed.
3	SDA	Serial input data.
4	SCL	Serial clock input.
5	VSS	Ground (0V).
6	VLCD	Power supply for LCD driver.

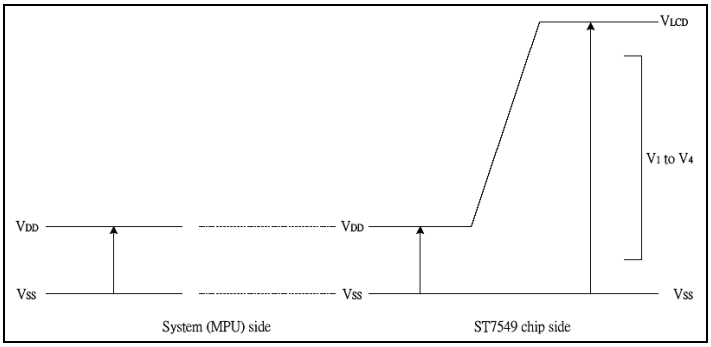
4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings-For IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage(VDD1)	VDD1	-0.5	5	V
Power supply voltage(VDD2)	VDD2	-0.5	5	V
Power supply voltage(VLCDIN) (VDD standard)	VLCDIN	4.5	13	V
Power supply voltage(V1,V2,V3,V4) (VDD standard)	V1,V2,V3,V4	0.3	VLCDIN	V
Input voltage	CSB,RESB,A0, /WR,/RD,D7~D0	-0.5	5	V

Note: The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltages are with respect to VSS unless otherwise noted.
Insure that the voltage levels of V1, V2, V3, and V4 are always such that
VLCDIN≥V0≥V1≥V2≥V3≥V4≥VSS.



4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C <50%RH for 40°C <Ta≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD =VDD1=VDD2= +3.0V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		2.85	3.0	3.1 5	V
High-level Input Voltage	V_{IHC}		0.7 VDD	-	VDD	V
Low-level Input Voltage	V_{ILC}		VSS	-	0.3 VDD	V
Supply Current (Logic & LCD)	IDD	Character mode, VDD = 3V, Note 1	-	0.6	0.9	mA
		Checker board mode, VDD = 3V, Note 1	-	0.7	1.1	mA

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note 2: VLCD can not be tested.

5.2 Timing Specifications

Reset Timing

Ta = 0 °C to +50 °C, VDD = 3.3V, VSS=0V;

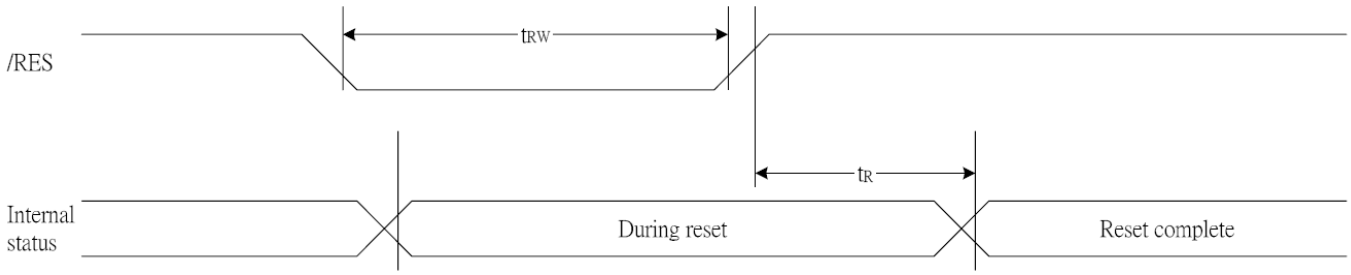
Table 6 (a)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1	—	—	us

Ta = 0 °C to +50 °C, VDD = 2.8V, VSS=0V;

Table 6 (b)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us



I²C BUS INTERFACE

Ta = 0 °C to + 50 °C, VDD = 3.3V, VSS=0V;

Table 7

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP condition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and START condition	SCL	TBUF		1.3		us

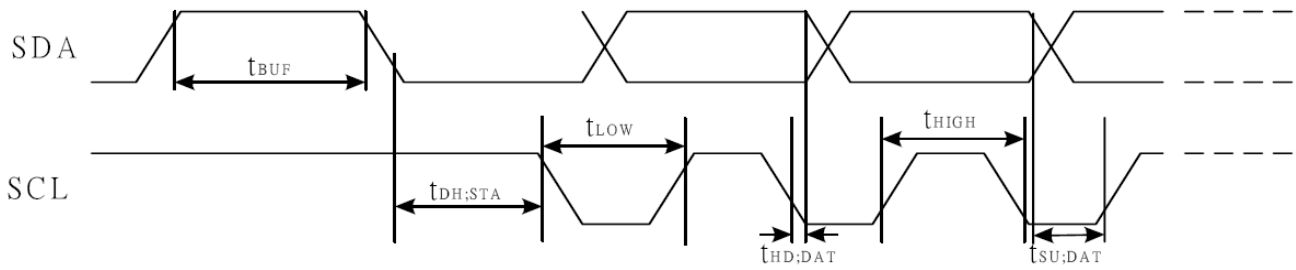


Figure 4: I²C bus timing diagram

5.3 Command Description

Referential instruction setup flow: Initializing with the built-in power supply circuits.

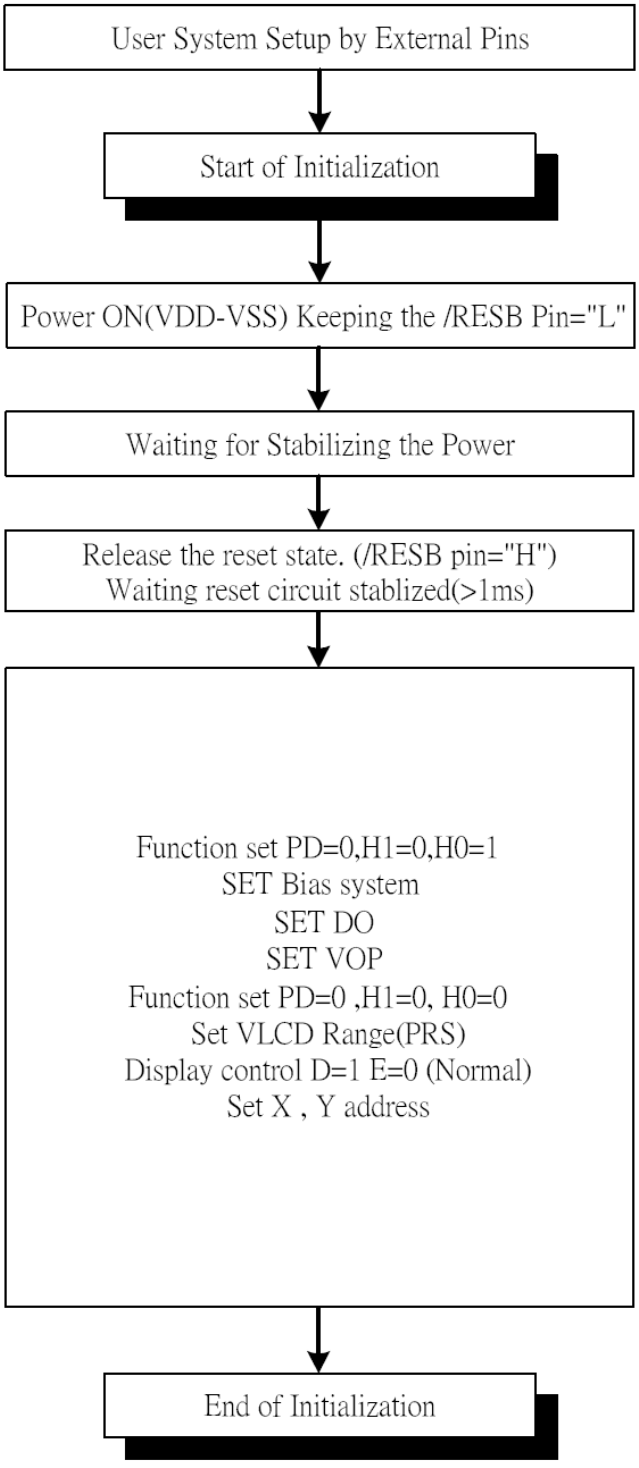


Figure 5: Initializing with the built-in Power Supply Circuits

6. LCD Specifications

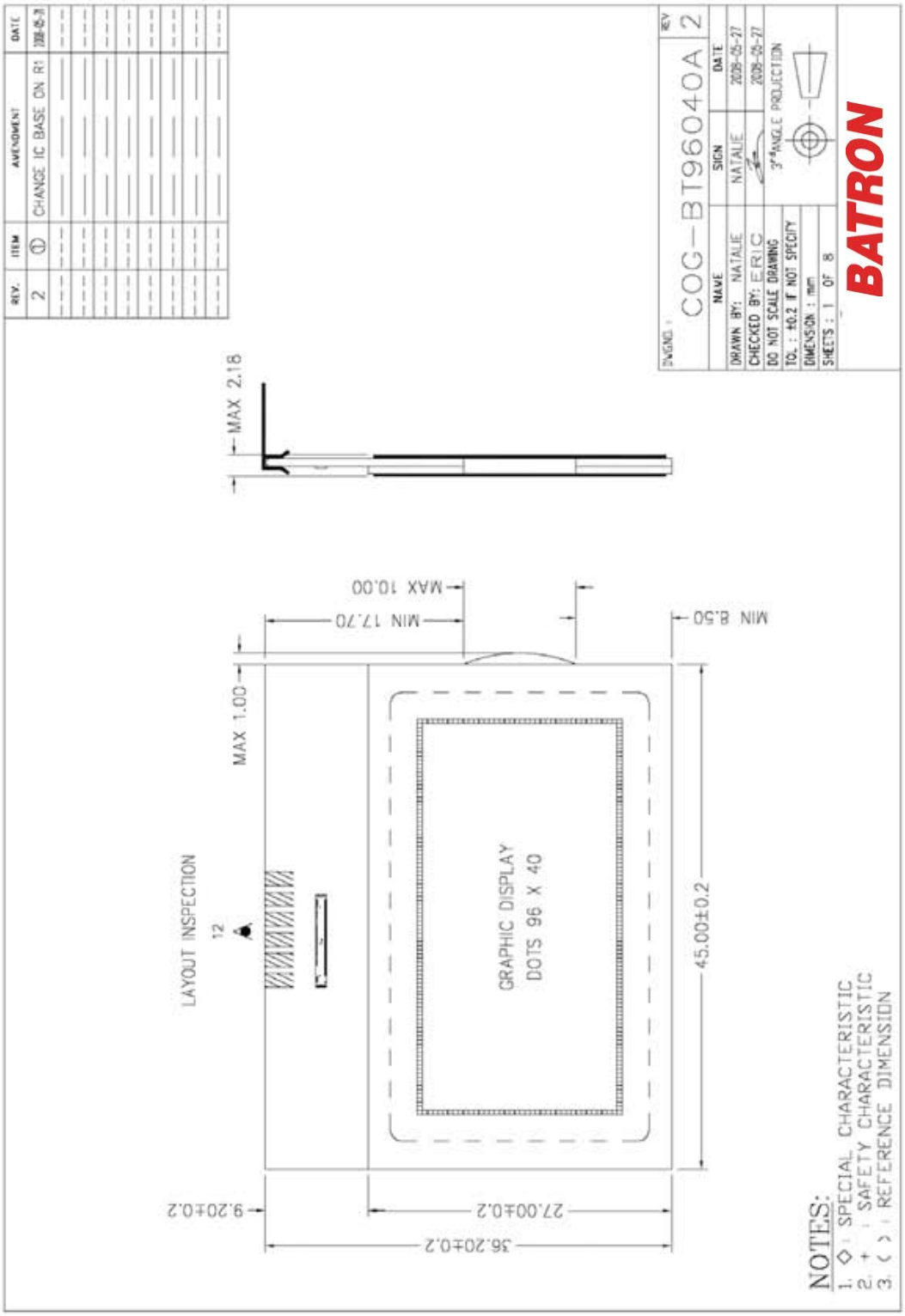


Figure 6: LCD drawing 1

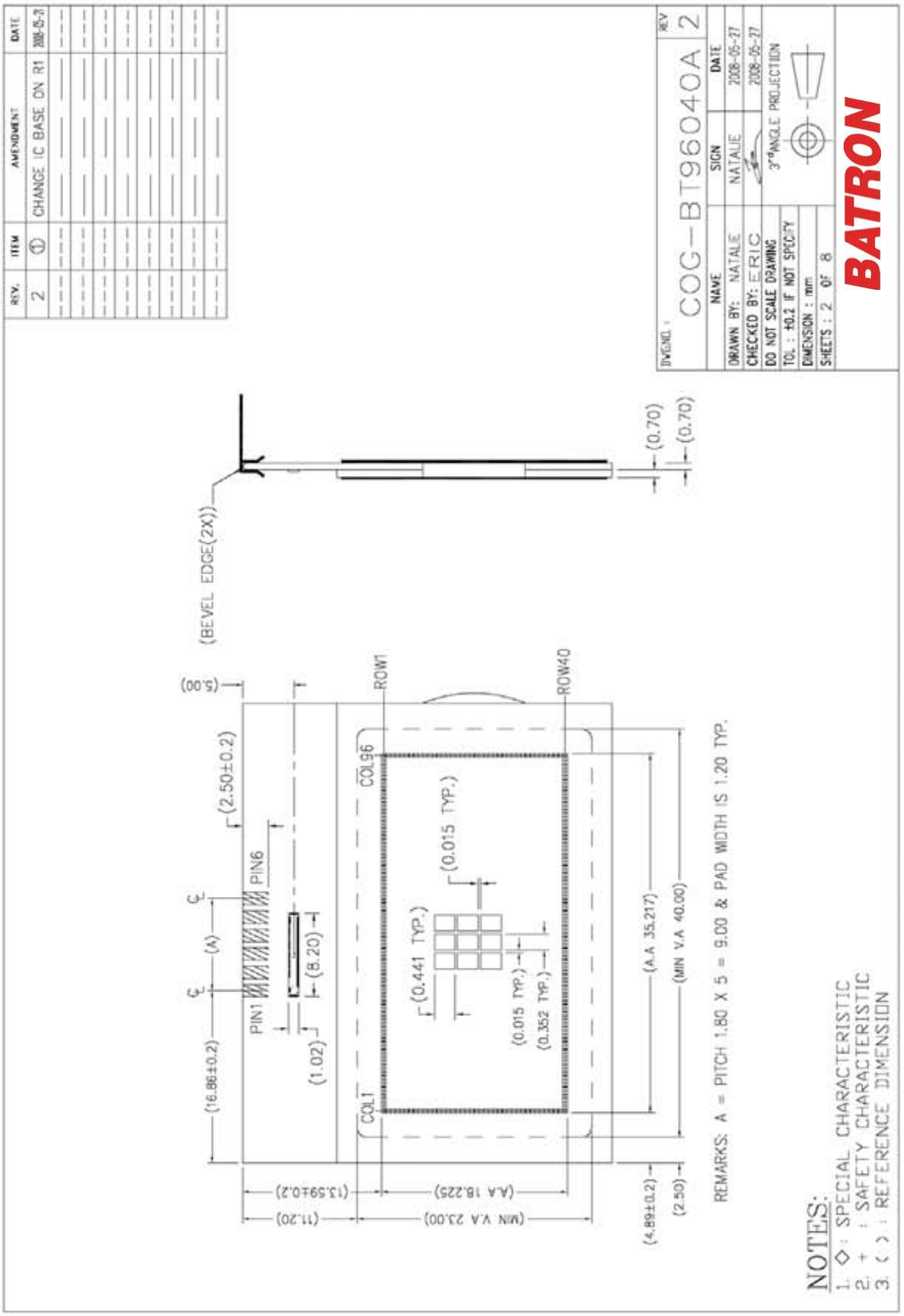


Figure 7: LCD drawing 2

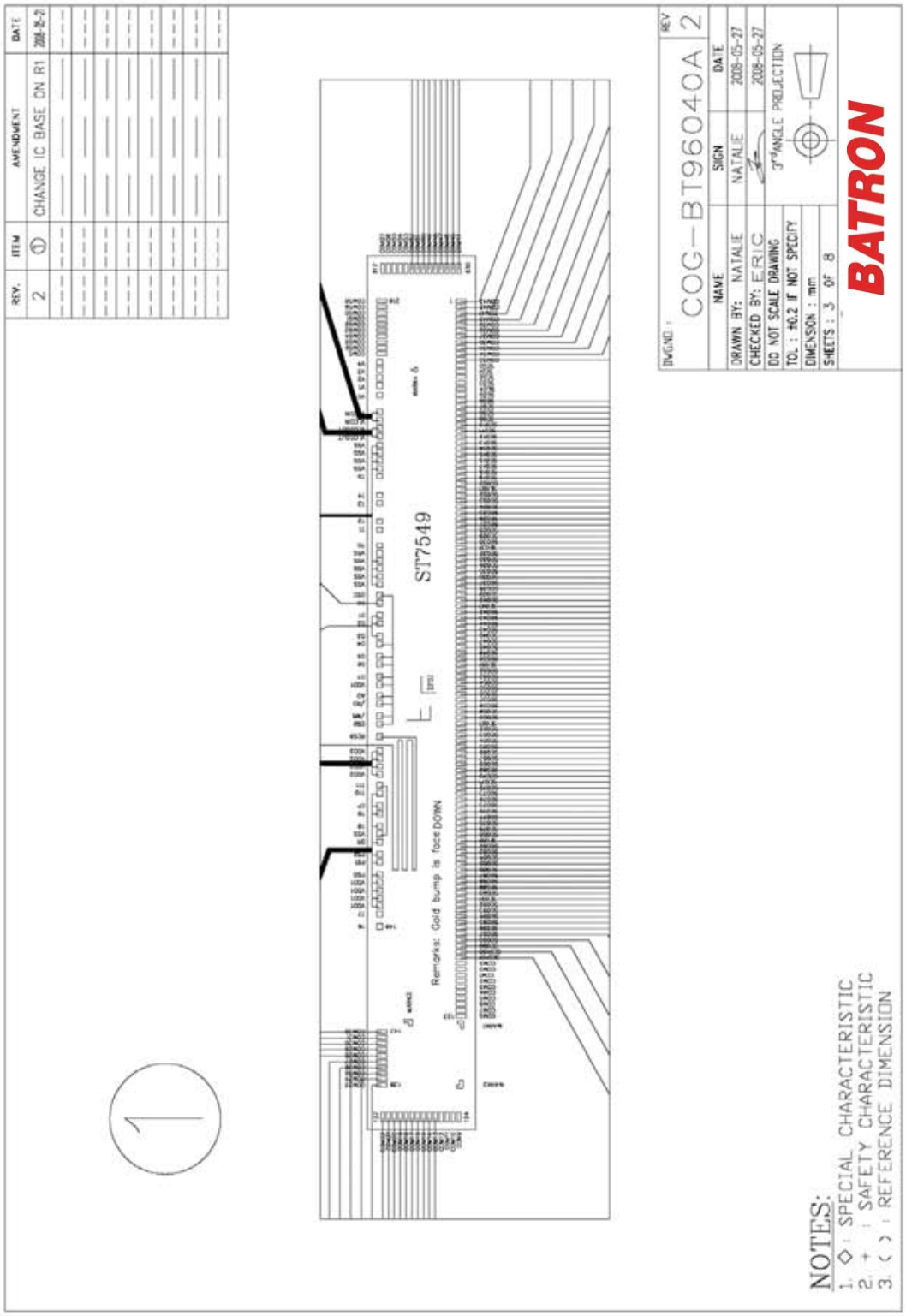


Figure 8: LCD drawing 3

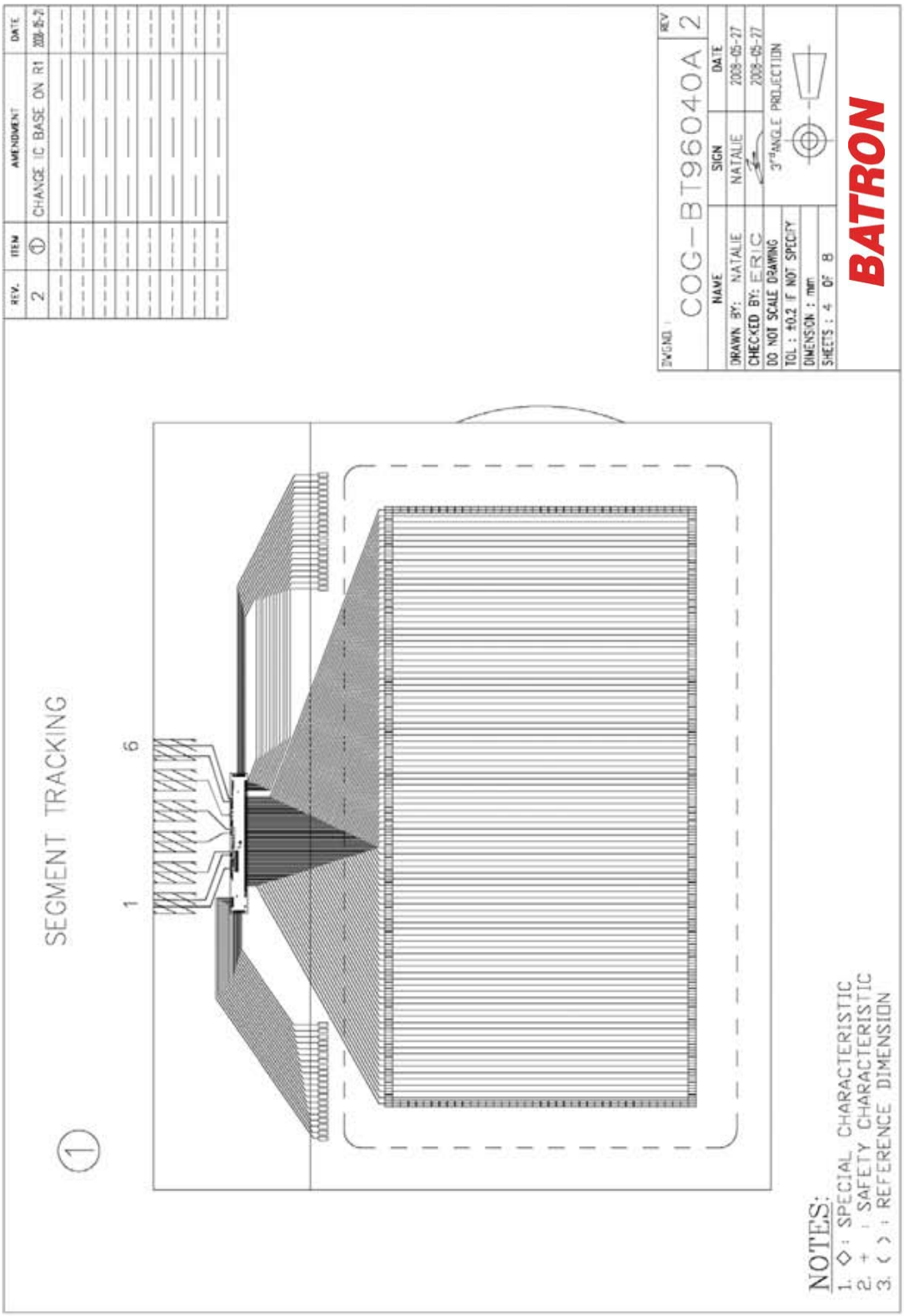


Figure 9: LCD drawing 4

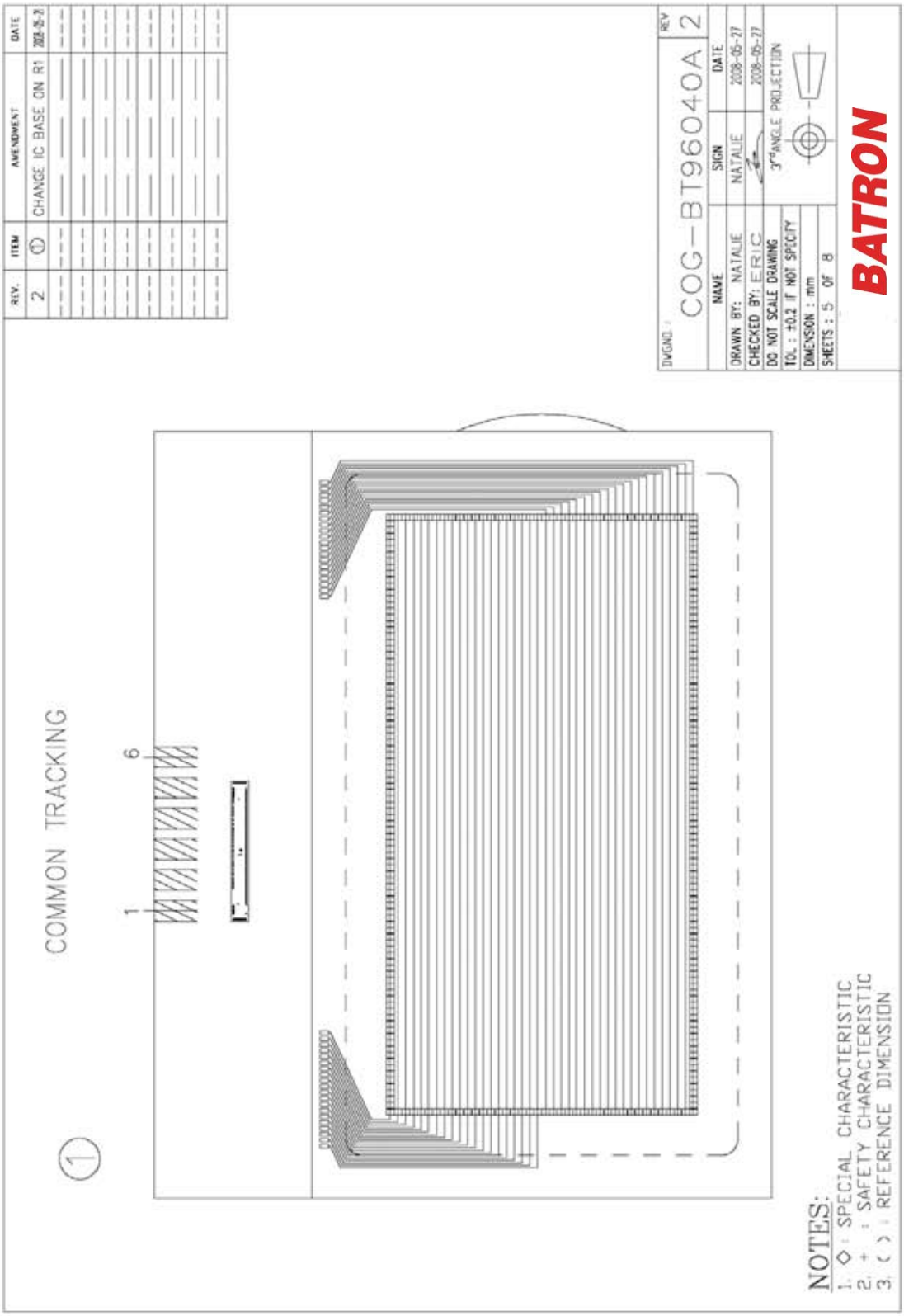


Figure 10: LCD drawing 5

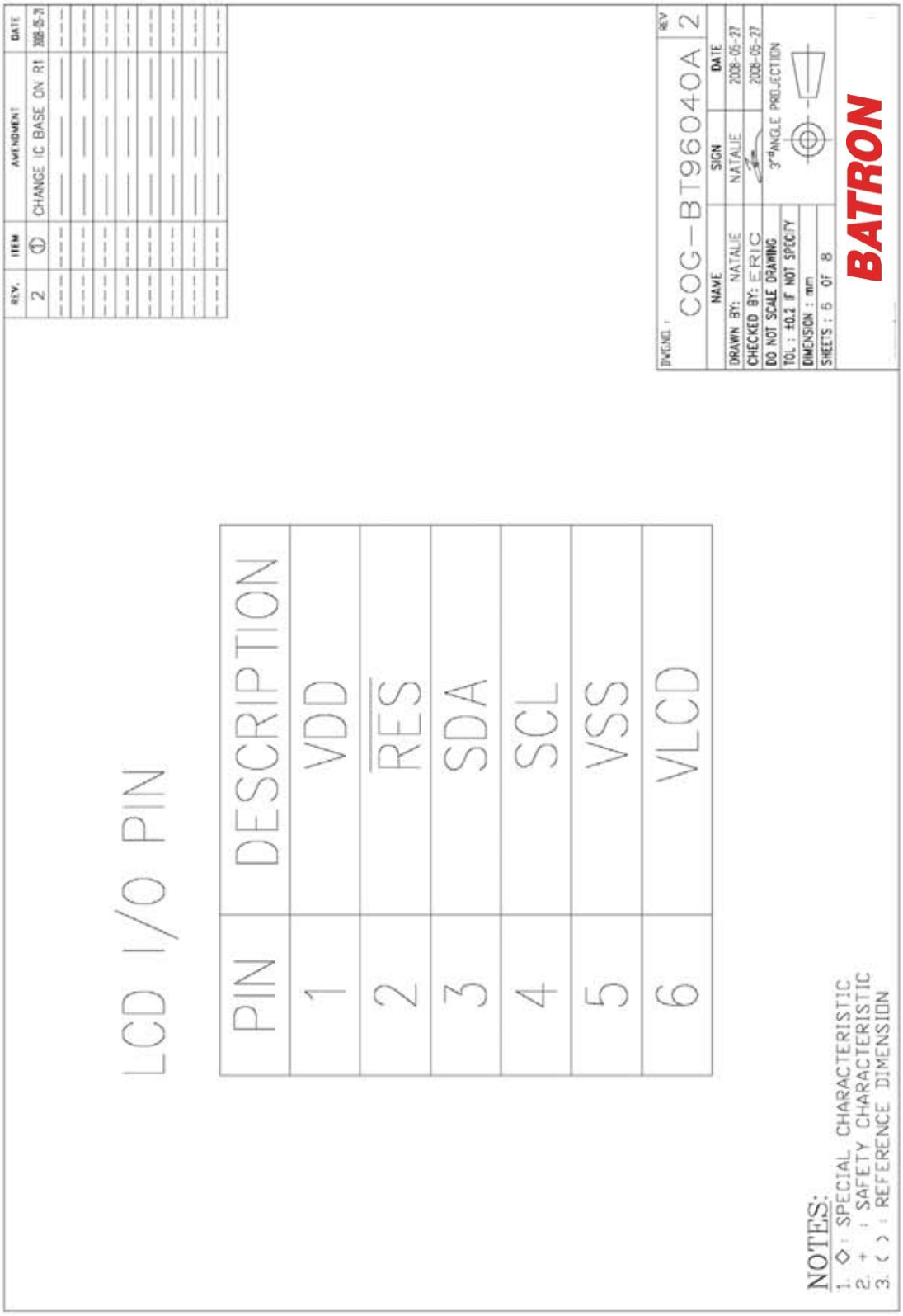


Figure 11: LCD drawing 6

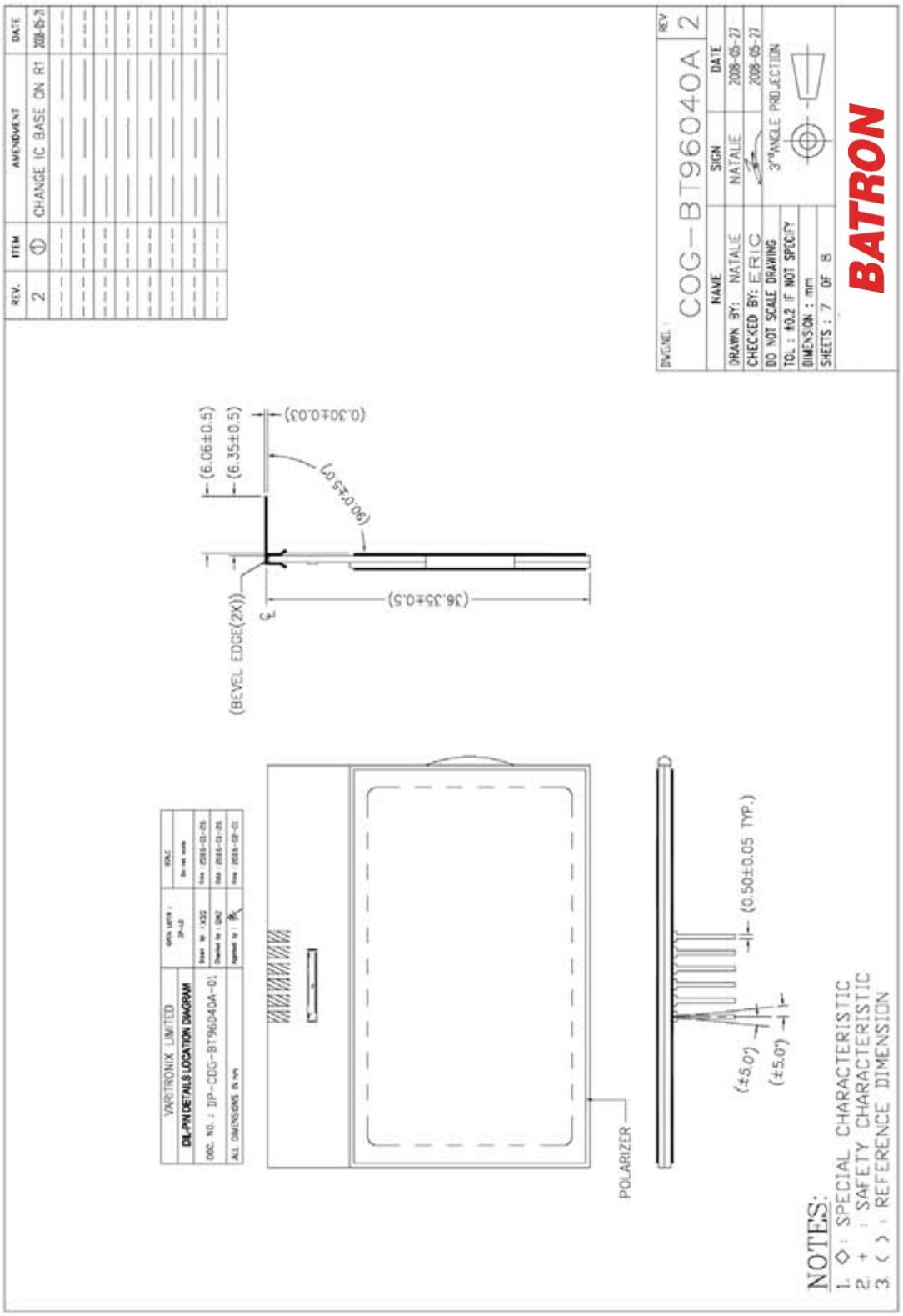


Figure 12: LCD drawing 7

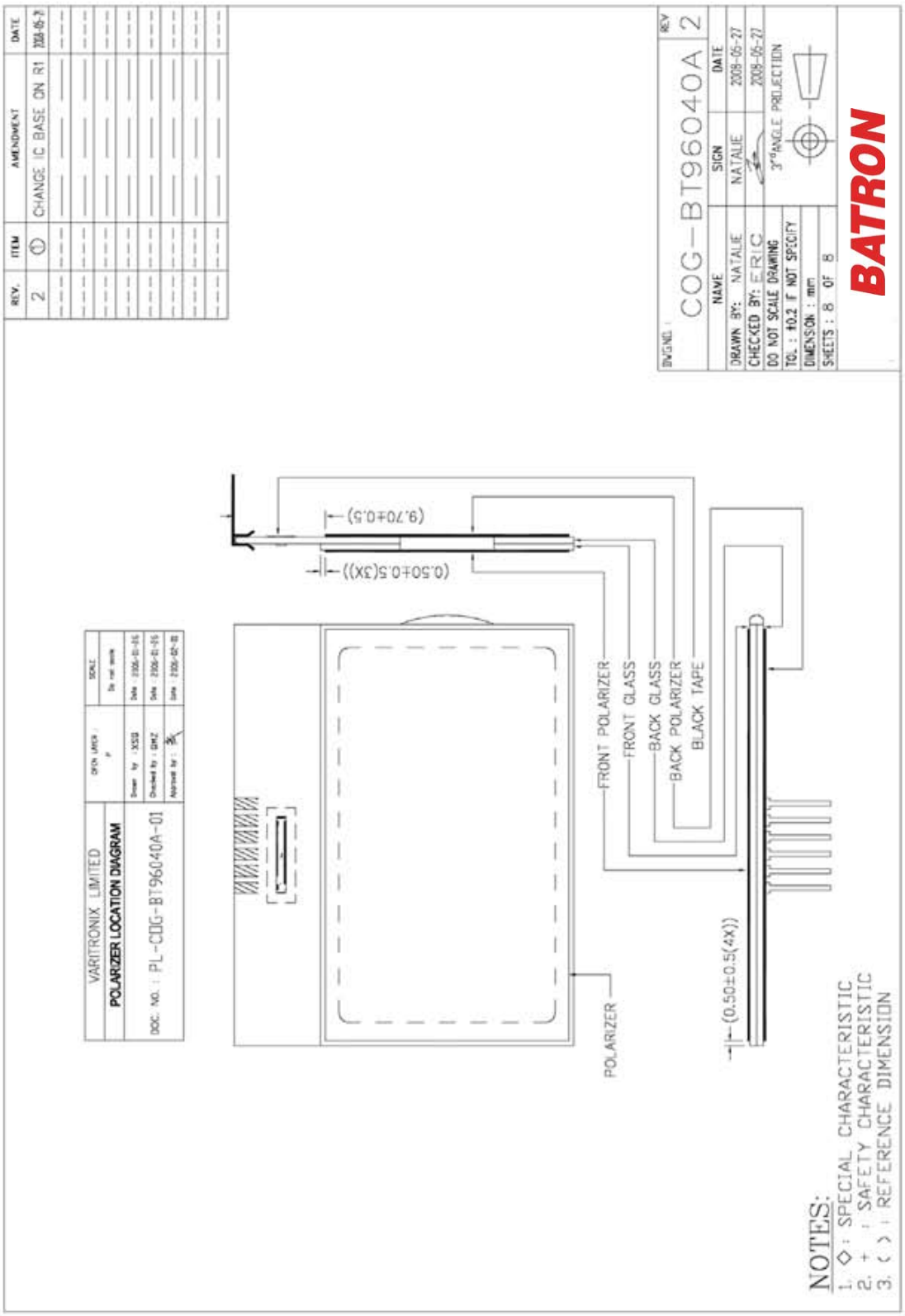


Figure 13: LCD drawing 8

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