

## FEATURES

- Real-time clock (RTC) counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap-year compensation valid up to 2100
- 96-byte, battery-backed, nonvolatile (NV) RAM for data storage
- Two time-of-day alarms—programmable on combination of seconds, minutes, hours, and day of the week
- 1Hz and 32.768kHz clock outputs
- Serial interface supports Motorola Serial Peripheral Interface (SPI) serial data ports or standard 3-wire interface
- Burst mode for reading/writing successive addresses in clock/RAM
- Dual-power supply pins for primary and backup power supplies
- Optional trickle charge output to backup supply
- 2.0V to 5.5V operation
- Optional industrial temperature range: -40°C to +85°C
- Available in space-efficient, 20-pin TSSOP package
- Underwriters Laboratory (UL) recognized

## ORDERING INFORMATION

DS1306	16-Pin DIP (300-mil)
DS1306N	16-Pin DIP (Industrial)
DS1306E	20-Pin TSSOP (4.4mm)
DS1306EN	20-Pin TSSOP (Industrial)

# DS1306

## Serial Alarm Real-Time Clock

## PIN ASSIGNMENT

V <sub>CC2</sub>	1	20	V <sub>CC1</sub>
V <sub>BAT</sub>	2	19	NC
X1	3	18	32kHz
NC	4	17	V <sub>CCIF</sub>
X2	5	16	SDO
<u>NC</u>	6	15	SDI
INT0	7	14	SCLK
INT1	8	13	NC
1Hz	9	12	CE
GND	10	11	SERMODE

DS1306 20-Pin TSSOP (4.4mm)

V <sub>CC2</sub>	1	16	V <sub>CC1</sub>
V <sub>BAT</sub>	2	15	32kHz
X1	3	14	V <sub>CCIF</sub>
X2	4	13	SDO
INT0	5	12	SDI
INT1	6	11	SCLK
1Hz	7	10	CE
GND	8	9	SERMODE

DS1306 16-Pin DIP (300-mil)

Package Dimension Information can be found at:  
[www.maxim-ic.com/TechSupport/PackInfo.html](http://www.maxim-ic.com/TechSupport/PackInfo.html)

## PIN DESCRIPTION

V <sub>CC1</sub>	- Primary Power Supply
V <sub>CC2</sub>	- Backup Power Supply
V <sub>BAT</sub>	- +3V Battery Input
V <sub>CCIF</sub>	- Interface Logic Power Supply Input
GND	- Ground
X1, X2	- 32.768kHz Crystal Connection
<u>INT0</u>	- Interrupt 0 Output
INT1	- Interrupt 1 Output
SDI	- Serial Data In
SDO	- Serial Data Out
CE	- Chip Enable
SCLK	- Serial Clock
SERMODE	- Serial Interface Mode
1Hz	- 1Hz Output
32kHz	- 32.768kHz Output

## DESCRIPTION

The DS1306 Serial Alarm Real-Time Clock (RTC) provides a full binary-coded decimal (BCD) clock calendar that is accessed via a simple serial interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. In addition, 96 bytes of NV RAM are provided for data storage.

An interface logic-power supply input pin (V<sub>CCIF</sub>) allows the DS1306 to drive SDO and 32kHz pins to a level that is compatible with the interface logic. This allows an easy interface to 3V logic in mixed supply systems. The DS1306 offers dual-power supplies as well as a battery-input pin. The dual-power supplies support a programmable trickle charge circuit that allows a rechargeable energy source (such as a super cap or rechargeable battery) to be used for a backup supply. The V<sub>BAT</sub> pin allows the device to be backed up by a non-rechargeable battery. The DS1306 is fully operational from 2.0V to 5.5V.

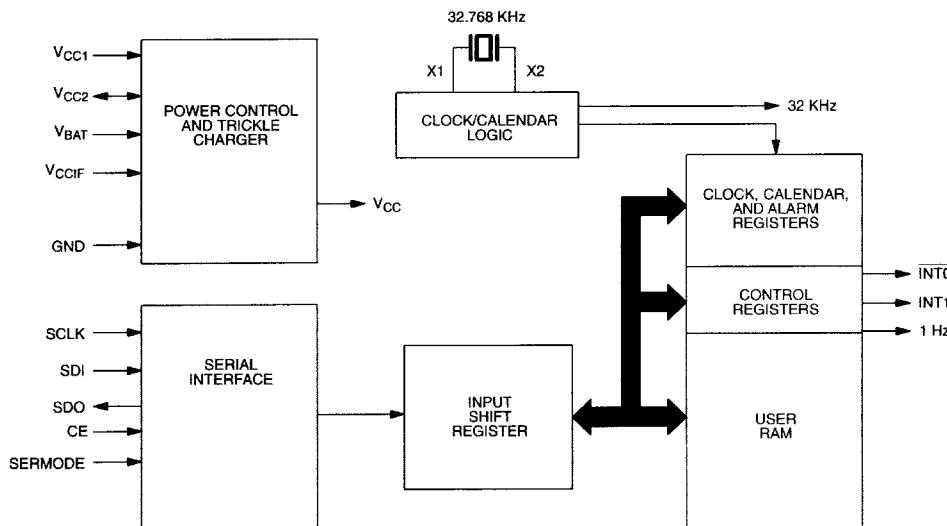
Two programmable time-of-day alarms are provided by the DS1306. Each alarm can generate an interrupt on a programmable combination of seconds, minutes, hours, and day. “Don’t care” states can be inserted into one or more fields if it is desired for them to be ignored for the alarm condition. A 1Hz and a 32kHz clock output are also available.

The DS1306 supports a direct interface to Motorola SPI serial data ports or standard 3-wire interface. An easy-to-use address and data format is implemented in which data transfers can occur 1 byte at a time or in multiple-byte burst mode.

## OPERATION

The block diagram in Figure 1 shows the main elements of the serial alarm RTC. The following paragraphs describe the function of each pin.

### DS1306 BLOCK DIAGRAM Figure 1



## SIGNAL DESCRIPTIONS

**V<sub>CC1</sub>** – DC power is provided to the device on this pin. V<sub>CC1</sub> is the primary power supply.

**V<sub>CC2</sub>** – This is the secondary power supply pin. In systems using the trickle charger, the rechargeable energy source is connected to this pin.

**V<sub>BAT</sub>** – Battery input for any standard 3V lithium cell or other energy source. UL recognized to ensure against reverse charging current when used in conjunction with a lithium battery. See “Conditions of Acceptability” at <http://www.maxim-ic.com/TechSupport/QA/ntr1.htm>.

**V<sub>CCIF</sub> (Interface Logic Power Supply Input)** – The V<sub>CCIF</sub> pin allows the DS1306 to drive SDO and 32kHz output pins to a level that is compatible with the interface logic, thus allowing an easy interface to 3V logic in mixed supply systems. This pin is physically connected to the source connection of the p-channel transistors in the output buffers of the SDO and 32kHz pins.

**SERMODE (Serial Interface Mode Input)** – The SERMODE pin offers the flexibility to choose between two serial interface modes. When connected to GND, standard 3-wire communication is selected. When connected to V<sub>CC</sub>, Motorola SPI communication is selected.

**SCLK (Serial Clock Input)** – SCLK is used to synchronize data movement on the serial interface for either the SPI or 3-wire interface.

**SDI (Serial Data Input)** – When SPI communication is selected, the SDI pin is the serial data input for the SPI bus. When 3-wire communication is selected, this pin must be tied to the SDO pin (the SDI and SDO pins function as a single I/O pin when tied together).

**SDO (Serial Data Output)** – When SPI communication is selected, the SDO pin is the serial data output for the SPI bus. When 3-wire communication is selected, this pin must be tied to the SDI pin (the SDI and SDO pins function as a single I/O pin when tied together). V<sub>CCIF</sub> provides the logic high level.

**CE (Chip Enable)** – The chip enable signal must be asserted high during a read or a write for both 3-wire and SPI communication. This pin has an internal 55k pull-down resistor (typical).

**INT0 (Interrupt 0 Output)** – The INT0 pin is an active low output of the DS1306 that can be used as an interrupt input to a processor. The INT0 pin can be programmed to be asserted by alarm 0. The INT0 pin remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. The INT0 pin operates when the DS1306 is powered by V<sub>CC1</sub>, V<sub>CC2</sub>, or V<sub>BAT</sub>. The INT0 pin is an open drain output and requires an external pull-up resistor.

**1Hz (1Hz Clock Output)** – The 1Hz pin provides a 1Hz square wave output. This output is active when the 1 Hz bit in the control register is a logic 1.

Both INT0 and 1Hz pins are open drain outputs. The interrupt, 1Hz signal, and the internal clock continue to run regardless of the level of V<sub>CC</sub> (as long as a power source is present).

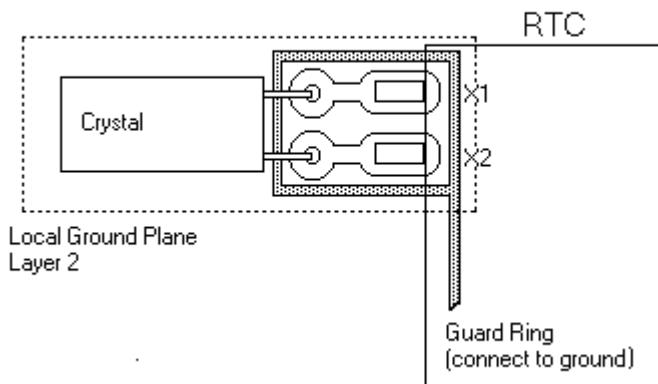
**INT1 (Interrupt 1 Output)** – The INT1 pin is an active high output of the DS1306 that can be used as an interrupt input to a processor. The INT1 pin can be programmed to be asserted by alarm 1. When an alarm condition is present, the INT1 pin generates a 62.5ms active high pulse. The INT1 pin operates

only when the DS1306 is powered by  $V_{CC2}$  or  $V_{BAT}$ . When active, the INT1 pin is internally pulled up to  $V_{CC2}$  or  $V_{BAT}$ . When inactive, the INT1 pin is internally pulled low.

**32kHz (32.768kHz Clock Output)** – The 32kHz pin provides a 32.768kHz output. This signal is always present.  $V_{CCIF}$  provides the logic high level.

**X1, X2** – Connections for a standard 32.768kHz quartz crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real-Time Clocks.” The DS1306 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

## RECOMMENDED LAYOUT FOR CRYSTAL



## CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. See Application Note 58, “Crystal Considerations with Dallas Real-Time Clocks” for detailed information.

## CLOCK, CALENDAR, AND ALARM

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Figure 2. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. Note that some bits are set to 0. These bits will always read 0 regardless of how they are written. Also note that registers 12h to 1Fh (read) and registers 92h to 9Fh are reserved. These registers will always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the BCD format.

## RTC REGISTERS AND ADDRESS MAP Figure 2

HEX ADDRESS READ WRITE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RANGE				
00H	80H	0	10 SEC			SEC			00-59				
01H	81H	0	10 MIN			MIN			00-59				
02H	82H	0	12	P	10 HR	HOURS			01-12 + P/A				
			A						00-23				
			24	10									
03H	83H	0	0	0	0	0	DAY		01-07				
04H	84H	0	0	10 DATE		DATE			1-31				
05H	85H	0	0	10 MONTH		MONTH			01-12				
06H	86H	10 YEAR				YEAR			00-99				
07H	87H	M	10 SEC ALARM 0			SEC ALARM 0			00-59				
08H	88H	M	10 MIN ALARM 0			MIN ALARM 0			00-59				
09H	89H	M	12	P	10 HR	HOUR ALARM 0			01-12 + P/A				
			A						00-23				
			24	10									
0AH	8AH	M	0	0	0	0	DAY ALARM 0		01-07				
0BH	8BH	M	10 SEC ALARM 1			SEC ALARM 1			00-59				
0CH	8CH	M	10 MIN ALARM 1			MIN ALARM 1			00-59				
0DH	8DH	M	12	P	10 HR	HOUR ALARM 1			01-12 + P/A				
			A						00-23				
			24	10									
0EH	8EH	M	0	0	0	0	DAY ALARM 1		01-07				
<hr/>													
0FH	8FH	CONTROL REGISTER											
10H	90H	STATUS REGISTER											
11H	91H	TRICKLE CHARGER REGISTER											
12-1FH	92-9FH	RESERVED											
20-7FH	A0-FFH	96-BYTES USER RAM											

**NOTE:**

1. Range for alarm registers does not include mask'm' bits.

The DS1306 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours).

The DS1306 contains two time-of-day alarms. Time-of-day alarm 0 can be set by writing to registers 87h to 8Ah. Time-of-day alarm 1 can be set by writing to registers 8 Bh to 8 Eh. Bit 7 of each of the time-of-day alarm registers are mask bits (Table 1). When all of the mask bits are logic 0, a time-of-day alarm will only occur once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time-of-day alarm registers. An alarm will be generated every day when bit 7 of the day alarm register is set to a logic 1. An alarm will be generated every hour when bit 7 of the day and hour alarm registers is set to a logic 1. Similarly, an alarm will be generated every minute when bit 7 of the day, hour, and minute alarm registers is set to a logic 1. When bit 7 of the day, hour, minute, and seconds alarm registers is set to a logic 1, an alarm will occur every second.

## TIME-OF-DAY ALARM MASK BITS Table 1

ALARM REGISTER MASK BITS (BIT 7)				
SECONDS	MINUTES	HOURS	DAYS	
1	1	1	1	Alarm once per second
0	1	1	1	Alarm when seconds match
0	0	1	1	Alarm when minutes and seconds match
0	0	0	1	Alarm when hours, minutes, and seconds match
0	0	0	0	Alarm when day, hours, minutes, and seconds match

## SPECIAL PURPOSE REGISTERS

The DS1306 has three additional registers (control register, status register, and trickle charger register) that control the real-time clock, interrupts, and trickle charger.

### CONTROL REGISTER (READ 0FH, WRITE 8FH)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	WP	0	0	0	1 Hz	AIE1	AIE0

**WP (Write Protect)** – Before any write operation to the clock or RAM, this bit must be logic 0. When high, the write protect bit prevents a write operation to any register, including bits 0, 1, and 2 of the control register. Upon initial power-up, the state of the WP bit is undefined. Therefore the WP bit should be cleared before attempting to write to the device. When WP is set, it must be cleared before any other control register bit can be written.

**1Hz (1Hz output enable)** – This bit controls the 1Hz output. When this bit is a logic 1, the 1Hz output is enabled. When this bit is a logic 0, the 1Hz output is High-Z.

**AIE0 (Alarm Interrupt Enable 0)** – When set to a logic 1, this bit permits the interrupt 0 request flag (IRQF0) bit in the status register to assert INT0. When the AIE0 bit is set to logic 0, the IRQF0 bit does not initiate the INT0 signal.

**AIE1 (Alarm Interrupt Enable 1)** – When set to a logic 1, this bit permits the interrupt 1 request flag (IRQF1) bit in the status register to assert INT1. When the AIE1 bit is set to logic 0, the IRQF1 bit does not initiate an interrupt signal, and the INT1 pin is set to a logic 0 state.

## STATUS REGISTER (READ 10H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	0	0	0	0	0	IRQF1	IRQF0

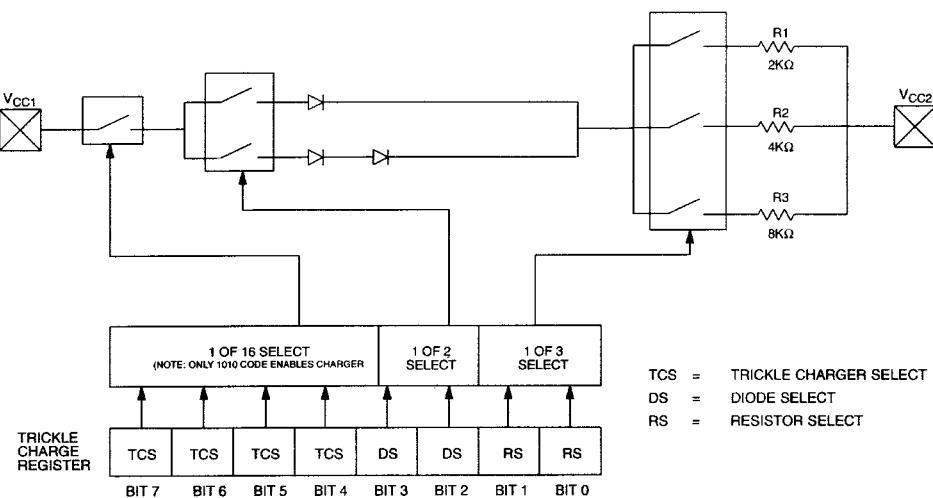
**IRQF0 (Interrupt 0 Request Flag)** – A logic 1 in the interrupt request flag bit indicates that the current time has matched the Alarm 0 registers. If the AIE0 bit is also a logic 1, the INT0 pin will go low. IRQF0 is cleared when the address pointer goes to any of the alarm 0 registers during a read or write. IRQF0 is activated when the device is powered by V<sub>CC1</sub>, V<sub>CC2</sub>, or V<sub>BAT</sub>.

**IRQF1 (Interrupt 1 Request Flag)** – A logic 1 in the interrupt request flag bit indicates that the current time has matched the Alarm 1 registers. If the AIE1 bit is also a logic 1, the INT1 pin will generate a 62.5ms active high pulse. IRQF1 is cleared when the address pointer goes to any of the alarm 1 registers during a read or write. IRQF1 is activated only when the device is powered by V<sub>CC2</sub> or V<sub>BAT</sub>.

## TRICKLE CHARGE REGISTER (READ 11H, WRITE 91H)

This register controls the trickle charge characteristics of the DS1306. The simplified schematic of Figure 3 shows the basic components of the trickle charger. The trickle charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1306 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2–3) select whether one diode or two diodes are connected between V<sub>CC1</sub> and V<sub>CC2</sub>. The diode select (DS) bits (bits 2–3) select whether one diode or two diodes are connected between V<sub>CC1</sub> and V<sub>CC2</sub>. The resistor select (RS) bits select the resistor that is connected between V<sub>CC1</sub> and V<sub>CC2</sub>. The resistor and diodes are selected by the RS and DS bits as shown in Table 2.

## PROGRAMMABLE TRICKLE CHARGER Figure 3



**TRICKLE CHARGER RESISTOR & DIODE SELECT Table 2**

TCS Bit 7	TCS Bit 6	TCS Bit 5	TCS Bit 4	DS Bit 3	DS Bit 2	RS Bit 1	RS Bit 0	FUNCTION
X	X	X	X	X	X	0	0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
1	0	1	0	0	1	0	1	1 Diode, 2kΩ
1	0	1	0	0	1	1	0	1 Diode, 4kΩ
1	0	1	0	0	1	1	1	1 Diode, 8kΩ
1	0	1	0	1	0	0	1	2 Diodes, 4kΩ
1	0	1	0	1	0	1	0	2 Diodes, 4kΩ
1	0	1	0	1	0	1	1	2 Diodes, 8kΩ

If RS is 00, the trickle charger is disabled independently of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to  $V_{CC1}$  and a super cap is connected to  $V_{CC2}$ . Also assume that the trickle charger has been enabled with one diode and resistor R1 between  $V_{CC1}$  and  $V_{CC2}$ . The maximum current  $I_{MAX}$  would, therefore, be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between  $V_{CC1}$  and  $V_{CC2}$  will decrease and, therefore, the charge current will decrease.

## POWER CONTROL

Power is provided through the  $V_{CC1}$ ,  $V_{CC2}$ , and  $V_{BAT}$  pins. Three different power supply configurations are illustrated in Figure 4. Configuration 1 shows the DS1306 being backed up by a non-rechargeable energy source such as a lithium battery. In this configuration, the system power supply is connected to  $V_{CC1}$  and  $V_{CC2}$  is grounded. When  $V_{CC}$  falls below  $V_{BAT}$  the device switches into a low-current battery backup mode. Upon power-up, the device switches from  $V_{BAT}$  to  $V_{CC}$  when  $V_{CC}$  is greater than  $V_{BAT} + 0.2V$ . The device is write protected whenever it is switched to  $V_{BAT}$ .

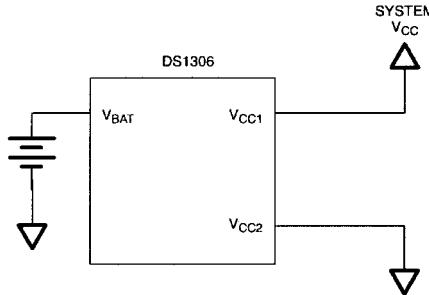
Configuration 2 illustrates the DS1306 being backed up by a rechargeable energy source. In this case, the  $V_{BAT}$  pin is grounded,  $V_{CC1}$  is connected to the primary power supply, and  $V_{CC2}$  is connected to the secondary supply (the rechargeable energy source). The DS1306 will operate from the larger of  $V_{CC1}$  or  $V_{CC2}$ . When  $V_{CC1}$  is greater than  $V_{CC2} + 0.2V$  (typical),  $V_{CC1}$  will power the DS1306. When  $V_{CC1}$  is less than  $V_{CC2}$ ,  $V_{CC2}$  will power the DS1306. The DS1306 does not write-protect itself in this configuration.

Configuration 3 shows the DS1306 in battery-operate mode, where the device is powered only by a single battery. In this case, the  $V_{CC1}$  and  $V_{BAT}$  pins are grounded and the battery is connected to the  $V_{CC2}$  pin.

Only these three configurations are allowed. Unused supply pins must be grounded.

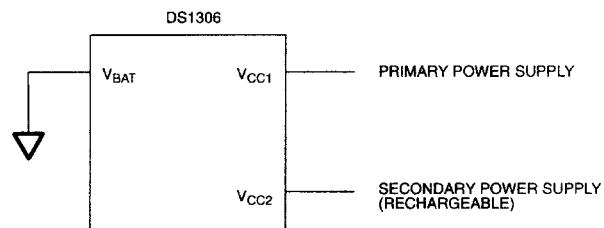
## POWER SUPPLY CONFIGURATIONS FOR THE DS1306 Figure 4

### Configuration 1: Backup Supply is a Nonrechargeable Lithium Battery



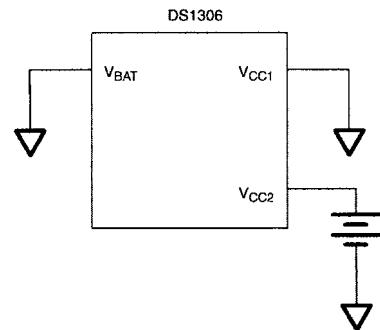
Note: Device is write protected if  $V_{CC} < V_{CCTP}$

### Configuration 2: Backup Supply is a Rechargeable Battery or Super Capacitor

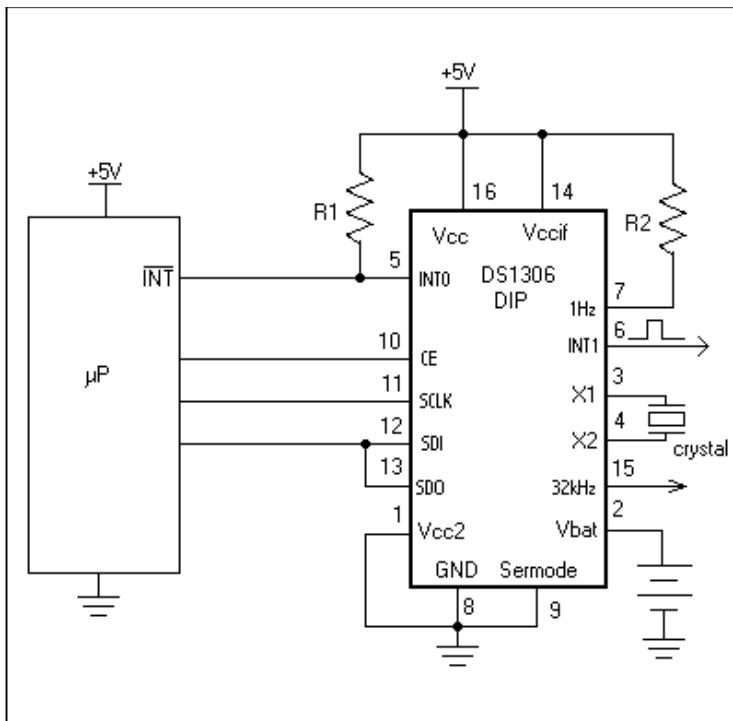


Note: Device does not provide automatic write protection.

### Configuration 3: Battery Operate Mode



## TYPICAL OPERATING CIRCUIT



## SERIAL INTERFACE

The DS1306 offers the flexibility to choose between two serial interface modes. The DS1306 can communicate with the SPI interface or with a standard 3-wire interface. The interface method used is determined by the SERMODE pin. When this pin is connected to V<sub>CC</sub>, SPI communication is selected. When this pin is connected to ground, standard 3-wire communication is selected.

## SERIAL PERIPHERAL INTERFACE (SPI)

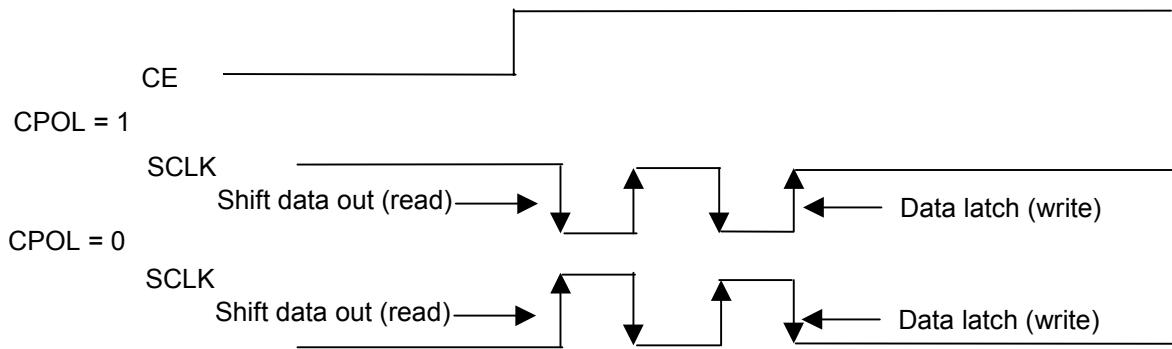
The serial peripheral interface (SPI) is a synchronous bus for address and data transfer and is used when interfacing with the SPI bus on specific Motorola microcontrollers such as the 68HC05C4 and the 68HC11A8. The SPI mode of serial communication is selected by tying the SERMODE pin to V<sub>CC</sub>.

Four pins are used for the SPI. The four pins are the SDO (serial data out), SDI (serial data in), CE (chip enable), and SCLK (serial clock). The DS1306 is the slave device in an SPI application, with the microcontroller being the master.

The SDI and SDO pins are the serial data input and output pins for the DS1306, respectively. The CE input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave (DS1306) devices.

The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is programmable in some microcontrollers. The DS1306 determines on the clock polarity by sampling SCLK when CE becomes active. Therefore either SCLK polarity can be accommodated. Input data (SDI) is latched on the internal strobe edge and output data (SDO) is shifted out on the shift edge (See Figure 5). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight.

## SERIAL CLOCK AS A FUNCTION OF MICROCONTROLLER CLOCK POLARITY (CPOL) Figure 5



CPHA bit polarity in the processor (if applicable) may need to be set accordingly.

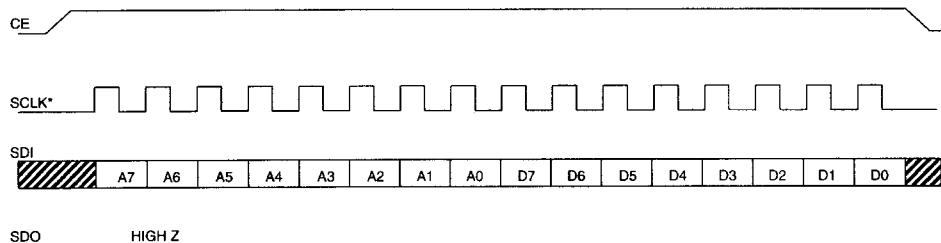
CPOL is a bit that is set in the microcontroller's control register.

SDO remains at High-Z until 8 bits of data are ready to be shifted out during a read.

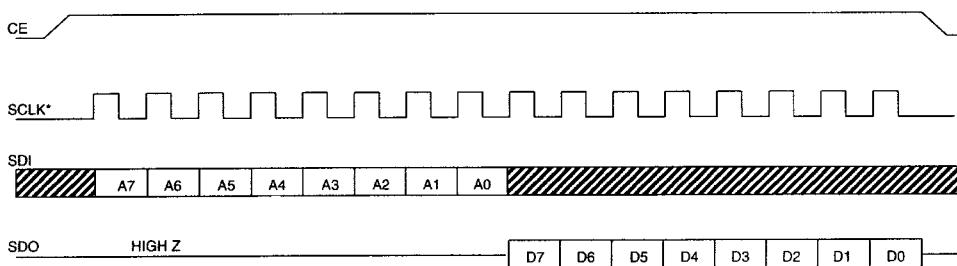
## ADDRESS AND DATA BYTES

Address and data bytes are shifted MSB first into the serial data input (SDI) and out of the serial data output (SDO). Any transfer requires the address of the byte to specify a write or read to either a RTC or RAM location, followed by one or more bytes of data. Data is transferred out of the SDO for a read operation and into the SDI for a write operation (See Figures 6 and 7).

## SPI SINGLE-BYTE WRITE Figure 6



## SPI SINGLE-BYTE READ Figure 7



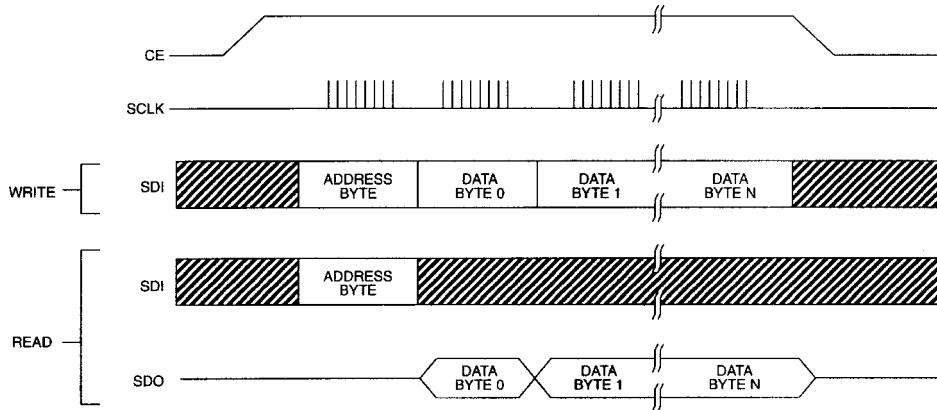
\* SCLK can be either polarity.

The address byte is always the first byte entered after CE is driven high. The most significant bit (A7) of this byte determines if a read or write will take place. If A7 is 0, one or more read cycles will occur. If A7 is 1, one or more write cycles will occur.

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Data transfers can occur 1 byte at a time or in multiple-byte burst mode. After CE is driven high an address is written to the DS1306. After the address, 1 or more data bytes can be written or read. For a single-byte transfer 1 byte is read or written and then CE is driven low. For a multiple-byte transfer, however, multiple bytes can be read or written to the DS1306 after the address has been written. Each read or write cycle causes the RTC register or RAM address to automatically increment. Incrementing continues until the device is disabled. When the RTC is selected, the address wraps to 00h after incrementing to 1Fh (during a read) and wraps to 80h after incrementing to 9Fh (during a write). When the RAM is selected, the address wraps to 20h after incrementing to 7Fh (during a read) and wraps to A0h after incrementing to FFh (during a write).

## SPI MULTIPLE-BYTE BURST TRANSFER Figure 8



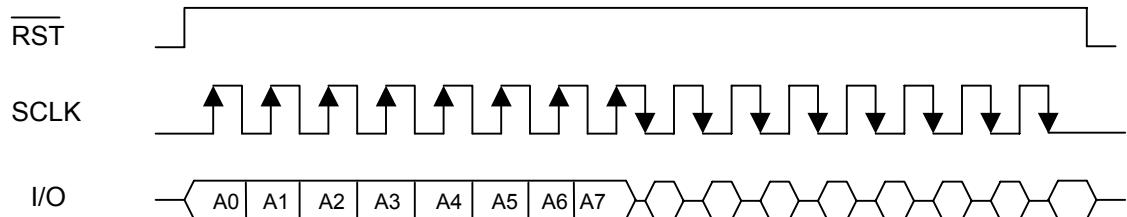
## 3-WIRE INTERFACE

The 3-wire interface mode operates similar to the SPI mode. However, in 3-wire mode there is one I/O instead of separate data in and data out signals. The 3-wire interface consists of the I/O (SDI and SDO pins tied together), CE, and SCLK pins. In 3-wire mode, each byte is shifted in LSB first, unlike SPI mode, where each byte is shifted in MSB first.

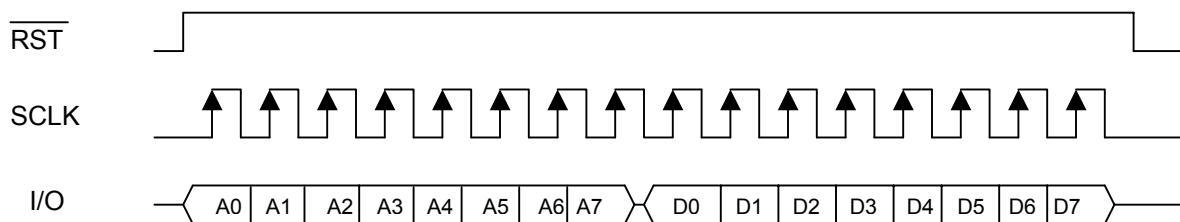
As is the case with the SPI mode, an address byte is written to the device followed by a single data byte or multiple data bytes. Figure 9 illustrates a read and write cycle. In 3-wire mode, data is input on the rising edge of SCLK and output on the falling edge of SCLK.

## 3-WIRE SINGLE BYTE TRANSFER Figure 9

### SINGLE BYTE READ



### SINGLE BYTE WRITE



I/O is SDI and SDO tied together.

In burst mode, **RST** is kept high and additional SCLK cycles are sent until the end of the burst.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds (DIP)
	See IPC/JEDEC Standard J-STD-020A for Surface Mount Devices

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Range	Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	2.0V to 5.5V V <sub>CC1</sub> or V <sub>CC2</sub>
Industrial	-40°C to +85°C	2.0V to 5.5V V <sub>CC1</sub> or V <sub>CC2</sub>

**RECOMMENDED DC OPERATING CONDITIONS**

(Over the operating range\*)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage V <sub>CC1</sub> , V <sub>CC2</sub>	V <sub>CC1</sub> , V <sub>CC2</sub>	2.0		5.5	V	1, 8
Logic 1 Input	V <sub>IH</sub>	2.0		V <sub>CC</sub> + 0.3	V	
Logic 0 Input	V <sub>IL</sub>	V <sub>CC</sub> = 2.0V	-0.3	+0.3	V	
		V <sub>CC</sub> = 5V	-0.3	+0.8		
V <sub>BAT</sub> Battery Voltage	V <sub>BAT</sub>	2.0		5.5	V	
V <sub>CCIF</sub> Supply Voltage	V <sub>CCIF</sub>	2.0		5.5	V	10

\*Unless otherwise specified.

**DC ELECTRICAL CHARACTERISTICS**

(Over the operating range\*)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I <sub>LI</sub>	-100		+500	µA	
Output Leakage	I <sub>LO</sub>	-1		1	µA	
Logic 0 Output I <sub>OL</sub> = 1.5mA I <sub>OL</sub> = 4.0mA	V <sub>OL</sub>	V <sub>CC</sub> = 2.0		0.4	V	
		V <sub>CC</sub> = 5V		0.4		
Logic 1 Output I <sub>OH</sub> = -0.4mA I <sub>OH</sub> = -1.0mA	V <sub>OH</sub>	V <sub>CCIF</sub> = 2.0V	1.6		V	
		V <sub>CCIF</sub> = 5V	2.4			
Logic 1 Output Current (INT1 pin)	I <sub>OH</sub> , INT1	(V <sub>CC2</sub> , V <sub>BAT</sub> ) -0.3V	-100			µA
V <sub>CC1</sub> Active Supply Current	I <sub>CC1A</sub>	V <sub>CC1</sub> = 2.0V		0.425	mA	2,7
		V <sub>CC1</sub> = 5V		1.28		
V <sub>CC1</sub> Timekeeping Current	I <sub>CC1T</sub>	V <sub>CC1</sub> = 2.0V		25.3	µA	1,7
		V <sub>CC1</sub> = 5V		81		
V <sub>CC2</sub> Active Supply Current	I <sub>CC2A</sub>	V <sub>CC2</sub> = 2.0V		0.4	mA	2,8
		V <sub>CC2</sub> = 5V		1.2		
V <sub>CC2</sub> Timekeeping Current	I <sub>CC2T</sub>	V <sub>CC2</sub> = 2.0V		0.4	µA	1,8
		V <sub>CC2</sub> = 5V		1		
Battery Timekeeping Current	I <sub>BAT</sub>	V <sub>BAT</sub> = 3V		550	nA	9
Battery Timekeeping Current (IND)	I <sub>BAT</sub>	V <sub>BAT</sub> = 3V		800	nA	9
V <sub>CC</sub> Trip Point	V <sub>CCTP</sub>		V <sub>BAT</sub> - 50	V <sub>BAT</sub> + 200	mV	
Trickle Charge Resistors	R1 R2 R3			2 4 8	kΩ kΩ kΩ	
Trickle Charger Diode Voltage Drop	V <sub>TD</sub>			0.7	V	

\*Unless otherwise specified.

**CAPACITANCE**(T<sub>A</sub> = 25°C)

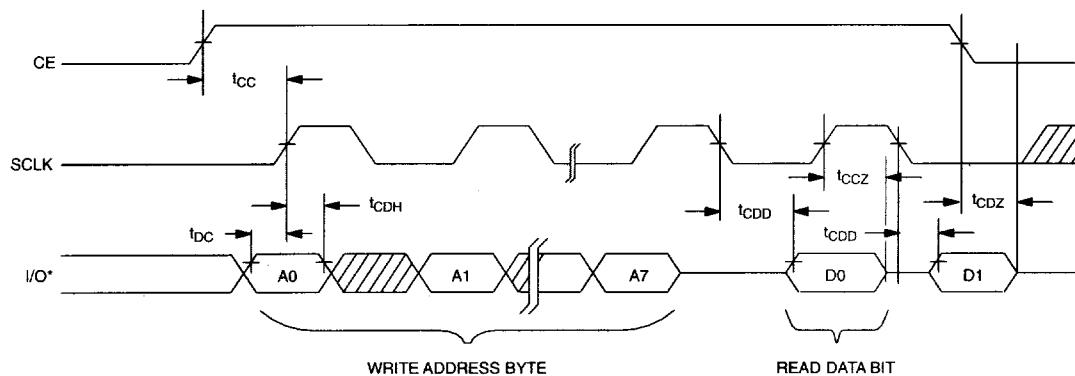
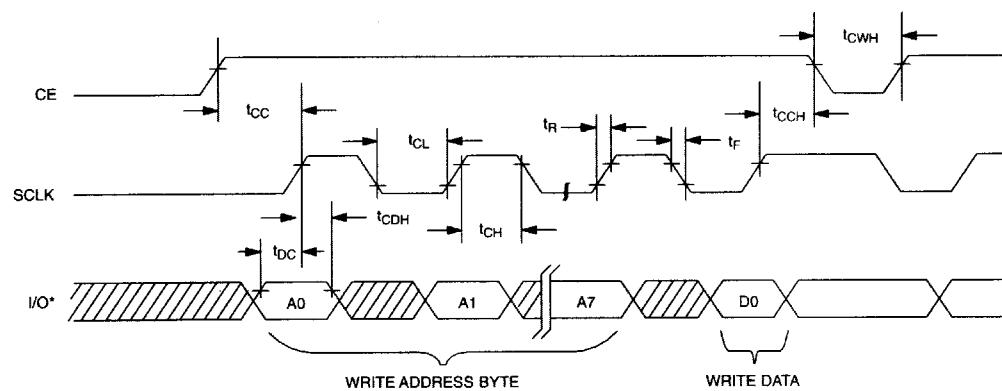
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>I</sub>		10		pF	
Output Capacitance	C <sub>O</sub>		15		pF	
Crystal Capacitance	C <sub>X</sub>		6		pF	

**3-WIRE AC ELECTRICAL CHARACTERISTICS**

(Over the operating range\*)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	$t_{DC}$	$V_{CC} = 2.0V$	200			ns 3,4
		$V_{CC} = 5V$	50			
CLK to Data Hold	$t_{CDH}$	$V_{CC} = 2.0V$	280			ns 3,4
		$V_{CC} = 5V$	70			
CLK to Data Delay	$t_{CDD}$	$V_{CC} = 2.0V$		800		ns 3,4,5
		$V_{CC} = 5V$		200		
CLK Low Time	$t_{CL}$	$V_{CC} = 2.0V$	1000			ns 4
		$V_{CC} = 5V$	250			
CLK High Time	$t_{CH}$	$V_{CC} = 2.0V$	1000			ns 4
		$V_{CC} = 5V$	250			
CLK Frequency	$t_{CLK}$	$V_{CC} = 2.0V$		0.6		MHz 4
		$V_{CC} = 5V$	DC	2.0		
CLK Rise and Fall	$t_R, t_F$	$V_{CC} = 2.0V$		2000		ns
		$V_{CC} = 5V$		500		
CE to CLK Setup	$t_{CC}$	$V_{CC} = 2.0V$	4			$\mu s$ 4
		$V_{CC} = 5V$	1			
CLK to CE Hold	$t_{CCH}$	$V_{CC} = 2.0V$	240			ns 4
		$V_{CC} = 5V$	60			
CE Inactive Time	$t_{CWH}$	$V_{CC} = 2.0V$	4			$\mu s$ 4
		$V_{CC} = 5V$	1			
CE to Output High-Z	$t_{CDZ}$	$V_{CC} = 2.0V$		280		ns 3,4
		$V_{CC} = 5V$		70		
SCLK to Output High-Z	$t_{CCZ}$	$V_{CC} = 2.0V$		280		ns 3,4
		$V_{CC} = 5V$		70		

\*Unless otherwise noted.

**TIMING DIAGRAM: 3-WIRE READ DATA TRANSFER Figure 10****TIMING DIAGRAM: 3-WIRE WRITE DATA TRANSFER Figure 11**

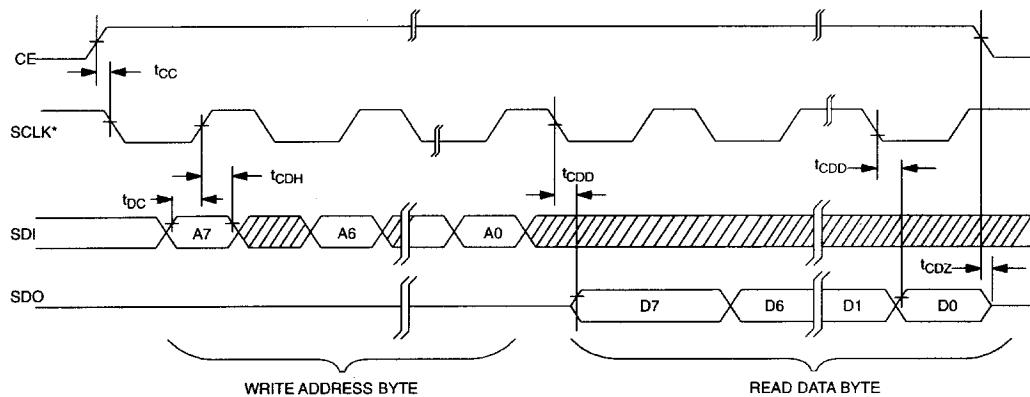
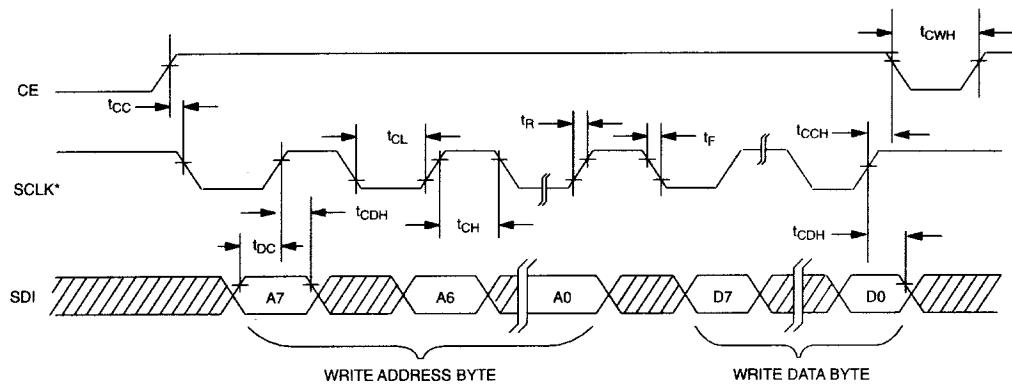
\* I/O is SDI and SDO tied together.

**SPI AC ELECTRICAL CHARACTERISTICS**

(Over the operating range\*)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	$t_{DC}$	$V_{CC} = 2.0V$	200			3,4
		$V_{CC} = 5V$	50			
CLK to Data Hold	$t_{CDH}$	$V_{CC} = 2.0V$	280			3,4
		$V_{CC} = 5V$	70			
CLK to Data Delay	$t_{CDD}$	$V_{CC} = 2.0V$		800		3,4,5
		$V_{CC} = 5V$		200		
CLK Low Time	$t_{CL}$	$V_{CC} = 2.0V$	1000			4
		$V_{CC} = 5V$	250			
CLK High Time	$t_{CH}$	$V_{CC} = 2.0V$	1000			4
		$V_{CC} = 5V$	250			
CLK Frequency	$t_{CLK}$	$V_{CC} = 2.0V$		0.6		MHz
		$V_{CC} = 5V$	DC	2.0		
CLK Rise and Fall	$t_R, t_F$	$V_{CC} = 2.0V$		2000		ns
		$V_{CC} = 5V$		500		
CE to CLK Setup	$t_{CC}$	$V_{CC} = 2.0V$	4			$\mu s$
		$V_{CC} = 5V$	1			
CLK to CE Hold	$t_{CCH}$	$V_{CC} = 2.0V$	240			ns
		$V_{CC} = 5V$	60			
CE Inactive Time	$t_{CWH}$	$V_{CC} = 2.0V$	4			$\mu s$
		$V_{CC} = 5V$	1			
CE to Output High-Z	$t_{CDZ}$	$V_{CC} = 2.0V$		280		ns
		$V_{CC} = 5V$		70		

\*Unless otherwise noted.

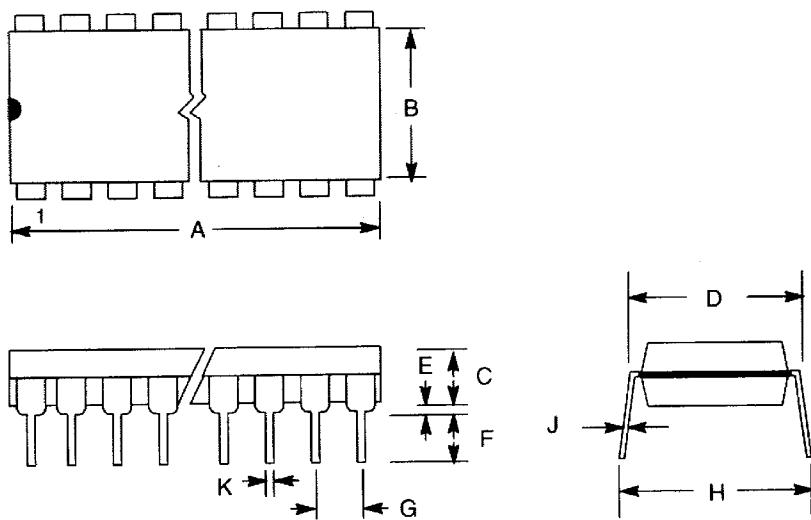
**TIMING DIAGRAM: SPI READ DATA TRANSFER Figure 12****TIMING DIAGRAM: SPI WRITE DATA TRANSFER Figure 13**

SCLK can be either polarity, timing shown for CPOL = 1.

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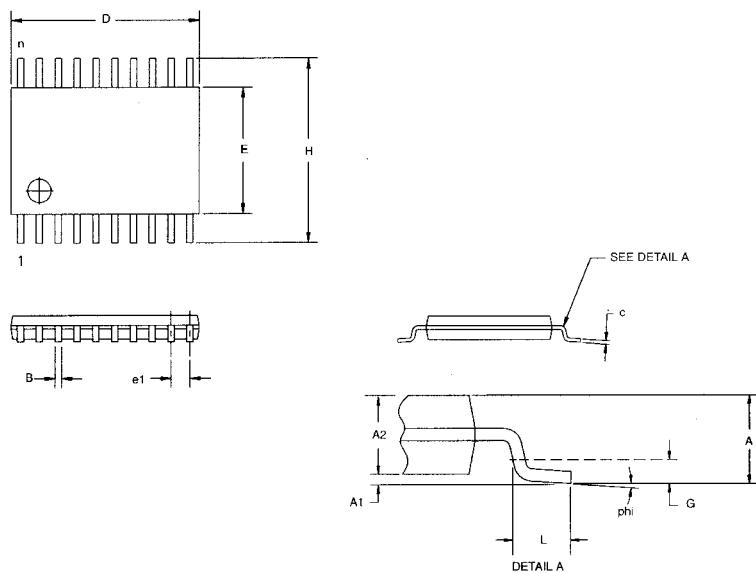
**NOTES:**

1.  $I_{CC1T}$  and  $I_{CC2T}$  are specified with CE set to a logic 0.
2.  $I_{CC1A}$  and  $I_{CC2A}$  are specified with  $CE = V_{CC}$ ,  $SCLK = 2\text{MHz}$  at  $V_{CC} = 5\text{V}$ ;  $SCLK = 500\text{kHz}$  at  $V_{CC} = 2.0\text{V}$ ,  $V_{IL} = 0\text{V}$ ,  $V_{IH} = V_{CC}$ .
3. Measured at  $V_{IH} = 2.0\text{V}$  or  $V_{IL} = 0.8\text{V}$  and 10ms maximum rise and fall time.
4. Measured with 50pF load.
5. Measured at  $V_{OH} = 2.4\text{V}$  or  $V_{OL} = 0.4\text{V}$ .
6.  $V_{CC} = V_{CC1}$ , when  $V_{CC1} > V_{CC2} + 0.2\text{V}$  (typical);  $V_{CC} = V_{CC2}$ , when  $V_{CC2} > V_{CC1}$ .
7.  $V_{CC2} = 0\text{V}$ .
8.  $V_{CC1} = 0\text{V}$ .
9.  $V_{CC1} < V_{BAT}$ .
10.  $V_{CC1F}$  must be less than or equal to the largest of  $V_{CC1}$ ,  $V_{CC2}$ , and  $V_{BAT}$ .

**DS1306 16-PIN DIP (300-MIL)**

PKG	16-PIN	
DIM	MIN	MAX
<b>A IN</b>	0.740	0.780
<b>MM</b>	18.80	19.81
<b>B IN</b>	0.240	0.260
<b>MM</b>	6.10	6.60
<b>C IN</b>	0.120	0.140
<b>MM</b>	3.05	3.56
<b>D IN</b>	0.300	0.325
<b>MM</b>	7.62	8.26
<b>E IN</b>	0.015	0.040
<b>MM</b>	0.38	1.02
<b>F IN</b>	0.120	0.140
<b>MM</b>	3.05	3.56
<b>G IN</b>	0.090	0.110
<b>MM</b>	2.29	2.79
<b>H IN</b>	0.320	0.370
<b>MM</b>	8.13	9.40
<b>J IN</b>	0.008	0.012
<b>MM</b>	0.20	0.30
<b>K IN</b>	0.015	0.021
<b>MM</b>	0.38	0.53

## DS1306 20-PIN TSSOP



<b>DIM</b>	<b>MIN</b>	<b>MAX</b>
<b>A MM</b>	-	1.10
<b>A1 MM</b>	0.05	-
<b>A2 MM</b>	0.75	1.05
<b>C MM</b>	0.09	0.18
<b>L MM</b>	0.50	0.70
<b>e1 MM</b>	0.65 BSC	
<b>B MM</b>	0.18	0.30
<b>D MM</b>	6.40	6.90
<b>E MM</b>	4.40 NOM	
<b>G MM</b>	0.25 REF	
<b>H MM</b>	6.25	6.55
<b>phi</b>	0°	8°