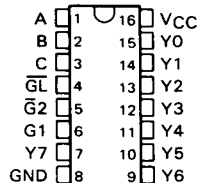


SN54HC137, SN74HC137 3-LINE TO 8-LINE DECODERS/DEMULPLEXERS WITH ADDRESS LATCHES

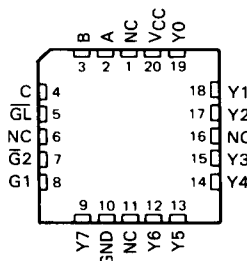
D2684, DECEMBER 1982—REVISED JUNE 1989

- Combines Decoder and 3-Bit Address Latch
- Incorporates 2 Output Enables to Simplify Cascading
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC137 . . . J PACKAGE
SN74HC137 . . . D[†] OR N PACKAGE
(TOP VIEW)



SN54HC137 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

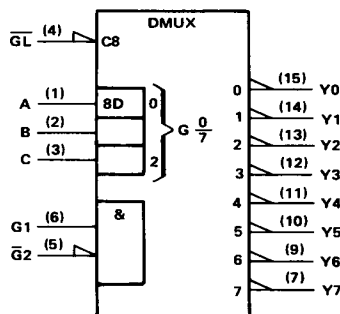
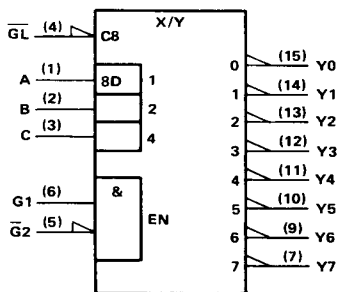
[†]Contact the factory for D availability

description

The 'HC137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input (\overline{GL}) is low, the 'HC137 acts as a decoder/demultiplexer. When \overline{GL} goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as \overline{GL} remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'HC137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HC137 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC137 is characterized for operation from -40°C to 85°C .

logic symbols[†] (alternatives)



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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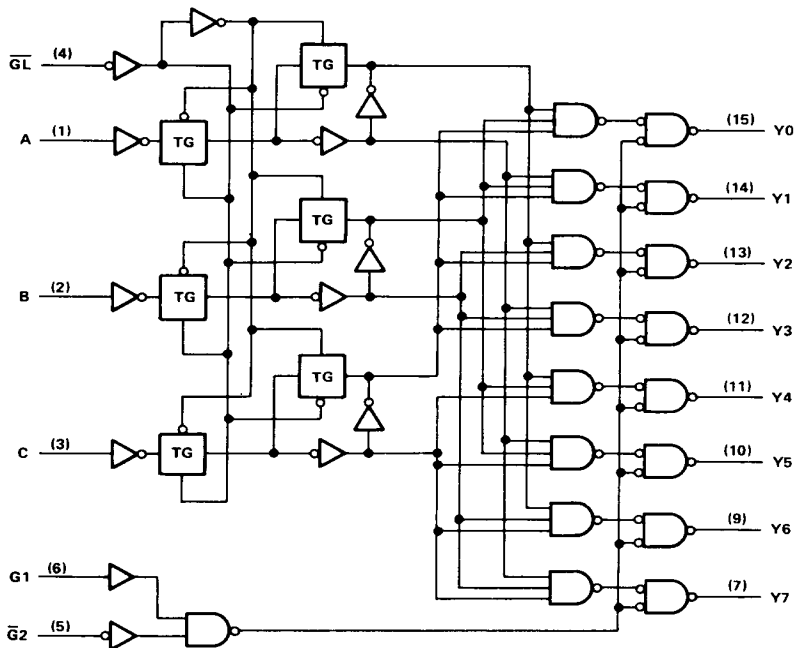
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HCMOS Devices

SN54HC137, SN74HC137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
WITH ADDRESS LATCHES

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
GL	G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H
L	H	L	H	H	L	H	H	H	H	H	L	H	H
L	H	L	H	H	H	H	H	H	H	H	H	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

SN54HC137, SN74HC137

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

WITH ADDRESS LATCHES

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC137			SN74HC137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
	$V_{CC} = 4.5$ V	3.15			3.15			
	$V_{CC} = 6$ V	4.2			4.2			
V_{IL} Low-level input voltage	$V_{CC} = 2$ V	0		0.3	0		0.3	V
	$V_{CC} = 4.5$ V	0		0.9	0		0.9	
	$V_{CC} = 6$ V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	$V_{CC} = 2$ V	0		1000	0		1000	ns
	$V_{CC} = 4.5$ V	0		500	0		500	
	$V_{CC} = 6$ V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC137		SN74HC137		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.80		5.2		5.34		V
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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HCMS Devices

SN54HC137, SN74HC137 **3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS** **WITH ADDRESS LATCHES**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC137		SN74HC137		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, $\overline{\text{GL}}$ low	2 V 4.5 V 6 V	80 16 14		120 24 20		100 20 17		ns
t _{su} Setup time, A, B, and C before $\overline{\text{GL}}$ ↑	2 V 4.5 V 6 V	75 15 13		115 23 20		95 19 16		ns
t _h Hold time, A, B, and C after $\overline{\text{GL}}$ ↓	2 V 4.5 V 6 V	5 5 5		5 5 5		5 5 5		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC137		SN74HC137		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, C	Y	2 V 4.5 V 6 V		82 23 19	190 38 32		285 57 48		240 48 41	ns
t _{pd}	$\overline{\text{G2}}$	Y	2 V 4.5 V 6 V		59 17 14	145 29 25		220 44 37		180 36 31	ns
t _{pd}	G1	Y	2 V 4.5 V 6 V		61 17 14	145 29 25		220 44 37		180 36 31	ns
t _{pd}	$\overline{\text{GL}}$	Y	2 V 4.5 V 6 V		77 22 19	190 38 32		285 57 48		240 48 41	ns
t _t		Y	2 V 4.5 V 6 V		38 8 6	75 15 13		110 22 19		95 19 16	ns

C _{pd}	Power dissipation capacitance	No load, T _A = 25°C	85 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.