FDB9506L-F085

Power MOSFET

−40 V, 3.6 mΩ, −110 A, Single P−Channel

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−40	V
Gate−to−Source Voltage			V_{GS}	±16	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	−110	A
		T_C = 100°C		−110	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	176	W
		T_C = 100°C		88	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	−24.5	A
		T_A = 100°C		−17.3	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.5	W
		T_A = 100°C		1.7	
Pulsed Drain Current	T_C = 25°C, t_p = 10 μs		I_{DM}	−1260	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode) (Note 1)			I_S	−110	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = −86 A)			E_{AS}	370	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	0.85	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	43	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Maximum current is limited by package configuration.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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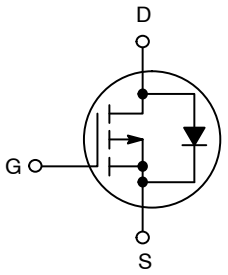
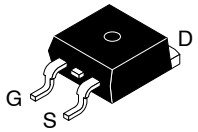
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
−40 V	3.6 mΩ @ −10 V	−80 A
	5.0 mΩ @ −4.5 V	

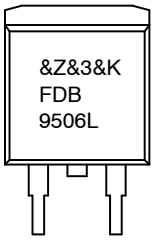


P−CHANNEL MOSFET



D^2PAK−3
TO−263
CASE 418AJ

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDB9506L	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	−40	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		–	−22	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −40 V, T_J = 25°C	–	–	−1	μA
		V_{GS} = 0 V, V_{DS} = −40 V, T_J = 175°C	–	–	−1	mA
Zero Gate Voltage Drain Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V	–	–	±100	nA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = −250 μA	−1	−1.8	−3	V
Threshold Temperature Coefficient	$V_{GS(th)}/T_J$		–	−6.4	–	mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −80 A	–	2.8	3.6	mΩ
		V_{GS} = −4.5 V, I_D = −40 A	–	3.9	5.0	
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 100 KHz, V_{DS} = −20 V	–	9100	–	pF
Output Capacitance	C_{oss}		–	3300	–	pF
Reverse Transfer Capacitance	C_{rss}		–	140	–	pF
Gate Resistance	R_g	V_{GS} = 0.5 V, f = 100 KHz	–	19	–	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −32 V, I_D = −80 A	–	126	–	nC
		V_{GS} = −4.5 V, V_{DS} = −32 V, I_D = −80 A	–	58	–	
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to −1 V	–	8	–	
Gate−to−Source Gate Charge	Q_{gs}	V_{DD} = −32 V, I_D = −80 A	–	27	–	
Gate−to−Drain “Miller” Charge	Q_{gd}		–	16	–	
Plateau Voltage	V_{GP}		–	−3.2	–	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −20 V, I_D = −80 A, V_{GS} = −10 V, R_{GEN} = 6 Ω	–	12	–	ns
Turn-On Rise Time	t_r		–	9	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	474	–	ns
Turn-Off Fall Time	t_f		–	140	–	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
Source−to−Drain Diode Voltage	V_{SD}	I_{SD} = −80 A, V_{GS} = 0 V	–	−0.91	−1.25	V
		I_{SD} = −40 A, V_{GS} = 0 V	–	−0.84	−1.2	V
Reverse Recovery Time	T_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs I_S = −80 A	–	87	–	ns
Charge Time	t_a		–	42	–	
Discharge Time	t_b		–	45	–	
Reverse Recovery Charge	Q_{RR}		–	101	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

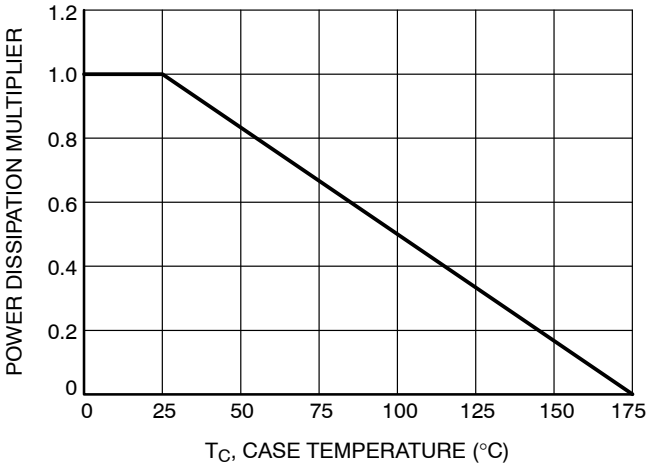


Figure 1. Normalized Power Dissipation vs. Case Temperature

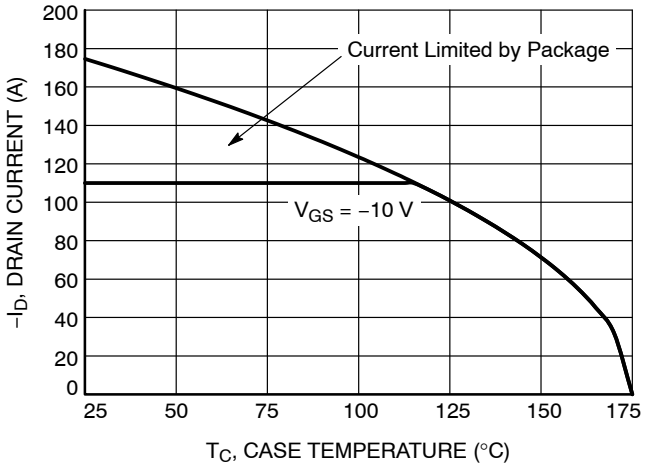


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

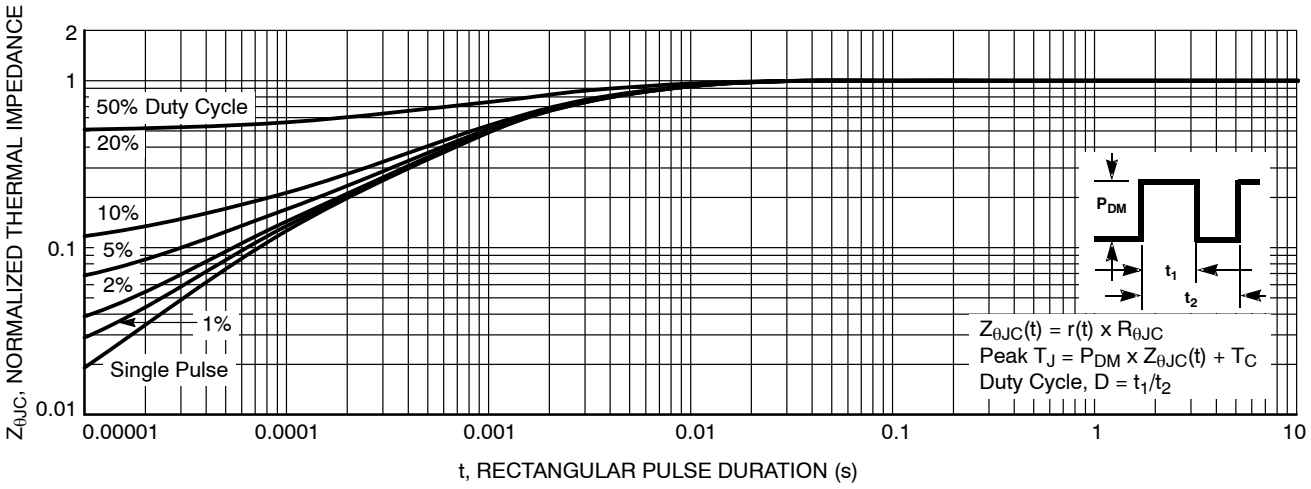


Figure 3. Normalized Maximum Transient Thermal Impedance

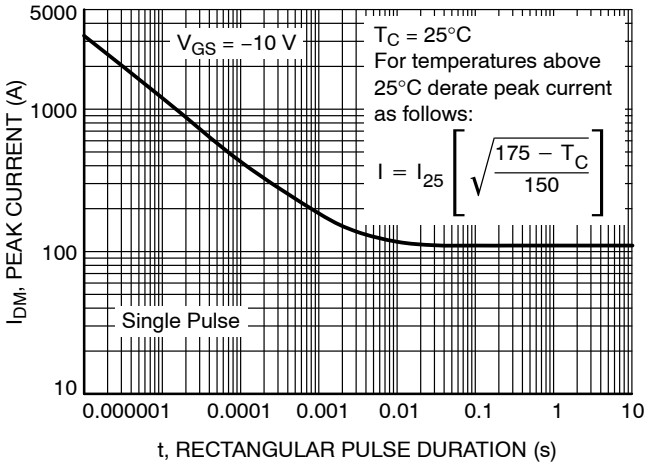


Figure 4. Peak Current Capability

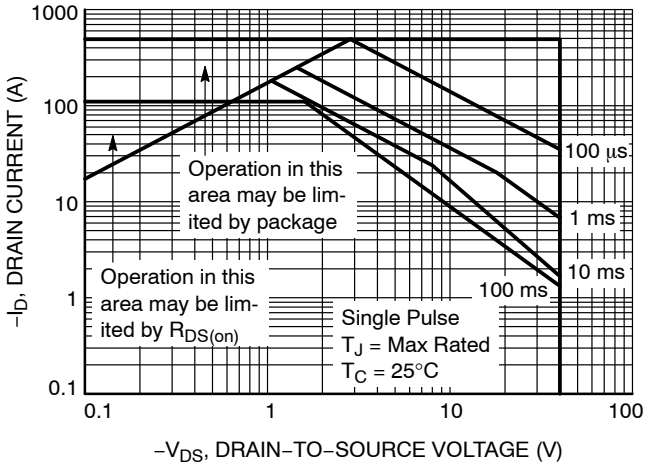


Figure 5. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

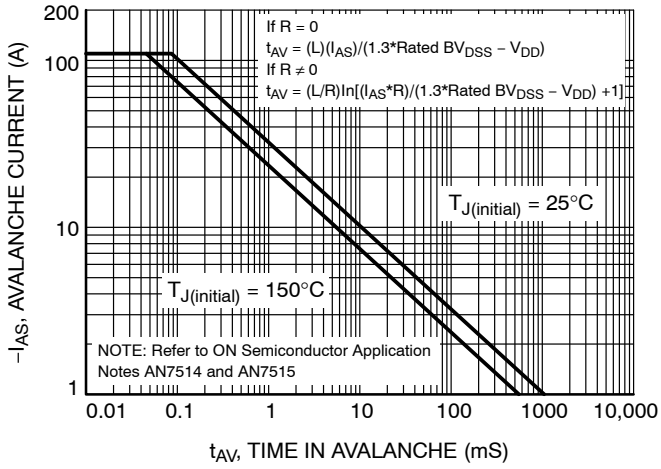


Figure 6. Unclamped Inductive Switching Capability

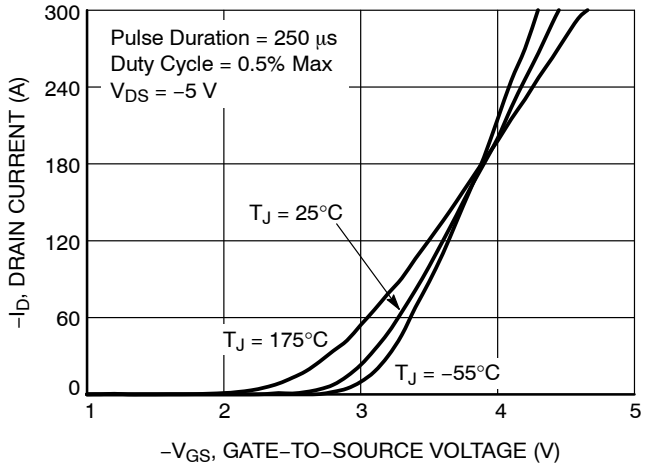


Figure 7. Transfer Characteristics

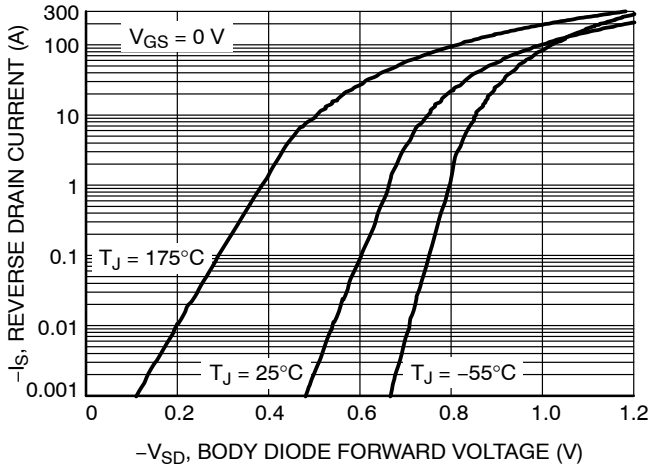


Figure 8. Forward Diode Characteristics

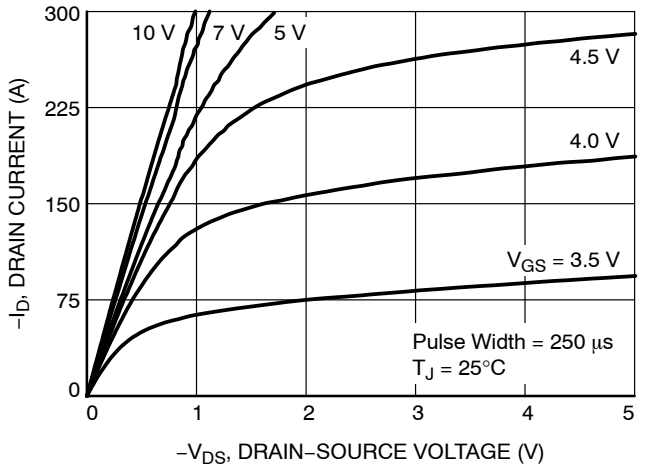


Figure 9. Saturation Characteristics

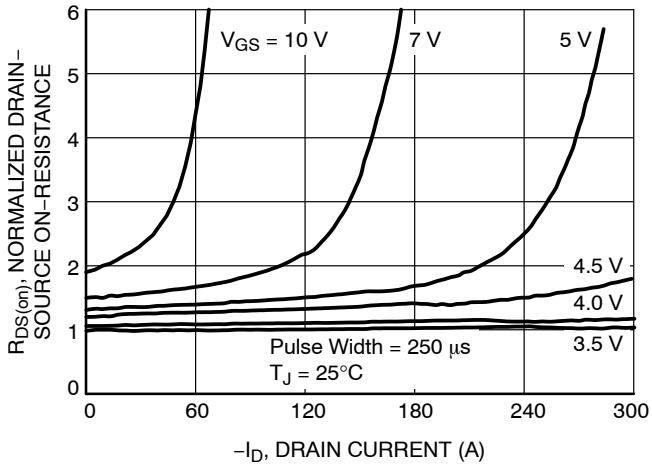


Figure 10. Normalized $R_{DS(on)}$ vs. Drain Current

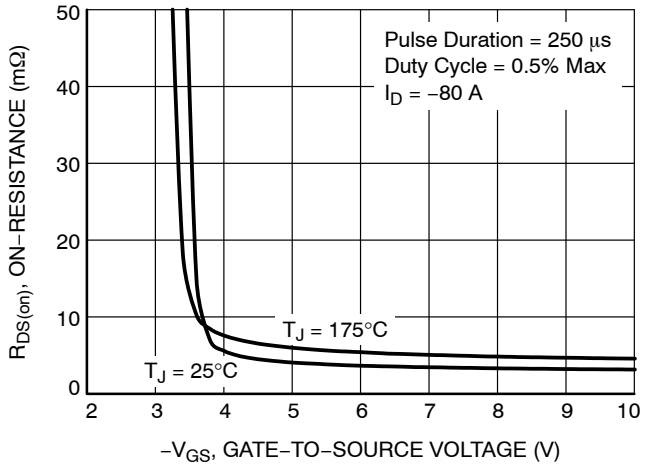


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

TYPICAL CHARACTERISTICS

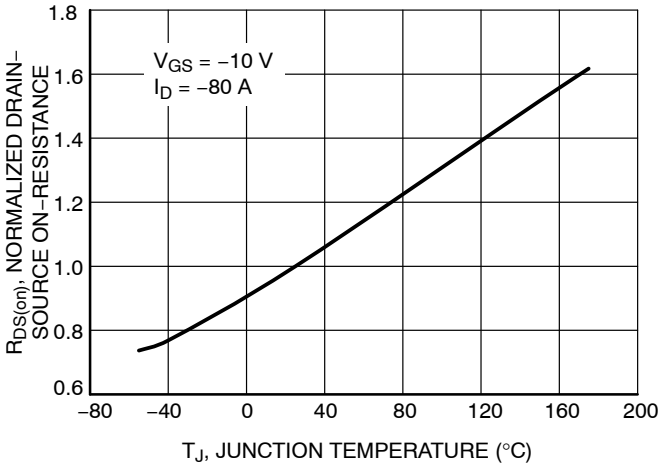


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

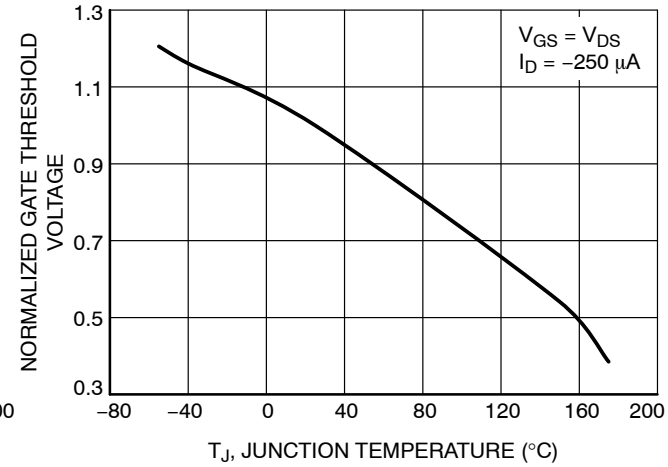


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

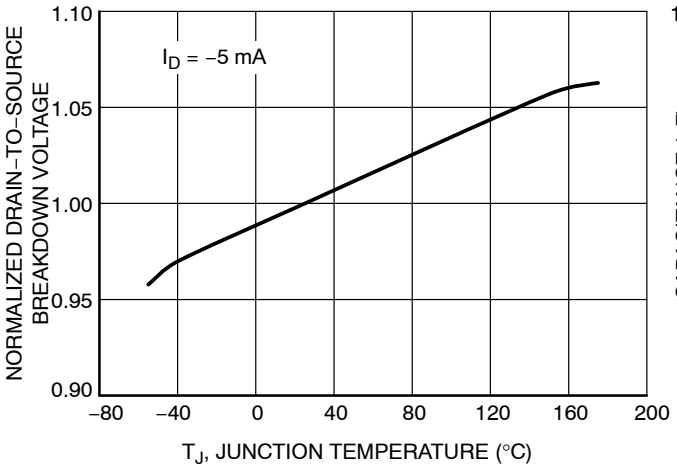


Figure 14. Normalized Drain−to−Source Breakdown Voltage vs. Junction Temperature

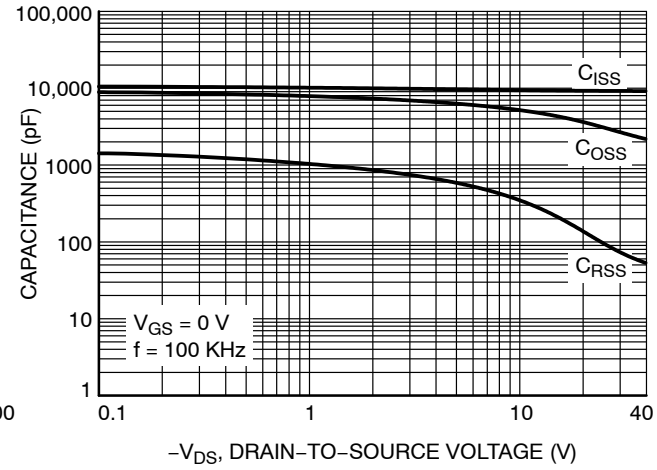


Figure 15. Capacitance vs. Drain−to−Source Voltage

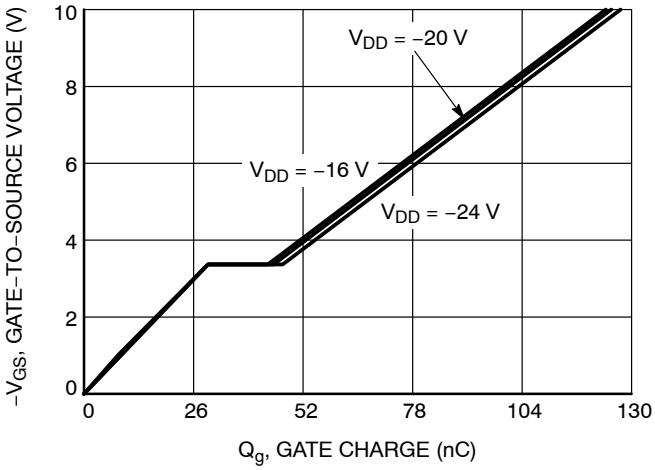
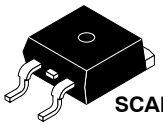


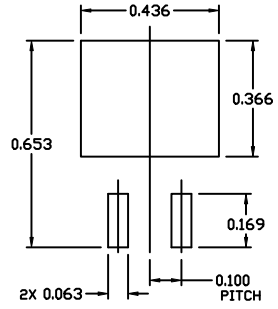
Figure 16. Gate Charge vs. Gate−to−Source Voltage

D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



SCALE 1:1



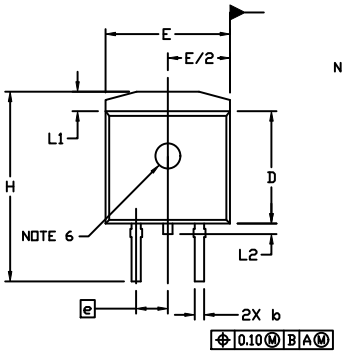
RECOMMENDED
MOUNTING FOOTPRINT

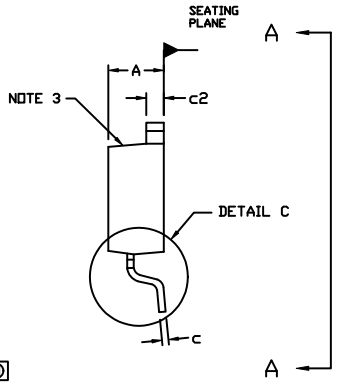
* For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

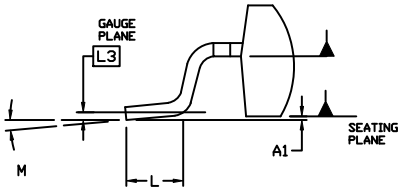
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② … OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

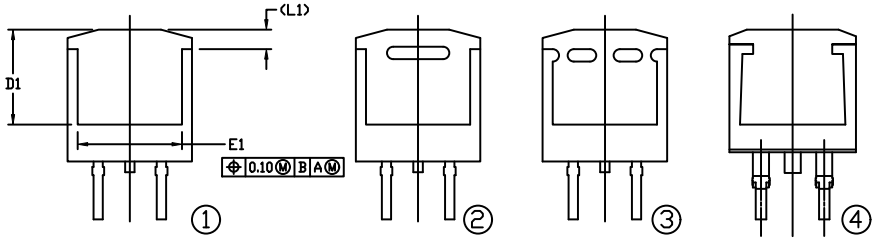
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°







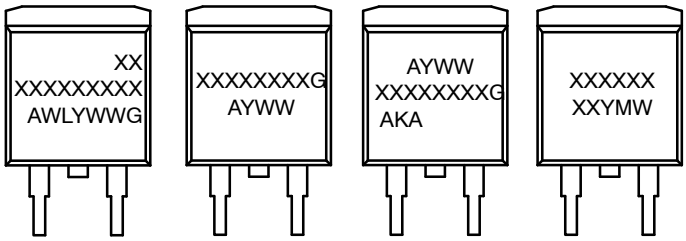
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

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