◇ STRUCTURE Silicon Monolithic Integrated Circuit
◇ PRODUCT Microwire BUS 4Kbit(256×16bit) EEPROM

# ◇ PART NUMBER BR93L66-W Series

| PART NUMBER | PACKAGE |
|---|---|
| BR93L66F-W | SOP8 |
| BR93L66RF-W | SOP8 |
| BR93L66FJ-W | SOP-J8 |
| BR93L66RFJ-W | SOP-J8 |
| BR93L66FV-W | SSOP-B8 |
| BR93L66RFV-W | SSOP-B8 |
| BR93L66FVT-W | TSSSOP-B8 |
| BR93L66RFVT-W | TSSSOP-B8 |
| BR93L66RFVM-W | MSOP8 |
| BR93L66RFVJ-W | TSSOP-B8J |

◇ FEATURES
Microwire BUS EEPROM
Wide operating supply voltage range(1.8V～5.5V)
1,000,000 erase/write cycles endurance

◇ ABSOLUTE MAXIMUM RATING (Ta=25℃)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | Vcc | -0.3～6.5 | V |
| Power Dissipation | Pd | 450 (BR93L66F-W) *1 | mW |
| | | 450 (BR93L66RF-W) *2 | |
| | | 450 (BR93L66FJ-W) *3 | |
| | | 450 (BR93L66RFJ-W) *4 | |
| | | 300 (BR93L66FV-W) *5 | |
| | | 300 (BR93L66RFV-W) *6 | |
| | | 330 (BR93L66FVT-W) *7 | |
| | | 330 (BR93L66RFVT-W) *8 | |
| | | 310 (BR93L66RFVM-W) *9 | |
| | | 310 (BR93L66RFVJ-W) *10 | |
| Storage Temperature | Tstg | -65～125 | ℃ |
| Operating Temperature | Topr | -40～85 | ℃ |
| Terminal Voltage | — | -0.3～Vcc+0.3 | V |

* Degradation is done at 4.5mW/℃ (*1,*2,*3,*4), 3.0mW/℃ (*5,*6), 3.3mW/℃ (*7,*8), 3.1mW/℃(*9,*10) for operation above 25℃

◇ RECOMMENDED OPERATING CONDITION

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | Vcc | 1.8～5.5 | V |
| Input Voltage | VIN | 0～Vcc | V |

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

## ◇ MEMORY CELL CHARACTERISTICS (Ta=25℃, Vcc=1.8～5.5V)

| Parameter | | Specification | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max | |
| Erase/Write Cycle | *1 | 1,000,000 | - | - | Cycles |
| Data Retention | *1 | 40 | - | - | Years |

○Initial Data FFFFh in all address. *1 Not 100% TESTED

## ◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40～85℃, Vcc=1.8～5.5V)

| Parameter | Symbol | Specification | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max | | |
| "L" Input Voltage1 | VIL1 | -0.3 | — | 0.8 | V | 4.0≦Vcc≦5.5 |
| "L" Input Voltage2 | VIL2 | -0.3 | — | 0.2×Vcc | V | 1.8≦Vcc≦4.0 |
| "H" Input Voltage1 | VIH1 | 2.0 | — | Vcc+0.3 | V | 4.0≦Vcc≦5.5 |
| "H" Input Voltage2 | VIH2 | 0.7×Vcc | — | Vcc+0.3 | V | 1.8≦Vcc≦4.0 |
| "L" Output Voltage1 | VOL1 | 0 | — | 0.4 | V | IOL=2.1mA , 4.0≦Vcc≦5.5 |
| "L" Output Voltage2 | VOL2 | 0 | — | 0.2 | V | IOL=100μA , 1.8≦Vcc≦4.0 |
| "H" Output Voltage1 | VOH1 | 2.4 | — | Vcc | V | IOH=-0.4mA , 4.0≦Vcc≦5.5 |
| "H" Output Voltage2 | VOH2 | Vcc-0.2 | — | Vcc | V | IOH=-100μA , 1.8≦Vcc≦4.0 |
| Input Leakage Current | ILI | -1 | — | 1 | μA | VIN=0～Vcc |
| Output Leakage Current | ILO | -1 | — | 1 | μA | VOUT=0～Vcc , CS=0V |
| Operating Current | ICC1 | — | — | 3.0 | mA | fSK=2MHz , tE/W=5ms (WRITE) |
| | ICC2 | — | — | 1.5 | mA | fSK=2MHz (READ) |
| | ICC3 | — | — | 4.5 | mA | fSK=2MHz , tE/W=5ms (WRAL,ERAL) |
| | ICC4 | — | — | 1.5 | mA | fSK=500kHz , tE/W=5ms (WRITE) |
| | ICC5 | — | — | 0.5 | mA | fSK=500kHz (READ) |
| | ICC6 | — | — | 2 | mA | fSK=500kHz (WRAL,ERAL) |
| Standby Current | ISB | | — | 2 | μA | CS=0V , DO=OPEN |

○This product is not designed for protection against radioactive rays.

## ◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified Ta=-40～85℃, Vcc=1.8～5.5V)

| Parameter | Symbol | 1.8V≦Vcc≦2.5V | | | Unit | 2.5V≦Vcc≦5.5V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max | | Min. | Typ. | Max | |
| SK Clock Frequency | fSK | 0 | — | 500 | kHz | — | — | 2 | MHz |
| SK High Time | tSKH | 0.8 | — | — | μs | 230 | — | — | ns |
| SK Low Time | tSKL | 0.8 | — | — | μs | 230 | — | — | ns |
| CS Low Time | tCS | 1 | — | — | μs | 200 | — | — | ns |
| CS Setup Time | tCSS | 200 | — | — | ns | 50 | — | — | ns |
| DI Setup Time | tDIS | 100 | — | — | ns | 100 | — | — | ns |
| CS Hold Time | tCSH | 0 | — | — | ns | 0 | — | — | ns |
| DI Hold Time | tDIH | 100 | — | — | ns | 100 | — | — | ns |
| Data "1" Output Delay Time | tPD1 | — | — | 0.7 | μs | — | — | 200 | ns |
| Data "0" Output Delay Time | tPD0 | — | — | 0.7 | μs | — | — | 200 | ns |
| CS to Status Valid | tSV | — | — | 0.7 | μs | — | — | 150 | ns |
| CS to Output High-Z | tDF | — | — | 200 | ns | — | — | 150 | ns |
| Write Cycle time | tE/W | — | — | 5 | ms | — | — | 5 | ms |

## ◇ BLOCK DIAGRAM

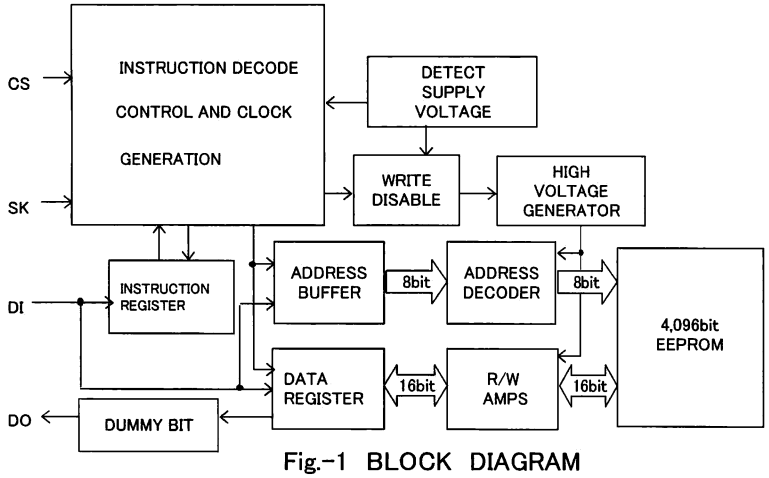


Fig.-1 BLOCK DIAGRAM

## ◇ PIN No. / PIN NAME

| PIN No. | PIN NAME | |
|---|---|---|
| 1 | CS | N.C. |
| 2 | SK | Vcc |
| 3 | DI | CS |
| 4 | DO | SK |
| 5 | GND | DI |
| 6 | N.C. | DO |
| 7 | N.C. | GND |
| 8 | Vcc | N.C. |
| PART NUMBER | BR93L66RF-W | BR93L66F-W |
| | BR93L66RFJ-W | BR93L66FJ-W |
| | BR93L66RFV-W | BR93L66FV-W |
| | BR93L66RFVT-W | BR93L66FVT-W |
| | BR93L66RFVM-W | |
| | BR93L66RFVJ-W | |

◇ NOTES FOR POWER SUPPLY

This IC has a POR (Power On Reset) circuit as mistake write countermeasure.
After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is "H" at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the following conditions.

1. Set CS = "L".
2. Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit operation.

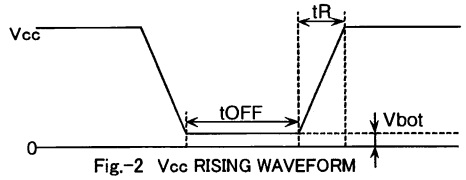

Fig.-2 Vcc RISING WAVEFORM

◇Recommended conditions of tR, tOFF, Vbot

| tR | tOFF | Vbot |
|---|---|---|
| Below 10ms | Above 10ms | Below 0.3V |
| Below 100ms | Above 10ms | Below 0.2V |

◇ CAUTIONS ON USE

(1) Absolute Maximum Ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(3) Heat design

In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

## ◇PHYSICAL DIMENSION

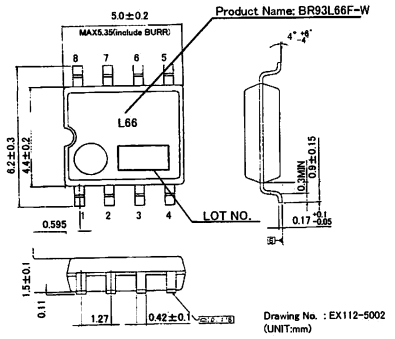


Fig4-(a) PHYSICAL DIMENSION
SOP8(BR93L46F-W)

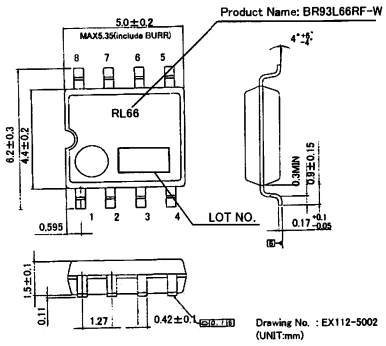


Fig4-(b) PHYSICAL DIMENSION
SOP8(BR93L46RF-W)

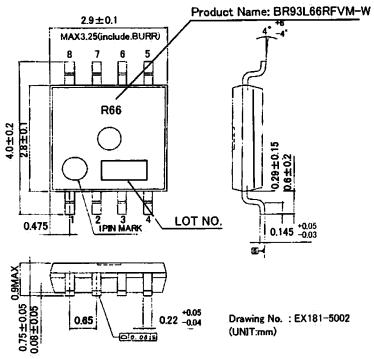


Fig4-(c) PHYSICAL DIMENSION
MSOP8(BR93L46RFVM-W)

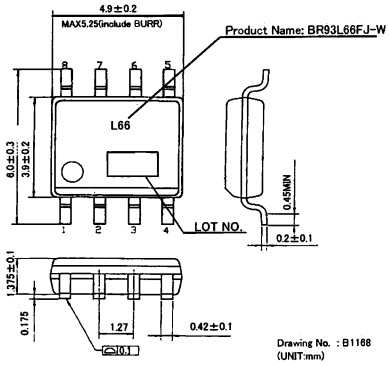


Fig4-(d) PHYSICAL DIMENSION
SOP-J8(BR93L66FJ-W)

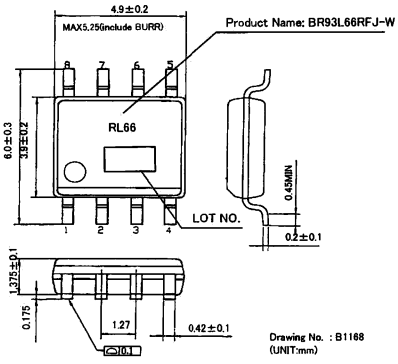


Fig4-(e) PHYSICAL DIMENSION
SOP-J8(BR93L66RFJ-W)

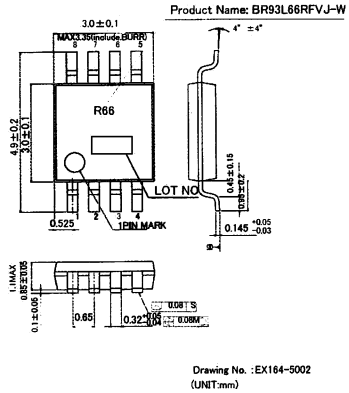


Fig4-(f) PHYSICAL DIMENSION
TSSOP-B8J(BR93L66RFVJ-W)

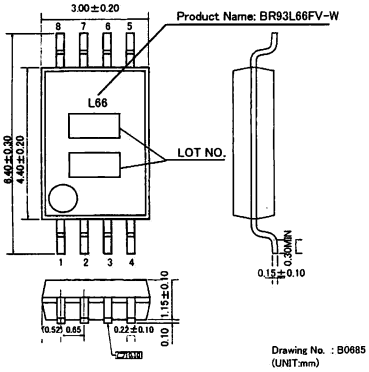


Fig4-(g) PHYSICAL DIMENSION
SSOP-B8(BR93L66FV-W)

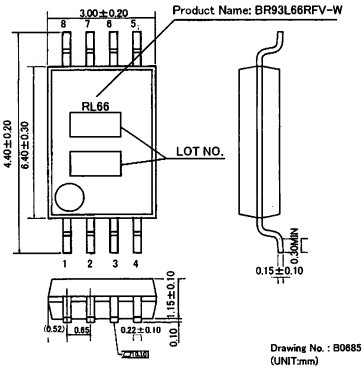


Fig4-(h) PHYSICAL DIMENSION
SSOP-B8(BR93L66RFV-W)

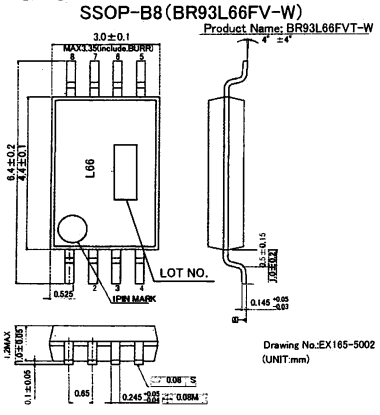


Fig4-(i) PHYSICAL DIMENSION
TSSOP-B8(BR93L66FVT-W)

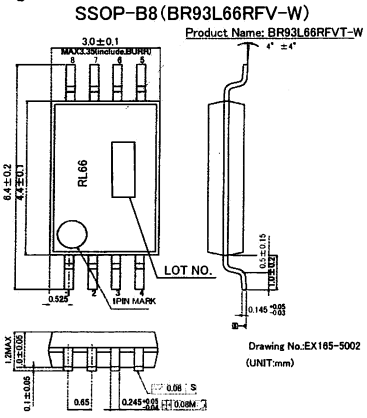


Fig4-(j) PHYSICAL DIMENSION
TSSOP-B8(BR93L66RFVT-W)

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