SONY

Zero-IF Tuner IC for Digital Satellite Broadcast

CXD2818ER

Description

The CXD2818ER is an IC developed for direct orthogonal detection of L band (1 to 2GHz) IF signals in a digital satellite broadcast reception tuner.
The CXD2818ER incorporates all the functions (RF gain control amplifier, oscillator circuit, wide-band phase shifter circuit and other RF circuits, a baseband LPF, baseband gain control amplifier, tuning PLL) required for a satellite broadcast tuner, and also an inductor and a varactor diode required for a tuning VCO. This makes it possible to mount it without tuning the RF circuits.
(Applications: digital satellite broadcast tuner)

Features

- ◆ Low power consumption: 430mW (Typ.) (Includes 30mW of current for controlling an external circuit)
- ◆ No need for an external inductor and a varactor diode
- ◆ 3.3V single power supply
- ◆ Reception frequency: 950MHz to 2150MHz
- ◆ High phase noise characteristic: –95dBc/Hz 100kHz offset (Typ.)
- ◆ Internal output for controlling an external attenuator
- ◆ Crystal output for a demodulation circuit
- ◆ Small package: 36-pin VQFN
- ◆ Enables to reduce power consumption in power saving mode when not used

Package

36-pin VQFN (Plastic)

Notes on Handling
A fine IC manufacturing process is used as this IC handles high-frequency signals.
As this IC is an ESD sensitive device, special handling precautions are required.

E09912C23

Absolute Maximum Ratings

◆ Supply voltage	AVcc, DVcc, OSCVcc, RFVcc	–0.3 to +3.6	V	(Ta = 25°C)
◆ Storage temperature	Tstg	–55 to +150	°C	

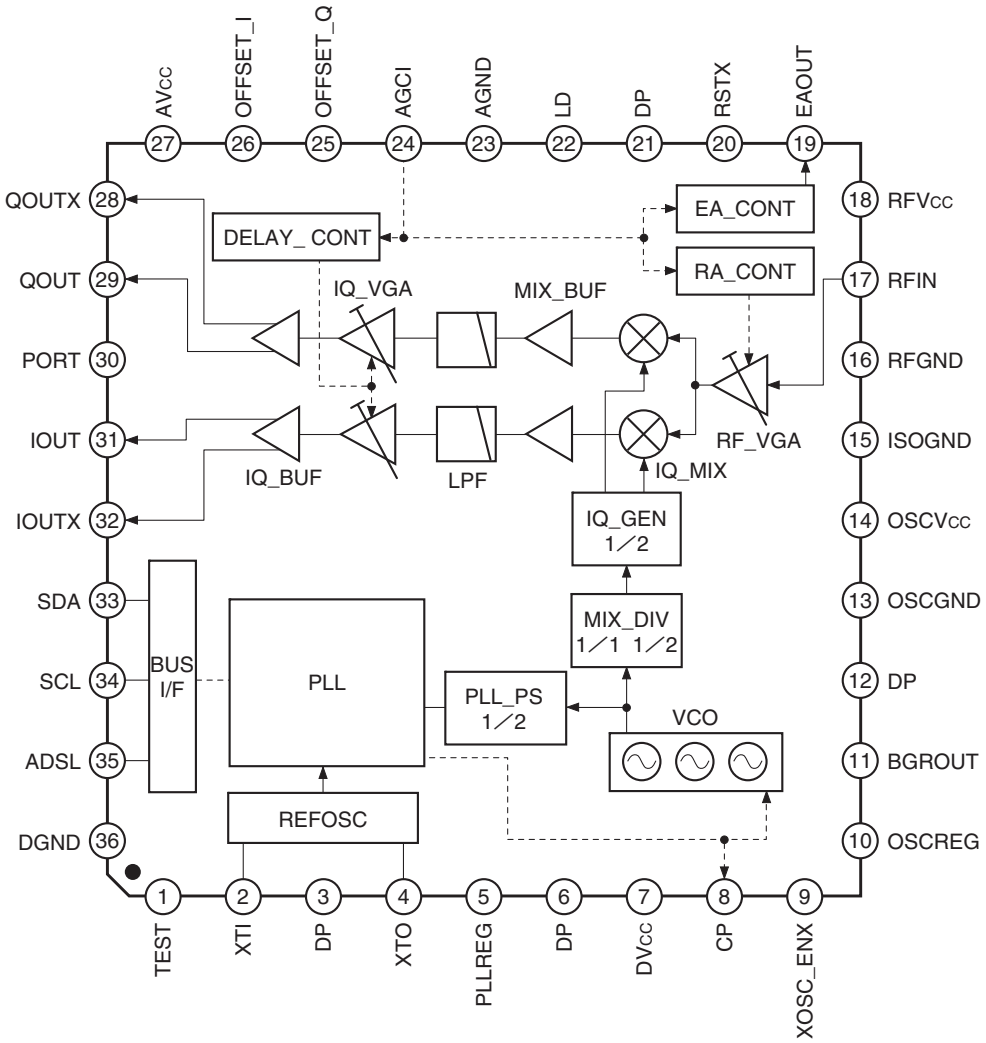
Operating Conditionsns

◆ Supply voltage	AVcc, DVcc, OSCVcc, RFVcc	3.1 to 3.5	V
◆ Operating temperature	Topr	–20 to +85	°C

Outline Specifications

Structure	Direct conversion
Reception frequency	950MHz to 2150MHz
Baseband bandwidth	5MHz to 36MHz
IQ output level	0.7Vp-p
Crystal oscillation frequency	16MHz, 27MHz
PLL comparison frequency	1MHz
PLL control	2-wire serial bus
Supply voltage	3.1V to 3.5V

Pin Configuration and Block Diagram



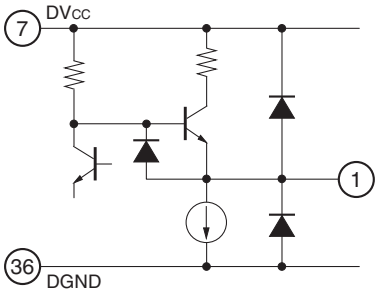
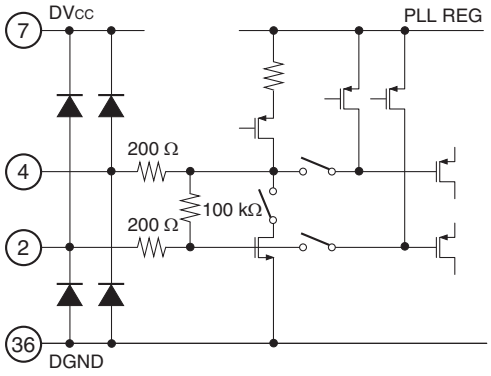
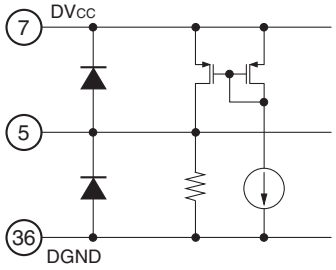
Description of Block Diagram

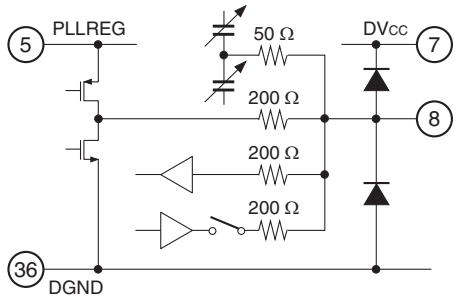
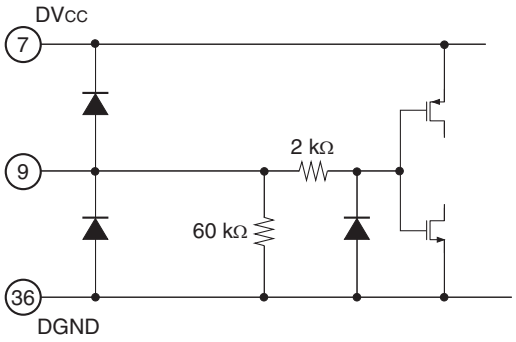
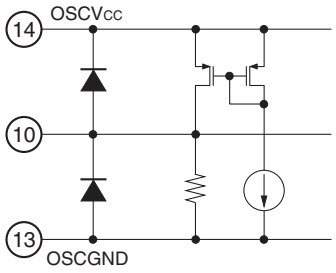
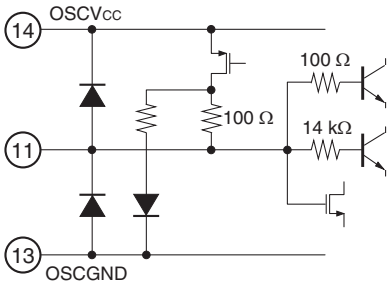
The block names shown in the block diagram above have the following functions.

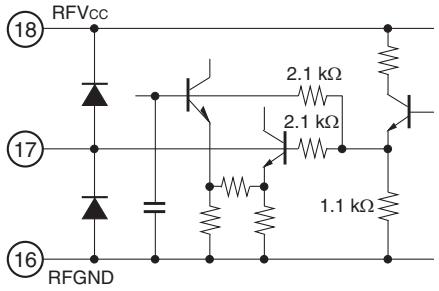
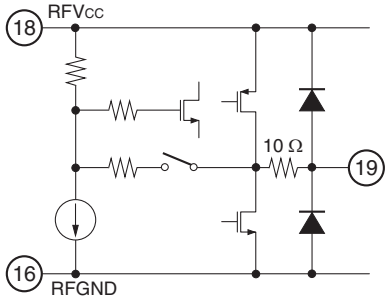
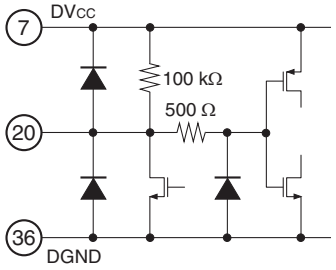
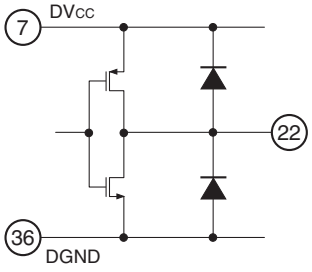
REFOSC	Crystal oscillation circuit for reference signal
BUS I/F	Interface block for 2-wire serial bus
PLL	Tuning PLL
PLL_PS	PLL fixed divider
VCO	VCO circuit for local signal
MIX_DIV	Divider for local signal
IQ_GEN	Divider and phase shifter for local signal
RF_VGA	Gain control amplifier for RF signal
IQ_MIX	Quadrature demodulator (Mixer circuit)
MIX_BUF	Buffer amplifier for mixer circuit
LPF	Low pass filter
IQ_VGA	Gain control amplifier for baseband signal
IQ_BUF	Buffer amplifier for baseband output
DELAY_CONT	Gain control amplifier control circuit for baseband
RA_CONT	RF gain control amplifier control circuit
EA_CONT	External attenuator control circuit

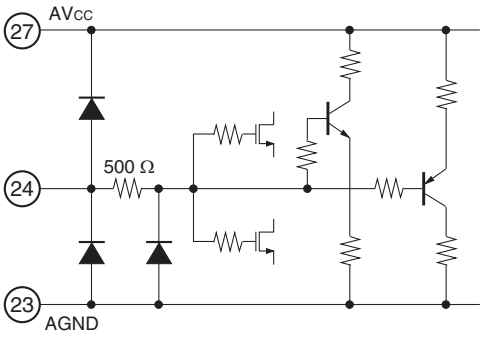
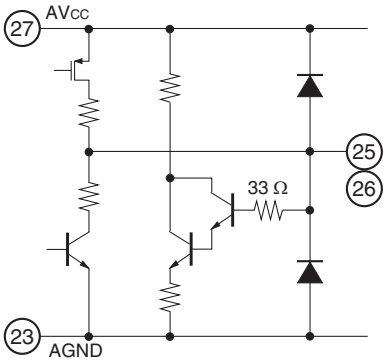
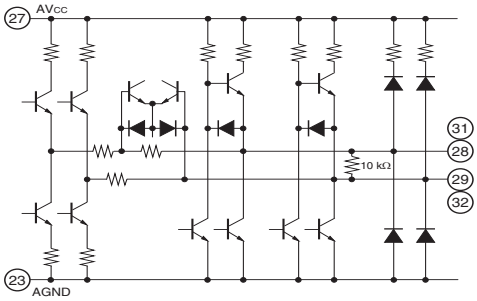
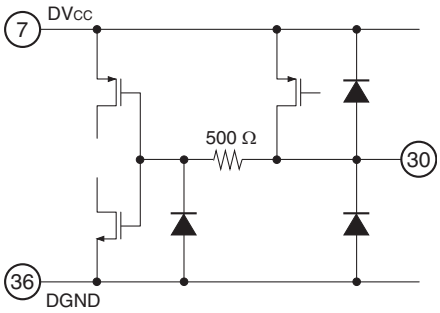
Pin Description and Input/Output Pin Equivalent Circuit

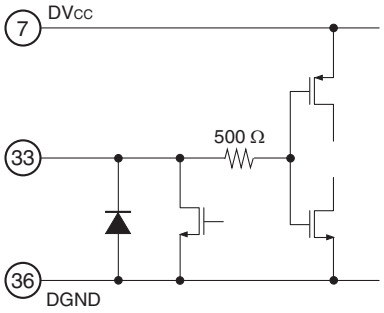
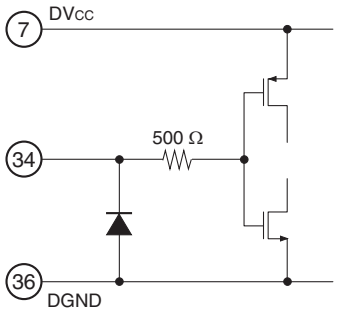
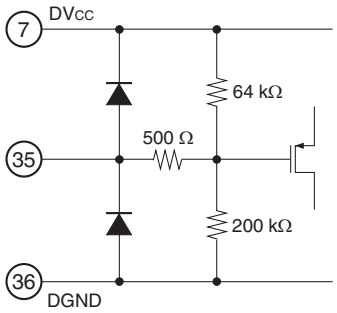
(Pin voltage shows typical DC voltage value when AGCI = 3.3V)

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
1	REFOUT	2.7		Reference signal output
2	XTI	0.9		Crystal oscillator connection for reference signal oscillation
4	XTO	0.7		
3	DP	0	Connected to the die pad (DP) inside the IC package. Connect to the GND pattern to take heat radiation effect.	
5	PLLREG	2.5		Reference voltage output for PLL circuit
6	DP	0	Connected to the die pad (DP) inside the IC package. Connect to the GND pattern to take heat radiation effect.	
7	DVCC	3.3		PLL power supply

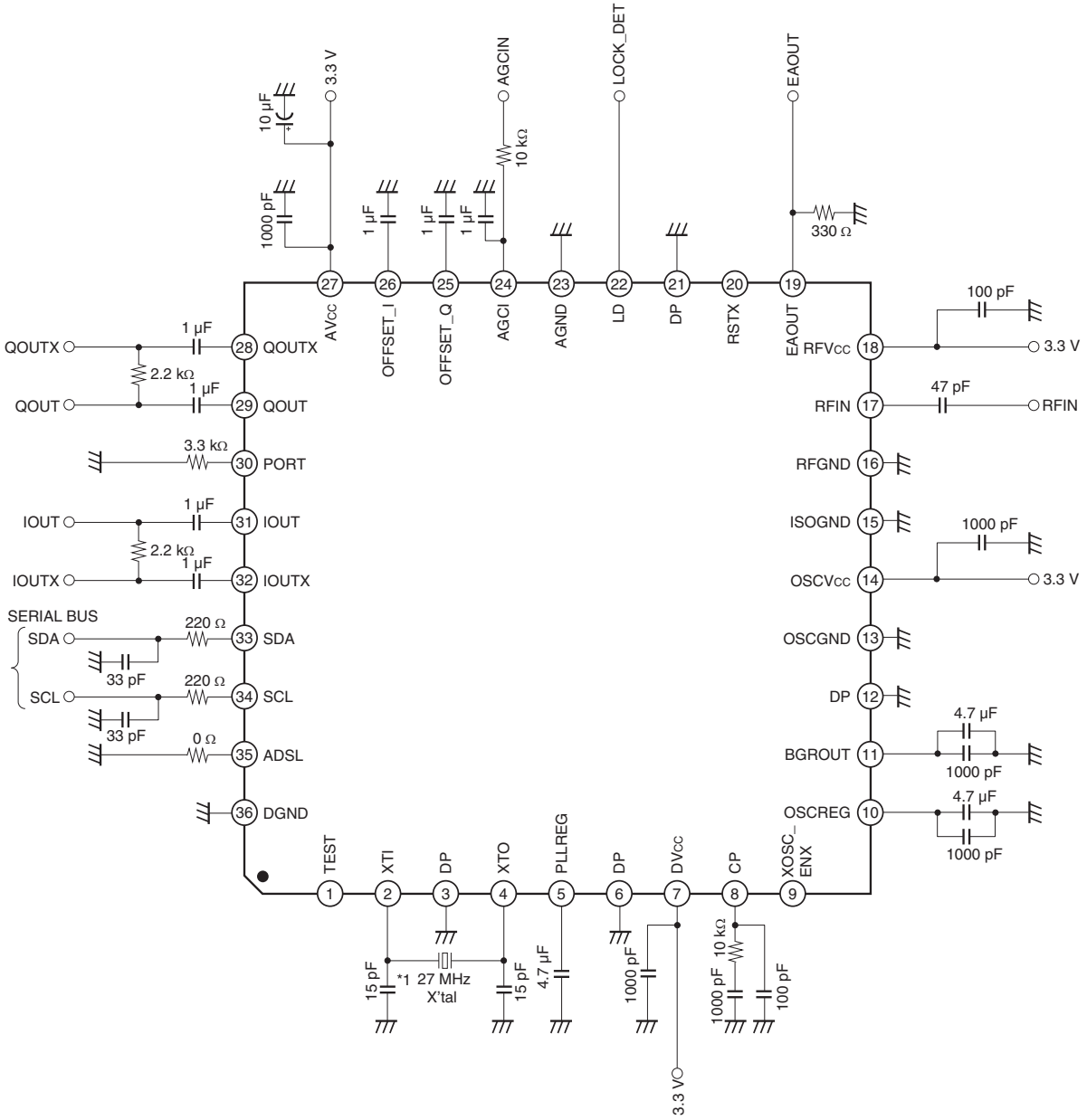
Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
8	CP	—		Charge pump output for tuning PLL
9	XOSC_ENX	0		Crystal oscillator control. Reception status when left open or Low. Crystal oscillator stops and internal analog circuit changes to power saving mode when High.
10	OSCREG	2.5		Regulator output for VCO oscillator
11	BGROUT	1.25		Reference voltage output
12	DP	0	Connected to the die pad (DP) inside the IC package. Connect to the GND pattern to take heat radiation effect.	
13	OSCGND	0		VCO circuit GND
14	OSCVCC	3.3		VCO circuit power supply
15	ISOGND	0		Isolation GND
16	RFGND	0		RF block GND

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
17	RFIN	1.4		RF input
18	RFVCC	3.3		RF block power supply
19	EAOUT	3.2		Gain control for external attenuator circuit
20	RSTX	3.3		Negative logic hard reset
21	DP	0	Connected to the die pad (DP) inside the IC package. Connect to the GND pattern to take heat radiation effect.	
22	LD	3.3		PLL lock status output
23	AGND	0		GND for mixer and baseband circuit

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
24	AGCI	3.3		AGC control voltage input
25	OFFSET_Q	2.2		Capacitor connection for DC offset correction circuit
26	OFFSET_I	2.2		
27	AVCC	3.3		Power supply for mixer and baseband circuit
28	QOUTX	1.4		Baseband signal output
29	QOUT	1.4		
31	IOUT	1.4		
32	IOUTX	1.4		
30	PORT	0		General-purpose port output

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
33	SDA	3.3		SDA input/output for serial bus
34	SCL	3.3		SCL input for serial bus
35	ADSL	2.5 (When open)		Serial bus slave address setting
36	DGND	0		PLL GND

Electrical Characteristics Measurement Circuit



*1 日本電波工業(株)製 NX2520SAを使用します。
本回路はP10～P12の電気的特性を測定するためのものです。

Electrical Characteristics

(See the Electrical Characteristics Measurement Circuit)

(Circuit voltage = 3.3V, AGCI = 3.3V, Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current	DICC		10	19	28	mA
	OSCICC		18	24	34	mA
	AICC		40	63	90	mA
	RFICC		18	26	36	mA
Input level range	RFDR	*1	–65		–15	dBm
IQ phase error	EPH	When RF input level is –40dBm *1	–5	0	+3	deg
IQ amplitude error	EAMP	When RF input level is –40dBm *1	–1	0	+1	dB
LPF cutoff frequency	FC	Attenuation at 26MHz when setting 23MHz Attenuation at 20.5MHz when setting 18MHz When RF input level is –40dBm *1	–27	–18	–10	dB
Noise figure	NF	fIF = 10MHz		9	13	dB
VCO phase noise	PN	fRF = 2150MHz 100kHz offset When RF input level is –40dBm *1		–92	–86	dBc/Hz
RF pin leakage	LO	RFIN pin 50Ω termination		–56	–50	dBm
RF input pin impedance	Rπ	fRF = 1550MHz		270		Ω
	Cπ			1.24		pF
IIP3	IIP3	When desired signal input level is –20dBm Calculates from IM3 measurement result by 2 signals, fLO + 5MHz and fLO + 7MHz		3		dBm
IIP2	IIP2	Calculates from IM2 by interferencesignal 1 of 1060MHz –20dBm and 2 1100MHz –20dBm when setting desired signal fRF = 2160MHz –20dBm		1		dBm

*1 Set AGCI voltage so that the baseband output becomes 0.7Vp-p between differential outputs.

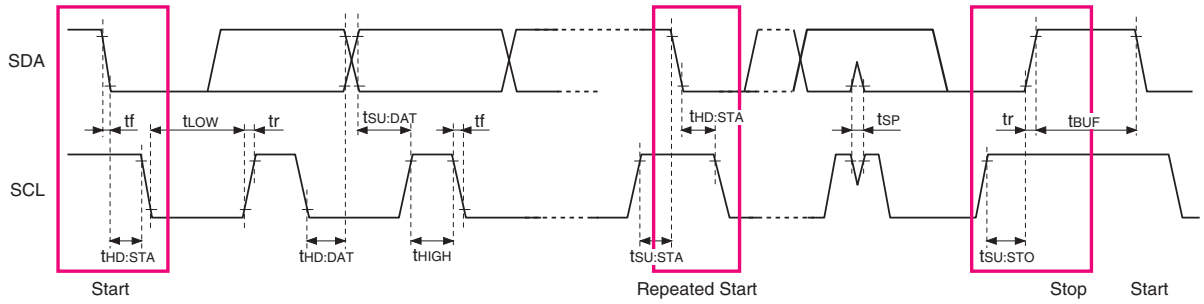
PLL Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Reference leak	REFL	fRF = 2150MHz Comparison frequency = 1MHz		–65	–50	dBc
SCL and SDA input						
High level input voltage	VIH		2.3		3.3	V
Low level input voltage	VIL		GND		1	V
High level input current	IIH	VIH = DV_{CC}		0	5	μA
Low level input current	IIL	VIL = GND	–30	–20		μA
REFOSC						
REFOUT output level	REFOUT	1kΩ loaded	0.5	0.6	0.75	Vp-p
PORT output voltage	PORTI	ON, Source current = 3mA	3.1	3.2	3.3	V
EAOUT output voltage	EAOUTI	Max. Gain, source current = 8mA	3.0	3.1	3.3	V

Register Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bus timing						
SCL clock frequency	f_{SCL}		0		400	kHz
Bus free time between “STOP” condition and “START” condition	t_{BUF}		1300			ns
Start - Hold time	$t_{HD:STA}$		600			ns
Low hold time	t_{LOW}		1300			ns
High hold time	t_{HIGH}		600			ns
Start - Setup time	$t_{SU:STA}$		600			ns
Data - Hold time	$t_{HD:DAT}$		0		900	ns
Data - Setup time	$t_{SU:DAT}$		100			ns
Rise time	tr				300	ns
Fall time	tf				300	ns
Stop - Setup time	$t_{SU:STO}$		600			ns
Spike pulse width	t_{SP}				50	ns
Capacitive load of bus line	Cb				400	pF

Bus Timing Chart

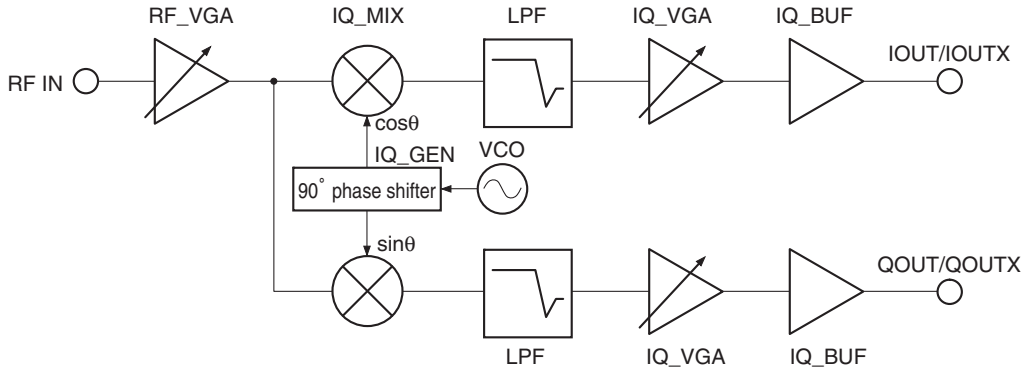


tr : Rise time
tf : Fall time
$t_{HD:STA}$: Start hold time
t_{LOW} : Low clock pulse width (Low hold time)
$t_{HD:DAT}$: Data hold time
$t_{SU:DAT}$: Data setup time
t_{HIGH} : High clock pulse width (High hold time)
$t_{SU:STA}$: Start setup time
t_{SP} : Spike pulse time
$t_{SU:STO}$: Stop setup time
t_{BUF} : Bus free time

Description of Operation

1. Analog Block

The CXD2818ER incorporates the RF gain control amplifier, quadrature mixer, low-pass filter and baseband gain control amplifier needed for satellite broadcast reception.



RF Gain Control Amplifier (RF_VGA)

The CXD2818ER's RF gain control amplifier has a continuous gain variable width of approximately 40dB and is a single signal input, so there is no need for an external balanced-unbalanced conversion component such as a balun.

The RF_VGA block has gradual BPF characteristics that enable switching of the center frequency. This effectively improves BS signal interference to the CS band caused by BS-IF signal attenuation at high frequencies.

The RF_VGA block filter must be set by the register according to the tuning frequency.

Quadrature Demodulator (IQ_MIX)

The mixer circuit uses a balanced type active mixer, and is configured to reduce local signal leakage and self-mixing.

LPF

The LPF incorporates an elliptic function filter with a trap to reduce the effects of second-adjacent interference. The cutoff frequency can be selected from 5/6/7/8/9/10/12/15/18/23/27/33/36MHz.

Baseband Gain Control Amplifier (IQ_VGA)

The IQ_VGA circuit has a gain variable range of approximately 35dB, and is composed of a gain control amplifier. The gain variation is controlled by the AGCI pin voltage, but both the IQ_VGA circuit and RF_VGA circuit variation relative to the AGCI voltage are controlled by an internal circuit to optimize the sensitivity and interference characteristics.

Output Buffer (IQ_BUF)

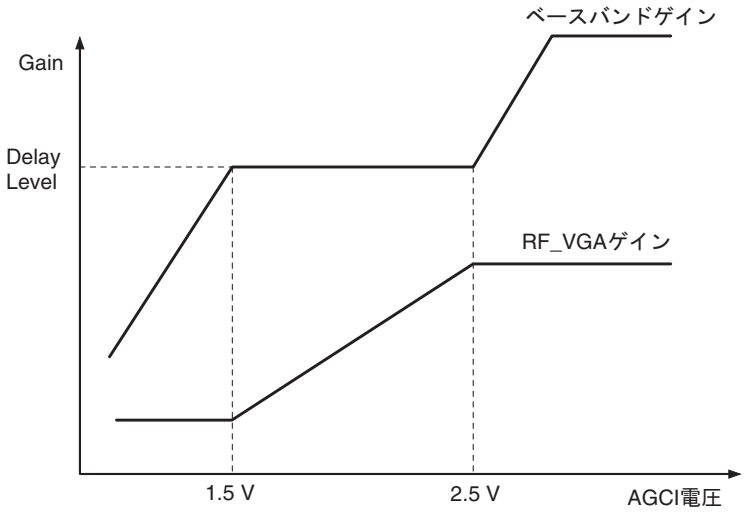
This output circuit outputs the baseband signal to a demodulator IC.
A load of 2kΩ can be connected between the differential outputs, or 1kΩ per side.
Therefore, the CXD2818ER can be used as a single output IC by using only one side of the differential outputs.

DC Offset Cancel Circuit

Direct conversion ICs handle signals up to near the DC frequency range, so there is the issue that normal output cannot be obtained due to the minute bias error caused by IC internal variance. This issue is known as DC offset.
This IC resolves the issue of DC offset by incorporating a DC feedback circuit.
The rectifier capacitor of the DC feedback circuit is connected to OFFSET_I and OFFSET_Q. Always connect a 1μF to 4.7μF capacitor.

2. AGC Control Block

The CXD2818ER incorporates an AGC control circuit that realizes the optimum gain characteristics by varying the gain relative to the external AGC control voltage (AGCI pin voltage) as shown in the figure below.



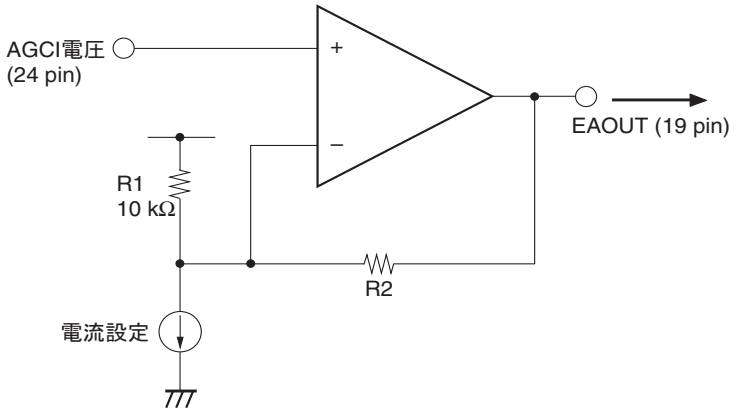
By providing the gain variation shown above, only the baseband block gain is varied during weak input (when the AGCI voltage is high), so the total NF does not worsen. This enables to improve the distortion characteristics by varying only the RF_VGA circuit gain over the AGCI voltage range of 2.5V to 1.5V.

The baseband gain (Delay Level) can be finely adjusted over the AGCI voltage range of 2.5V to 1.5V.

In addition, this IC also incorporates an external attenuator control output for when an external attenuator circuit composed of a PIN diode, etc. is connected. (EAOUT pin)
The EAOUT pin can output current of 8mA, and can directly connect a PIN diode, etc. The EAOUT pin variation relative to the AGC control voltage can also be set by the register.

3. EAOUT Pin Control Method

The equivalent circuit for the control circuit is a non-inverted type DC amplifier as shown in the figure below, and the output voltage characteristics relative to the AGCI pin voltage can be changed by the register settings.



Register Setting Method

Each bit of sub address 06h is set as shown below.

EA_GAIN

This changes the R2 resistance value in the equivalent circuit shown above. Increasing the R2 value increases the EAOUT pin variation relative to the AGC voltage.

EA_START

This changes the current value in the equivalent circuit shown above. This changes the voltage on the - input side of the operational amplifier, so the EAOUT variation start point relative to the AGC voltage changes. Increasing the EA_START current causes EAOUT pin variation to start at a lower AGC voltage.

Sub Addr	Register Name [:]	Bit	RW	Bit Position							
				7	6	5	4	3	2	1	0
06	EA_GAIN [2:0]	3	RW	0	0	1					
	EA_PS	1	RW				0				
	EA_START [2:0]	3	RW					1	0	1	
	RESERVE	1	RW								0

EA_ST Control

Bit3	Bit2	Bit1	Current [μA]
0	0	0	25
0	0	1	50
0	1	0	75
0	1	1	100
1	0	0	125
1	0	1	150
1	1	0	175
1	1	1	200

EA_GAIN (R2 Value) Control

Bit7	Bit6	Bit5	Resistance [Ω]
0	0	0	40k
0	0	1	35k
0	1	0	30k
0	1	1	25k
1	0	0	20k
1	0	1	15k
1	1	0	10k
1	1	1	5k

Output Control

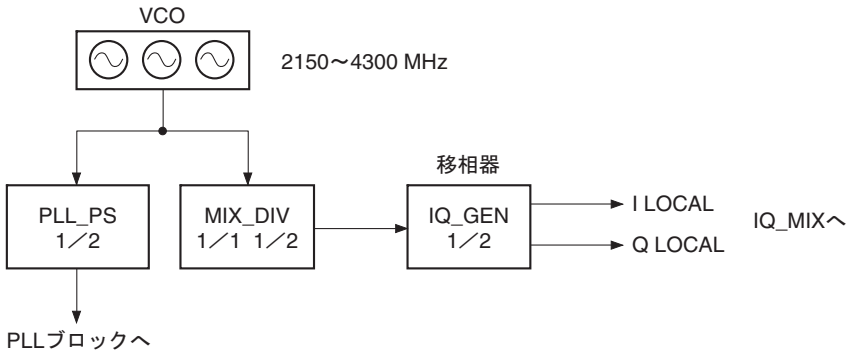
Bit4	Amp
0	ON
1	OFF

4. VCO PLL Block

The CXD2818ER incorporates three sets of VCO circuits (VCO_L/M/H), and these three VCO circuits together cover an oscillation frequency range of 2150MHz to 4300MHz.
Each VCO has sub band which switch its oscillation frequency, and the optimum band and sub band points are automatically selected according to the reception frequency.

In addition, the PLL block charge pump current is also automatically calculated to the optimum point according to the reception frequency.
These functions are collectively called PLL calibration, and are executed by setting “1” in bit 1 of sub address 02h by the serial bus.

The PLL becomes unlocked when PLL calibration is executed, which causes noise when executed during broadcast reception. Therefore, avoid executing PLL calibration when refreshing the registers after tuning.



The signal from the VCO is used as the local signal, and is passed through a fixed 1/2 frequency divider and then input to the PLL circuit.

In the path that uses the signal from the VCO as the local signal, the 2150MHz to 4300MHz signal from the VCO is 1/2 frequency divided, and a 90° phase difference signal is created and used as the local signal. However, the range covered by the VCO is insufficient to receive frequencies less than 1075MHz, so a fixed 1/2 frequency divider is further added to enable reception of the 950MHz to 2150MHz range.

PLL Calibration

The CXD2818ER requires 1MHz as an internal clock to execute PLL calibration. For this reason, the crystal oscillation frequency is set in a register and 1MHz is generated by an internal frequency divider, so the crystal oscillation frequency must be an integer multiple of 1MHz.

Sub address 0Ah FIN is the setting register. Use the CXD2818ER with 10h (16MHz) of the initial value or 1Bh (27MHz).

5. 2-wire Serial Bus Interface Block

Description

The internal registers of this IC are set via the 2-wire serial bus.

Registers that can be set via the bus have an 8-bit sub address, and this IC uses the sub addresses 00h to 2Ah. (See page 20 and onward for a detailed description of the registers.)
Continuous write and read is possible to registers with continuous sub addresses.
There is no limit to the number of words that can be continuously written or continuously read.
Write to read-only registers is ignored.

This serial bus can be set regardless of reference crystal operation. In addition, the operation speed is also independent of the crystal frequency.

Slave Address Selection

Four different slave addresses can be selected by the voltage applied to the ADSL pin to support mounting of multiple tuner ICs. Generate the voltage applied to the ADSL pin by dividing the DVCC voltage applied to the IC with a resistor.
WRITE mode that sets various data and READ mode that transmits the IC internal register data to the host side are switched by setting the LSB (R/W bit) of the address byte.

Slave Address

1	1	0	0	0	MA1	MA0	R/W

MA1 to MA0 : Portion that changes according to the ADSL pin voltage

R/W : WRITE mode and READ mode switching
R/W = 0: WRITE mode
R/W = 1: READ mode

Slave Address Switching by the ADSL Pin Voltage

ADSL pin voltage	MA1	MA0
0 to 0.33V	0	0
0.66 to 0.99V	0	1
1.32 to 1.98V	1	0
OPEN (2.5V)	Use prohibited	
2.97 to 3.3V	1	1

The ADSL pin voltage in the table above is the voltage when 3.3V is applied to the DVCC pin.

Write Procedure and Read Procedure

Write is performed in 1-byte units as follows.

Write slave address → Write desired sub address → Write register setting value

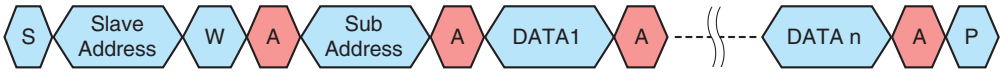
This procedure is also applied to continuous write mode that performs continuous write to consecutive sub addresses.

Read is also performed in 1-byte units as follows.

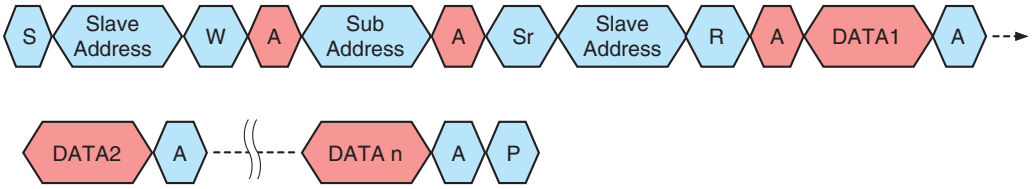
Write slave address → Write desired sub address → Repeated Start condition → Write slave address → Read data

The Repeated Start condition can be replaced by “Stop condition → Start condition” without problem.
This procedure is also applied to continuous read mode that performs continuous read from consecutive sub addresses.

Write Procedure



Read Procedure

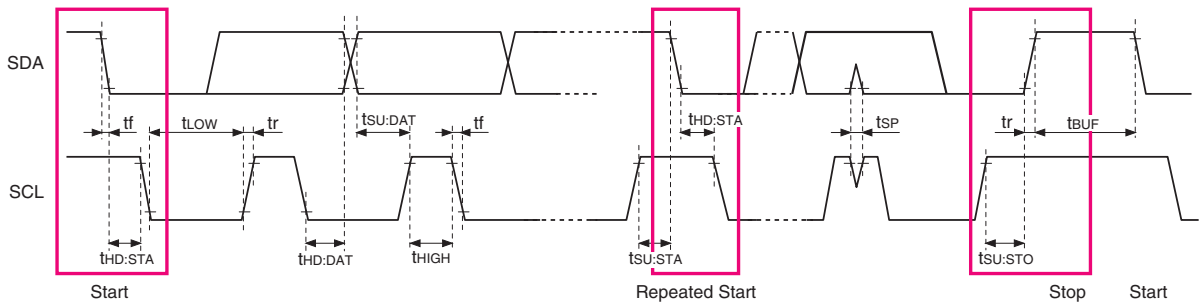


From Master to Slave
From Slave to Master

S : Start condition
Sr : Repeated start condition
P : Stop condition
A : Acknowledge
W : W/R Bit = "0" Write mode
R : W/R Bit = "1" Read mode

Description of SCL and SDA Signals during Bus Communication

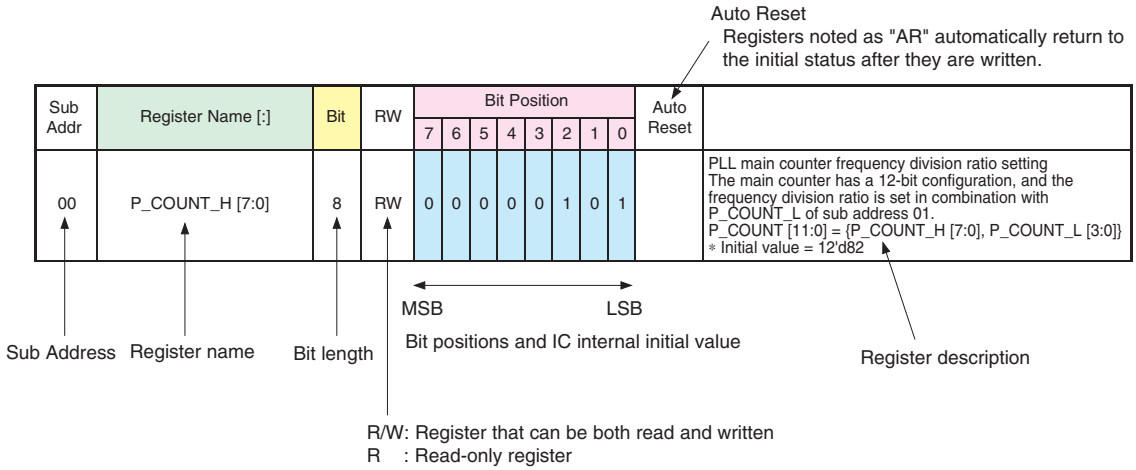
The Start condition, Stop condition and Repeated start condition signals are as shown in the figure below.
See the Electrical Specifications for the detailed timing.



Detailed Description of Registers

Register Map Notation Method

The register map is created in the following format.



Register Map

(The data noted for each register are the initial values for this IC.)

Sub Addr	Register Name [:]	Bit	RW	Bit Position 7	6	5	4	3	2	1	0	Auto Reset	
00	P_COUNT_H [7:0]	8	RW	0	0	0	0	0	1	0	1		PLL main counter frequency division ratio setting The main counter has a 12-bit configuration, and the frequency division ratio is set in combination with P_COUNT_L of sub address 01. P_COUNT [11:0] = {P_COUNT_H [7:0], P_COUNT_L [3:0]} The settings to the internal counters are executed when they are written to sub address 01h. * Initial value = 12'd82
01	P_COUNT_L [3:0]	4	RW	0	0	1	0						See P_COUNT_H.
	S_COUNT [3:0]	4	RW					0	1	1	0		PLL swallow counter frequency division ratio setting * Initial value = 4'd6
02	LPF_FREQ	1	RW	0									LPF cutoff frequency switching This register is valid only when LPF_FREQ_ENX (sub address 05h) = 0. 0: 23MHz 1: 18MHz * Initial value = 0 When also using other cutoff frequencies, always set LPF_FREQ_ENX = 1. When setting 18MHz or 23MHz, also set LPF_EXP (sub address 05h).
	RF_LOAD_SEL [2:0]	4	RW		1	0	0						RFVGA block tracking filter setting. This must be set according to the reception frequency. fRF < 1100MHz rfload = 000 1100 ≤ fRF < 1200MHz rfload = 010 1200 ≤ fRF < 1400MHz rfload = 100 1400 ≤ fRF < 1500MHz rfload = 101 1500 ≤ fRF < 1600MHz rfload = 110 1600 ≤ fRF MHz rfload = 111
	POR_MONI	1	RW					0					After this bit is set to 1'b1 when writing the tuning data, it automatically returns to the initial value 1'b0 when a reset is applied. This can be used to recognize reset generation by periodically monitoring this bit.
	IQ_GEN_ENX	1	RW						0				IQ_GEN block and MIX_DIV block enable (negative logic) 1: Disable * 0: Enable (Initial value)
	PLL_CAL_START	1	RW							0		AR	PLL calibration start bit. When “1” is set, the PLL_CAL sequence starts and the optimum VCO selection and CP current setting value are calculated. Always execute PLL calibration when changing the tuning data. 1: Calibration start; this bit automatically returns to “0” after calibration ends.
	PORT_EN	1	RW								0		General-purpose port control bit. The general-purpose port (Pin 30) is turned ON by setting this bit to “1”. 1: Enable (Output) * 0: Disable (Output stopped) (Initial value)
03	MIX_ENX	1	RW	0									IQ_MIXER block enable (negative logic) 1: Disable 0: Enable (Initial value)
	MIXBUF_ENX	1	RW		0								MIX_BUFFER block enable (negative logic) 1: Disable * 0: Enable (Initial value)
	IQVGA_ENX	1	RW			0							IQVGA and control circuit enable (negative logic) 1: Disable * 0: Enable (Initial value)
	IQBUF_ENX	1	RW				0						IQ_BUFFER control circuit enable (negative logic) (The IQ_BUFFER cannot be turned OFF.) 1: Disable * 0: Enable (Initial value)
	MIX_DIV_EN	1	RW					0					MIX_DIV circuit enable When MIX_DIV is enabled, the frequency division ratio between the VCO and the MIXER changes from 1/2 to 1/4. Set to “1” when receiving a frequency between 950MHz and 1075MHz. 1: Enable (1/2 frequency division) * 0: Disable (Through) (Initial value)
	PLL_PS_ENX	1	RW						0				PLL_PS (PLL 1/2 frequency divider) enable (negative logic) 1: Disable * 0: Enable (Initial value)
	DMPS_ENX	1	RW							0			Dual-modulus divider enable (negative logic) 1: Disable * 0: Enable (Initial value)
	AREG_ENX	1	RW								0		VCO regulator enable (negative logic) 1: Disable * 0: Enable (Initial value)

Sub Addr	Register Name [:]	Bit	RW	Bit Position 7	6	5	4	3	2	1	0	Auto Reset	
04	REG_DELAY_UPDN [1:0]	2	RW	0	0								This register changes the IQVGA block gain of delay level. 2'b00 = 0dB * Initial value 2'b01 = +3dB 2'b10 = –3dB 2'b11 = –6dB Increasing this gain setting value improves the interference characteristics, but worsens the S/N characteristics.
	TUNE_LPF_EN	1	RW			0							LPF cutoff frequency fine adjustment enable bit. When this is 1'b1, the LPF cutoff frequency can be finely adjusted by the TUNE_LPF [4:0] register. However, this function may not be available due to IC variance or other factors. (This function is not guaranteed.) 1: Enable (Addition executed) * 0: Disable (Initial value)
	TUNE_LPF [2:0]	3	RW				0	0	0				LPF cutoff frequency fine adjustment register. This is valid when TUNE_LPF_EN = 1. This register is 2's complement expression. 3'b011 = +3 (decimal) Maximum value 3'b010 = +2 (decimal) 3'b001 = +1 (decimal) * 3'b000 = 0 (decimal) (Initial value) 3'b111 = –1 (decimal) 3'b110 = –2 (decimal) 3'b101 = –3 (decimal) 3'b100 = –4 (decimal) Minimum value
	TUNE_RF [1:0]	2	RW							0	0		RF_VGA circuit gain adjustment register. (Operation is not guaranteed.) 2'b00 = 0dB (Initial value) 2'b01 = –1.5dB 2'b10 = +1.5dB 2'b11 = +3dB
05	LPF_FREQ_ENX	1	RW	1									LPF_FREQ register's negative logic enable. Set this register to “1” when setting a filter other than 18MHz or 23MHz. 1'b0 = LPF_FREQ (sub address 02h) valid 1'b1 = LPF_EXP setting valid Do not change when LPF_FREQ_ENX from “1” to “0” during operation.
	LPF_CONT [2:0]	3	RW		0	0	0						Reserved (not used)
	LPF_EXP [3:0]	4	RW					1	0	0	1		LPF cutoff frequency switching register. This is valid when LPF_FREQ_ENX = 1. When LPF_FREQ_ENX = 0, the LPF_FREQ (sub address 02h) setting (23/18MHz) is used. LPF_EXP cutoff frequency 0000: 5MHz 0001: 6MHz 0010: 7MHz 0011: 8MHz 0100: 9MHz 0101: 10MHz 0110: 12MHz 0111: 15MHz 1000: 18MHz 1001: 23MHz 1010: 27MHz 1011: 33MHz 1100: 36MHz
06	EA_GAIN [2:0]	3	RW	0	0	1							Control characteristics setting register for external ATT control output (EAOUT). When bit4 is “1”, the output is fixed High. Bits7 to 5 set the AGC gain. Bits3 to 1 set the start point.
	EA_PS	1	RW				0						
	EA_START [2:0]	3	RW					1	0	1			
	RESERVE	1	RW								0		
07	RA_GAIN [2:0]	3	RW	1	1	1							RFVGA block gain control characteristics setting register. When bit4 is “1”, the output is fixed High. Bits7 to 5 set the AGC gain. Bits3 to 1 set the start point.
	RA_PS	1	RW				0						
	RA_START [2:0]	3	RW					1	0	0			
	RESERVE	1	RW								0		
08	REF_SEL	1	RW	1									Test register
	LF_MODE	1	RW		1								Test register
	REFOUT_ENX	1	RW			0							REFOUT pin output enable (negative logic) register. An approximately 600mVp-p signal is output from the REFOUT pin at the same frequency as the crystal. 1: Disable * 0: Enable (Initial value)
	XOSC_SEL [4:0]	5	RW				1	1	1	1	1		Crystal oscillator drive current setting register, 1LSB = 25μA. The crystal oscillator is stopped by setting 5'b0_0000. This is set to the maximum value at power-on, so it should be reset to an appropriate value according to the crystal to be used. * Initial value = 5'b1_1111

Sub Addr	Register Name [:]	Bit	RW	Bit Position								Auto Reset	
				7	6	5	4	3	2	1	0		
09	FREQCTR_START	1	RW	0								AR	Test register
	FC_CLK_DIV_TEST [1:0]	2	RW		0	0							Test register
	RST_LCK_DTCT	1	RW				0					AR	Test register
	VCO_FC_CLK_TEST	1	RW					0					Test register
	VCO_RC_CLK_SEL	1	RW						0				Test register
	CLK_SRC_DIV_EN	1	RW							1			Logic clock signal enable bit * 1: Enable (Initial value) 0: Disable; related clocks are stopped.
	SOFT_RST	1	RW								0		SOFT RESET start bit. When set to “1”, all registers and internal logic return to the initial status. 1: Executes SOFT RESET (The registers and logic return to the initial status.) * 0: Ends SOFT RESET
0A	RESERVE [1:0]	2	RW	0	0								
	FIN [5:0]	6	RW			0	1	0	0	0	0		Reference clock frequency (crystal oscillation frequency) setting register * Initial value = '6b01_0000 (16MHz) This is used as the frequency division ratio for the system clock (1MHz) required by the logic block, and also to calculate the comparison frequency during PLL calibration.
0B	KBW [7:0]	8	RW	0	1	1	1	1	0	0	0		CP current automatic calculation parameter. Normally use the initial value. * Initial value = 8'd120
0C	KC1 [7:0]	8	RW	0	0	0	1	1	1	1	0		CP current automatic calculation parameter. Normally use the initial value. * Initial value = 8'd30
0D	KC0 [7:0]	8	RW	0	0	0	0	1	0	1	0		CP current automatic calculation parameter. Normally use the initial value. * Initial value = 8'd10
0E	CAL_FVCO_ENX	1	RW	0									Test register
	VCO_CAL_EN	1	RW		1								Test register
	CP_I_CAL_EN	1	RW			1							Test register
	CPDA_TARGET [4:0]	5	RW				0	1	1	1	1		Test register
0F	REF_R_H [7:0]	8	RW	0	0	0	0	0	1	0	0		PLL comparison frequency setting register. The value is set in 10 bits at sub addresses 0Fh and 10h. REF_R = {REF_R_H [7:0], REF_R_L [1:0]} * Set to 10'd16 when using a 16MHz crystal, or to 10'd27 when using a 27MHz crystal.
10	REF_R_L [1:0]	2	RW	0	0								See REF_R_H.
	RESERVE	1	RW			0							
	CPDA_RSEL [4:0]	5	RW				0	1	1	1	1		Test register
11	LCK_DTCT_MONI_SEL [3:0]	4	RW	0	0	0	0						Register for switching the output to the LD pin. * 4'b0000: Output OFF (Initial value) 4'b0001: LOCK_DET output Others are for test settings.
	LCK_DTCT_CYCLE [1:0]	2	RW					0	0				Test register
	UNLCK_DTCT_CYCLE [1:0]	2	RW							0	0		Test register
12	RESERVE [3:0]	4	RW	0	0	0	0						
	VCO_CAL_ERR	1	R					0					This bit goes to “1” when band selection could not be performed correctly during VCO calibration.
	LCK_DTCT	1	R						0				Lock Detect signal output. This bit goes to “1” when locked properly.
	ALD_REG	1	RW							0			Test register
	SEL_ALD_REG	1	RW								0		Test register
13	FVCO_H [7:0]	8	RW	0	1	0	1	0	0	1	0		Test register
14	FVCO_L [4:0]	5	RW	0	1	1	0	0					Test register
	RESERVE [2:0]	3	RW						0	0	0		
15	CP_I [7:0]	8	RW	0	0	0	0	0	0	0	0		Charge pump current monitor register, 1LSB = 10μA This register indicates the automatic calculation results.
16	VCO_MUX_EN	1	RW	1									Test register
	VCO_BUF_H_EN	1	RW		1								Test register
	VCO_BUF_M_EN	1	RW			0							Test register
	VCO_BUF_L_EN	1	RW				0						Test register
	RESERVE	1	RW					0					
	VCO_H_EN	1	RW						1				Test register
	VCO_M_EN	1	RW							0			Test register
	VCO_L_EN	1	RW								0		Test register
17	RESERVE [2:0]	3	RW	0	0	0							
	ADJ_VCO_RSW_EN	1	RW				0						Test register
	REG_VCO_RSW [3:0]	4	RW					1	0	0	0		Test register

Sub Addr	Register Name [:]	Bit	RW	Bit Position 7	6	5	4	3	2	1	0	Auto Reset	
18	DIV_BIAS [1:0]	2	RW	0	0								IQ phase error adjustment register. The initial value is 2'b00, but set to 2'b01 for use.
	RESERVE	1	RW			0							
	VCO_CSW [4:0]	5	RW				0	0	0	0	0		Test register
19	RESERVE	1	RW	0									
	IREF_EN	1	RW		1								PLL block and crystal oscillator circuit reference current source enable. The crystal oscillator circuit is stopped by setting this to disable. * 1: Enable 0: Disable
	ECL2CMOS_EN	1	RW			1							DMPS block ECL2CMOS buffer enable * 1: Enable 0: Disable
	RC_CLK_N_BUF_EN	1	RW				0						Test register
	RESERVE	1	RW					0					
	CLK1M_MASTER_EN	1	RW						0				Test register
	AD_CLK_SEL	1	RW							0			Test register
	AD_CLK_EN	1	RW								0		Test register
1A	FREQ_CTR_H [7:0]	8	R	0	0	0	0	0	0	0	0		Test register
1B	FREQ_CTR_L [4:0]	5	R	0	0	0	0	0					Test register
	RESERVE [2:0]	3	RW						0	0	0		
1C	RESERVE [1:0]	2	RW	0	0								
	COMP_OUT	1	R			0							Test register
	CP_EN	1	RW				1						Test register
	CPDA_REF_EN	1	RW					1					Test register
	CPDA_OUT_EN	1	RW						0				Test register
	CP_AMP_EN	1	RW							1			Test register
	COMP_EN	1	RW								0		Test register
1D	RESERVE [3:0]	4	RW	0	0	0	0						
	PFD_EN	1	RW					1					Test register
	PFD_TUP	1	RW						0				Test register
	PFD_TDN	1	RW							0			Test register
	PFD_CPP	1	RW								1		Test register
1E	TEST_SEL [7:0]	8	RW	0	0	0	0	0	0	0	0		Test register
1F	VER [2:0]	3	R	1	0	1							IC internal chip version indication. 3'b101 CXD2818ER 3'b100 CXA3775ER
	CHIP_TYPE [2:0]	3	R				0	0	0				Test register
	SLAVE_ADD [1:0]	2	R							0	0		Test register
20	RESERVE [1:0]	2	RW	0	0								
	RESERVE [1:0]	2	R			0	0						
	BIAS165_ENX	1	RW					0					Analog block reference voltage enable (negative logic) 1: Disable * 0: Enable (Initial value)
	RESERVE [2:0]	3	RW						0	0	0		
21	RESERVE [1:0]	2	RW	0	0								
	ADJ_LPF_EN	1	RW			0							Test register
	REG_ADJ_LPF [2:0]	3	RW				0	1	1				Test register The initial value varies for each IC.
	RESERVE [1:0]	2	RW							0	0		
22	GIQ_CONT [3:0]	4	R	1	1	0	0						Test register The initial value varies for each IC.
	ADJ_GIQ_EN	1	RW					0					Test register
	REG_ADJ_GIQ [2:0]	3	RW						0	0	0		Test register The initial value varies for each IC.
23	TEST_BB [3:0]	4	RW	0	0	0	0						Reserved (not used)
	XOSC_ENX	1	R					0					External input signal XOSC_ENX monitoring register
	RFVGA_ENX	1	RW						0				RFVGA block disable register 1'b0 ⇒ RFVGA ON (normal reception mode) 1'b1 ⇒ RFVGA OFF (power saving mode) This register does not accept XOSC_ENX control. (The RFVGA block is not subject to entire power saving.)
	PS_ALL_EN	1	RW							0			Entire power saving register This performs the same function as the external pin XOSC_ENX. 1'b0 ⇒ Normal reception mode 1'b1 ⇒ Power saving mode
	PS_PTL_EN	1	RW								0		Register for limiting the XOSC_ENX and PS_ALL_EN control subject range to only IREF_EN 1'b0 ⇒ Analog block also disabled (Initial value) 1'b1 ⇒ IREF_EN only controlled

Sub Addr	Register Name [:]	Bit	RW	Bit Position								Auto Reset	
				7	6	5	4	3	2	1	0		
24	RESERVE	1	RW	0									
	RESERVE [2:0]	3	R		0	0	0						
	RESERVE	1	RW					0					
	DELAY_DECODER [2:0]	3	R						0	0	1		Test register
25	RESERVE [3:0]	4	RW	0	0	0	0						
	MIXBUF_TEST_EN	1	RW					0					Test register
	LD_ENX	1	RW						0				Test register
	RESERVE	1	RW							0			
	TEST_IN_EN	1	RW								0		Test register
26	RF_SW [1:0]	2	RW	0	0								Reserved (not used)
	LPF_SW [5:0]	6	RW			0	0	0	0	0	0		Reserved (not used)
27	LPF_FREQ_DEC [4:0]	5	R	1	0	0	0	0					Test register The initial value varies for each IC.
	LPF_TRIM [2:0]	3	R						0	0	1		Test register The initial value varies for each IC.
28	LPF_TEST_EN	1	RW	0									Test register
	RESERVE [1:0]	2	RW		0	0							
	LPF_TEST [4:0]	5	RW			0	0	1	0	0			Test register
29	RESERVE [4:0]	5	RW	0	0	0	0	0					
	REFOUT_DIV [2:0]	3	R						0	0	0		Reserved (not used)
2A	PIN_BIAS [1:0]	2	RW	0	0								Test register
	PIN_GAIN [4:0]	5	RW			0	0	0	0	0			Test register
	PIN_COMP_EN	1	RW								0		Test register

Note) Rewriting registers noted as test registers or RESERVE may result in abnormal operation, so use the initial values or write the values described in the specifications.

In addition, the register contents change according to the reception status and other factors, so the register contents may not be as described in the specifications.

Main Counter and Swallow Counter Settings

The VCO tuning frequency is obtained by the following formulas.

RF = fosc/4 = 1/2 × fref × (16P + S) (950 ≤ RF < 1075MHz) MIX_DIV_EN = 1'b1
RF = fosc/2 = fref × (16P + S) (1075 ≤ RF < 2150MHz) MIX_DIV_EN = 1'b0
(Related register)

RF: Tuning frequency
fosc: Local oscillator circuit frequency
fref: Comparison frequency

P: Main counter frequency division ratio
S: Swallow counter frequency division ratio

The variable frequency division ranges of M and S are as follows, and are set as binary.
$S < P \leq 4095$
$0 < S \leq 15$

Initial Settings

The following initial settings must be made after power-on to operate the CXD2818ER.

(1) AGC Control Characteristics Setting

Sub address 06h must be set when controlling an external attenuator circuit. See page 15 and page 21.

(2) Reference Signal Setting and REFOUT Pin Setting

At power-on a clock signal is output from the REFOUT pin, so the REFOUT_ENX register must be set to “1” when this clock signal is not used.
The XOSC_SEL register sets the crystal oscillator drive current.
The maximum value is set at power-on, but this may cause undesired spurious, so using the smallest possible value is recommended.
However, note that when this value is too small, the phase noise may worsen or oscillation may stop, so be sure to check operation with the crystal to be used when setting the value.
FIN is used to generate the internal system clock, so always set FIN.

Sub Addr	Register Name [:]	Bit	RW	Bit Position								Auto Reset	
				7	6	5	4	3	2	1	0		
08	REF_SEL	1	RW	1									Test register
	LF_MODE	1	RW		1								Test register
	RESERVE	1	RW			0							REFOUT pin output enable (negative logic) register. An approximately 600 mVp-p signal is output from the REFOUT pin at the same frequency as the crystal. 1: Disable * 0: Enable (Initial value)
	XOSC_SEL [4:0]	5	RW				1	1	1	1	1		Crystal oscillator drive current setting register, 1LSB = 25 µA. The crystal oscillator is stopped by setting 5'b0_0000. * Initial value = 5'b1_1111
0A	RESERVE [1:0]	2	RW	0	0								
	FIN [5:0]	6	RW			0	1	0	0	0	0		Reference clock frequency (crystal oscillation frequency) setting register. *Initial value = '6b01_0000 (16 MHz) This is used as the frequency division ratio for the system clock (1 MHz) required by the logic block, and also to calculate the comparison frequency during PLL calibration.

(3) Reference Counter (Comparison Frequency) Setting

The initial setting is for a 16MHz reference crystal and a comparison frequency of 1MHz.

Sub Addr	Register Name [:]	Bit	RW	Bit Position								Auto Reset	
				7	6	5	4	3	2	1	0		
0F	REF_R_H [7:0]	8	RW	0	0	0	0	0	1	0	0		REF_R = {REF_R_H [7:0], REF_R_L [1:0]} REF_DIV frequency division ratio ∗ Use the CXD2818ER with the initial value = 10'd16 or 10'd27
10	REF_R_L [1:0]	2	RW	0	0								See REF_R_H.

Power Saving Mode Setting

CXD2818ER has the power saving mode for reducing power consumption in the standby mode.
Set the registers shown in white areas of the following table to set the power saving mode.
The following settings result in power consumption of approximately 150mW.

Register Setting for Power Saving Mode

Sub Addr	Register Name [:]	Bit	RW	Bit Position							
				7	6	5	4	3	2	1	0
02	LPF_FREQ	1	RW	*							
	RF_LOAD_SEL [2:0]	3	RW		*	*	*				
	POR_MONI	1	RW					1			
	IQ_GEN_ENX	1	RW						1		
	PLL_CAL_START	1	RW							0	
	PORT_EN	1	RW								*
03	MIX_ENX	1	RW	1							
	MIXBUF_ENX	1	RW		1						
	IQVGA_ENX	1	RW			1					
	IQBUF_ENX	1	RW				1				
	MIX_DIV_EN	1	RW					*			
	PLL_PS_ENX	1	RW						1		
	DMPS_ENX	1	RW							1	
	AREG_ENX	1	RW								1
19	RESERVE	1	RW	0							
	IREF_EN	1	RW		0						
	ECL2CMOS_EN	1	RW			0					
	RC_CLK_N_BUF_EN	1	RW				0				
	RESERVE	1	RW					0			
	CLK1M_MASTER_EN	1	RW						0		
	AD_CLK_SEL	1	RW							0	
	AD_CLK_EN	1	RW								0
20	RESERVE [1:0]	2	RW	0	0						
	RESERVE [1:0]	2	R			0	0				
	BIAS165_ENX	1	RW					1			
	RESERVE [2:0]	3	RW						0	0	0

The marks * indicate arbitrary values.

Make sure to set “0” for the register PLL_CAL_START when setting and canceling the power saving mode.
Perform the tuning operation after return from the power saving status.

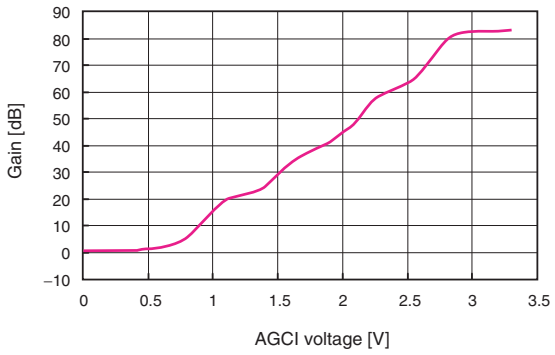
Entire Power Saving Mode Setting

A register that can set the internal circuits to power saving settings at once has been added to the CXD2818ER. The internal circuits including the crystal oscillator are set to power saving mode by setting PS_ALL_EN (sub address 23h Bit1) to 1'b1.
In this case, clock supply to the outside of the IC also stops, so care should be taken when supplying the clock to a demodulator or other IC.
In addition, this same setting can also be made by setting external Pin 9 to High.
To stop only the crystal, set sub address 23h Bit0 to 1'b1. This stops only the crystal regardless of whether control is performed from the external pin or from PS_ALL_EN.

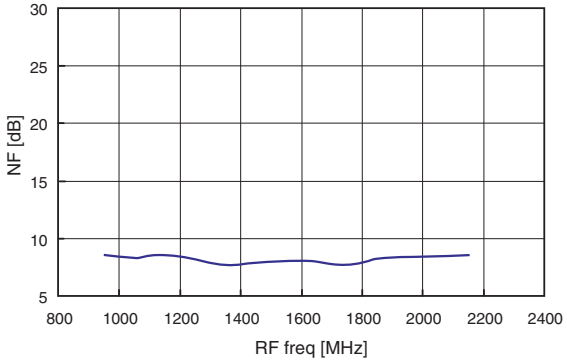
Example of Representative Characteristics

The following data is representative characteristics measured by the electrical characteristic measurement circuit on page 9.
Unless otherwise specified, the data is obtained by the measurement under the condition that Ta = 25°C, V_{CC} = 3.3V, reception status at 1318MHz, input level at –40dBm (SG display), output level at 0.7Vp-p (between differential outputs).

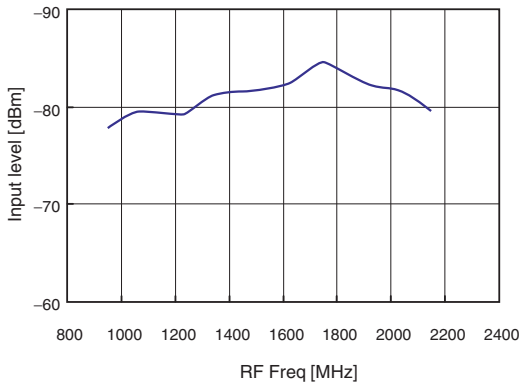
AGC control characteristic



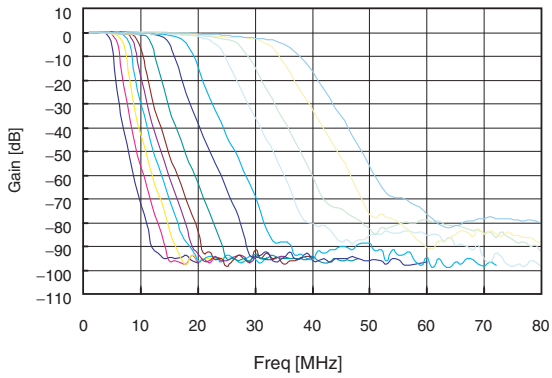
NF (Full Gain)



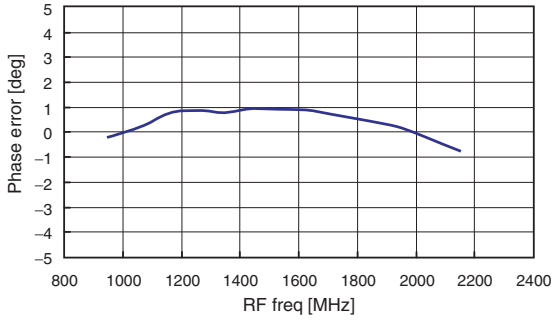
Input sensitivity



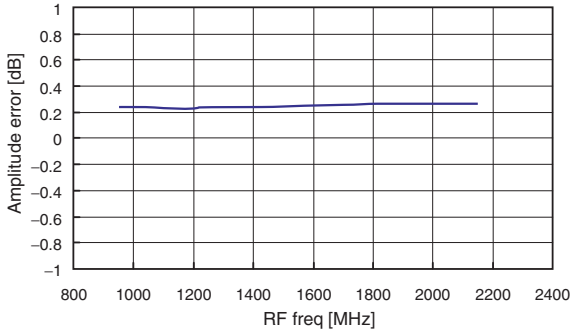
Baseband pass characteristics



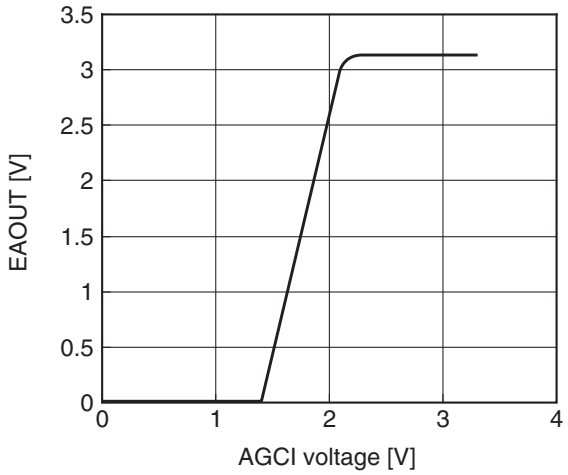
Phase Error



Amplitude Error

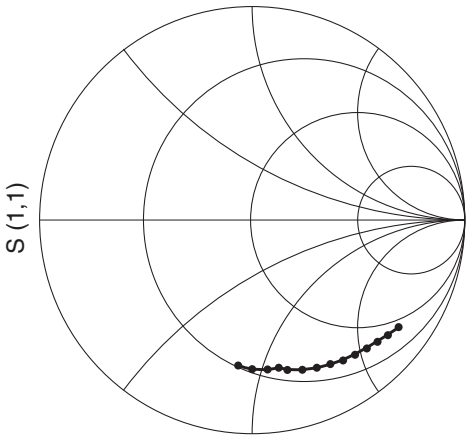


EAOUT control characteristic



(EA_GAIN = d'1, EA_START = d'5)

RFIN pin input impedance



Freq (900.0 MHz to 2.200 GHz)

Register Setting for Electrical Characteristic Measurement

(1318MHz reception setting, * = Don't Care, and crosshatched area needs to be changed according to reception frequency.)

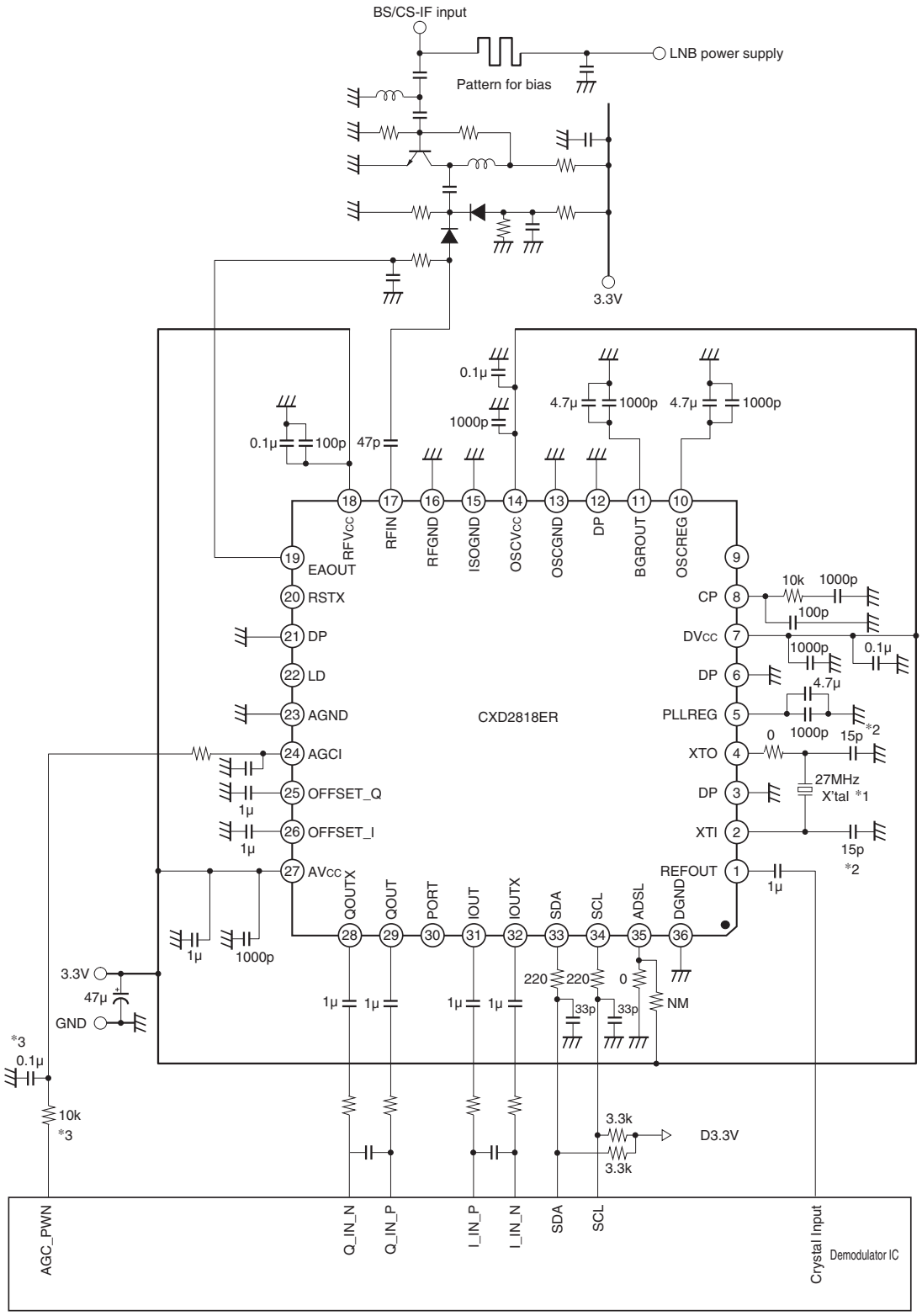
Sub Addr	Register Name [:]	RW	Bit Position							
			7	6	5	4	3	2	1	0
00	P_COUNT_H [7:0]	RW	0	0	0	0	0	1	0	1
01	P_COUNT_L [3:0]	RW	0	0	1	0				
	S_COUNT [3:0]	RW					0	1	1	0
02	LPF_FREQ	RW	0							
	RF_LOAD_SEL [2:0]	RW		1	0	0				
	POR_MONI	RW					1			
	IQ_GEN_ENX	RW						0		
	PLL_CAL_START	RW							1	
	PORT_EN	RW								1
03	MIX_ENX	RW	0							
	MIXBUF_ENX	RW		0						
	IQVGA_ENX	RW			0					
	IQBUF_ENX	RW				0				
	MIX_DIV_EN	RW					0			
	PLL_PS_ENX	RW						0		
	DMPS_ENX	RW							0	
	AREG_ENX	RW								0
04	REG_DELAY_UPDN [1:0]	RW	0	0						
	TUNE_LPF_EN	RW			0					
	TUNE_LPF [2:0]	RW				0	0	0		
	TUNE_RF [1:0]	RW							0	0
05	LPF_FREQ_ENX	RW	1							
	LPF_CONT [2:0]	RW		0	0	0				
	LPF_EXP [3:0]	RW					1	0	0	1
06	EA_GAIN [2:0]	RW	0	0	1					
	EA_PS	RW				0				
	EA_START [2:0]	RW					1	0	1	
	RESERVE	RW								0
07	RA_GAIN [2:0]	RW	1	1	1					
	RA_PS	RW				0				
	RA_START [2:0]	RW					1	0	0	
	RESERVE	RW								0
08	REF_SEL	RW	1							
	LF_MODE	RW		1						
	REFOUT_ENX	RW			0					
	XOSC_SEL [4:0]	RW				0	0	1	0	0

Sub Addr	Register Name [:]	RW	Bit Position							
			7	6	5	4	3	2	1	0
09	FREQCTR_START	RW	0							
	FC_CLK_DIV_TEST [1:0]	RW		0	0					
	RST_LCK_DTCT	RW				0				
	VCO_FC_CLK_TEST	RW					0			
	VCO_RC_CLK_SEL	RW						0		
	CLK_SRC_DIV_EN	RW							1	
	SOFT_RST	RW								0
0A	RESERVE [1:0]	RW	0	0						
	FIN [5:0]	RW			0	1	1	0	1	1
0B	KBW [7:0]	RW	0	1	1	1	1	0	0	0
0C	KC1 [7:0]	RW	0	0	0	1	1	1	1	0
0D	KC0 [7:0]	RW	0	0	0	0	1	0	1	0
0E	CAL_FVCO_ENX	RW	0							
	VCO_CAL_EN	RW		1						
	CP_I_CAL_EN	RW			1					
	CPDA_TARGET [4:0]	RW				0	1	1	1	1
0F	REF_R_H [7:0]	RW	0	0	0	0	0	1	1	0
10	REF_R_L [1:0]	RW	1	1						
	RESERVE	RW			0					
	CPDA_RSEL [4:0]	RW				0	1	1	1	1
11	LCK_DTCT_MONI_SEL [3:0]	RW	0	0	0	0				
	LCK_DTCT_CYCLE [1:0]	RW					0	0		
	UNLCK_DTCT_CYCLE [1:0]	RW							0	0
12	RESERVE [3:0]	RW	0	0	0	0				
	VCO_CAL_ERR	R					*			
	LCK_DTCT	R						*		
	ALD_REG	RW							0	
	SEL_ALD_REG	RW								0
13	FVCO_H [7:0]	RW	0	1	0	1	0	0	1	0
14	FVCO_L [4:0]	RW	0	1	1	0	0			
	RESERVE [2:0]	RW						0	0	0
15	CP_I [7:0]	RW	0	0	0	0	0	0	0	0
16	VCO_MUX_EN	RW	1							
	VCO_BUF_H_EN	RW		1						
	VCO_BUF_M_EN	RW			0					
	VCO_BUF_L_EN	RW				0				
	RESERVE	RW					0			
	VCO_H_EN	RW						1		
	VCO_M_EN	RW							0	
	VCO_L_EN	RW								0

Sub Addr	Register Name [:]	RW	Bit Position							
			7	6	5	4	3	2	1	0
17	RESERVE [2:0]	RW	0	0	0					
	ADJ_VCO_RSW_EN	RW				0				
	REG_VCO_RSW [3:0]	RW					1	0	0	0
18	DIV_BIAS [1:0]	RW	0	1						
	RESERVE	RW			0					
	VCO_CSW [4:0]	RW				0	0	0	0	0
19	RESERVE	RW	0							
	IREF_EN	RW		1						
	ECL2CMOS_EN	RW			1					
	RC_CLK_N_BUF_EN	RW				0				
	RESERVE	RW					0			
	CLK1M_MASTER_EN	RW						0		
	AD_CLK_SEL	RW							0	
	AD_CLK_EN	RW								0
1A	FREQ_CTR_H [7:0]	R	*	*	*	*	*	*	*	*
1B	FREQ_CTR_L [4:0]	R	*	*	*	*	*			
	RESERVE [2:0]	RW						0	0	0
1C	RESERVE [1:0]	RW	0	0						
	COMP_OUT	R			*					
	CP_EN	RW				1				
	CPDA_REF_EN	RW					1			
	CPDA_OUT_EN	RW						0		
	CP_AMP_EN	RW							1	
	COMP_EN	RW								0
1D	RESERVE [3:0]	RW	0	0	0	0				
	PFD_EN	RW					1			
	PFD_TUP	RW						0		
	PFD_TDN	RW							0	
	PFD_CPP	RW								1
1E	TEST_SEL [7:0]	RW	0	0	0	0	0	0	0	0
1F	VER [2:0]	R	*	*	*					
	CHIP_TYPE [2:0]	R				*	*	*		
	SLAVE_ADD [1:0]	R							*	*
20	RESERVE [1:0]	RW	0	0						
	RESERVE [1:0]	R			*	*				
	BIAS165_ENX	RW					0			
	RESERVE [2:0]	RW						0	0	0
21	RESERVE [1:0]	RW	0	0						
	ADJ_LPF_EN	RW			0					
	REG_ADJ_LPF [3:0]	RW				0	1	1		
	RESERVE [1:0]	RW							0	0

Sub Addr	Register Name [:]	RW	Bit Position							
			7	6	5	4	3	2	1	0
22	GIQ_CONT [3:0]	R	*	*	*	*				
	ADJ_GIQ_EN	RW					0			
	REG_ADJ_GIQ [2:0]	RW						0	0	0
23	TEST_BB [3:0]	RW	0	0	0	0				
	XOSC_ENX	R					0			
	RFVGA_ENX	RW						0		
	PS_ALL_EN	RW							0	
	PS_PTL_EN	RW								0
24	RESERVE	RW	0							
	RESERVE [2:0]	R		*	*	*				
	RESERVE	RW					0			
	DELAY_DECODER [2:0]	R						*	*	*
25	RESERVE [3:0]	RW	0	0	0	0				
	MIXBUF_TEST_EN	RW					0			
	LD_ENX	RW						0		
	RESERVE	RW							0	
	TEST_IN_EN	RW								0
26	RF_SW [1:0]	RW	0	0						
	LPF_SW [5:0]	RW			0	0	0	0	0	0
27	LPF_FREQ_DEC [4:0]	R	*	*	*	*	*			
	LPF_TRIM [2:0]	R						*	*	*
28	LPF_TEST_EN	RW	0							
	RESERVE [1:0]	RW		0	0					
	LPF_TEST [4:0]	RW				0	0	1	0	0
29	RESERVE [4:0]	RW	0	0	0	0	0			
	REFOUT_DIV [2:0]	R						*	*	*
2A	PIN_BIAS [1:0]	RW	0	0						
	PIN_GAIN [4:0]	RW			0	0	0	0	0	
	PIN_COMP_EN	RW								0

Application Circuit



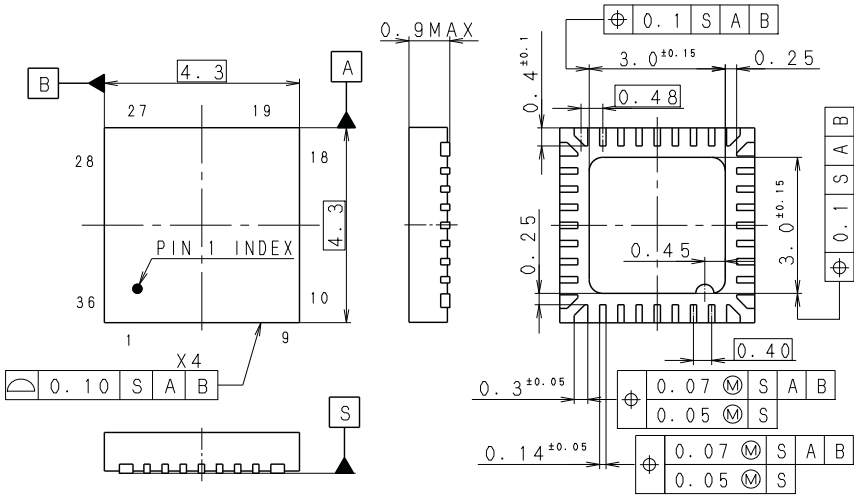
*1: NX2520SA manufactured by NIHON DENPA KOGYO Co., LTD. used.
*2: These are the capacitance values when using the crystal of *1. When using crystals other than shown in *1, determine the adoption of crystal after enough matching verification with a crystal manufacturer.
*3: AGC response time may be affected by these CR, so they are required to be adjusted by this external circuit.

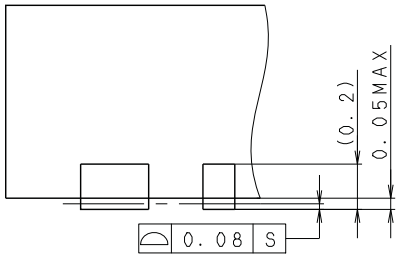
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline

(Unit: mm)
Ass'y: ASE

36PIN VQFN (PLASTIC)





TERMINAL SECTION

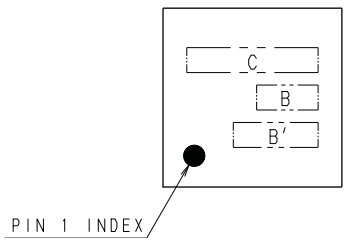
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	Sn PLATING
LEAD MATERIAL	COPPER
PACKAGE MASS	0.04g

SONY CODE	VQFN-36P-481
JEITA CODE	————
JEDEC CODE	————

PART No. AP-2000-36QNAX1	Rev. 0
ISSUED 11.11.28	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS CODE:ER-36-KAX	

Marking



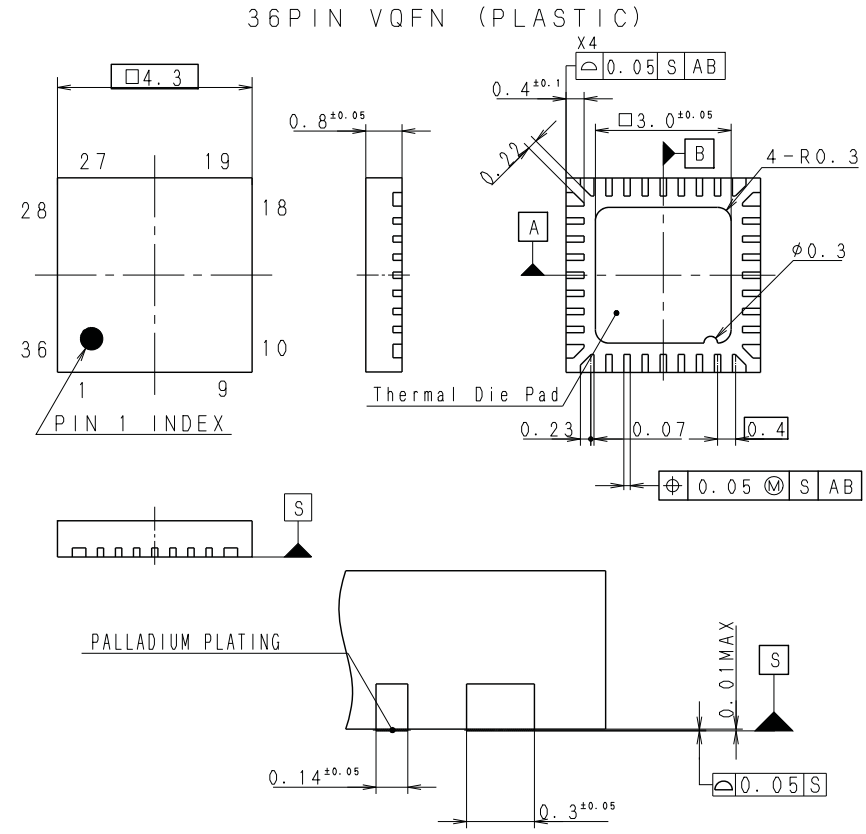
MARKING C: D2818

注1) C部は製品名(Max6文字)を配置する。
(6文字を超える場合は製品名省略標示規定に従う。)
2) B, B' 部はロット番号(Max7文字)を配置する。
(但し B部Max3文字, B' 部Max4文字とする。)

< INSTRUCTIONS >
1) TYPE NO. (MAX 6 CHARACTERS) IN SECTION C.
(FOR MORE THAN 6 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B, B'.
(B: 3 CHARACTERS , B': 4 CHARACTERS.)

Package Outline

(Unit: mm)
Ass'y: KATOH



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

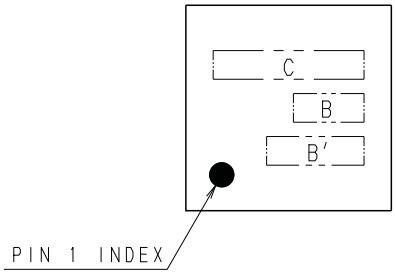
SONY CODE	VQFN-36P-541
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

PART No. AP-2000-36QNBE1	Rev. 0
ISSUED 11.11.24	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:ER-36-KBE	

Marking



MARKING C: D2818

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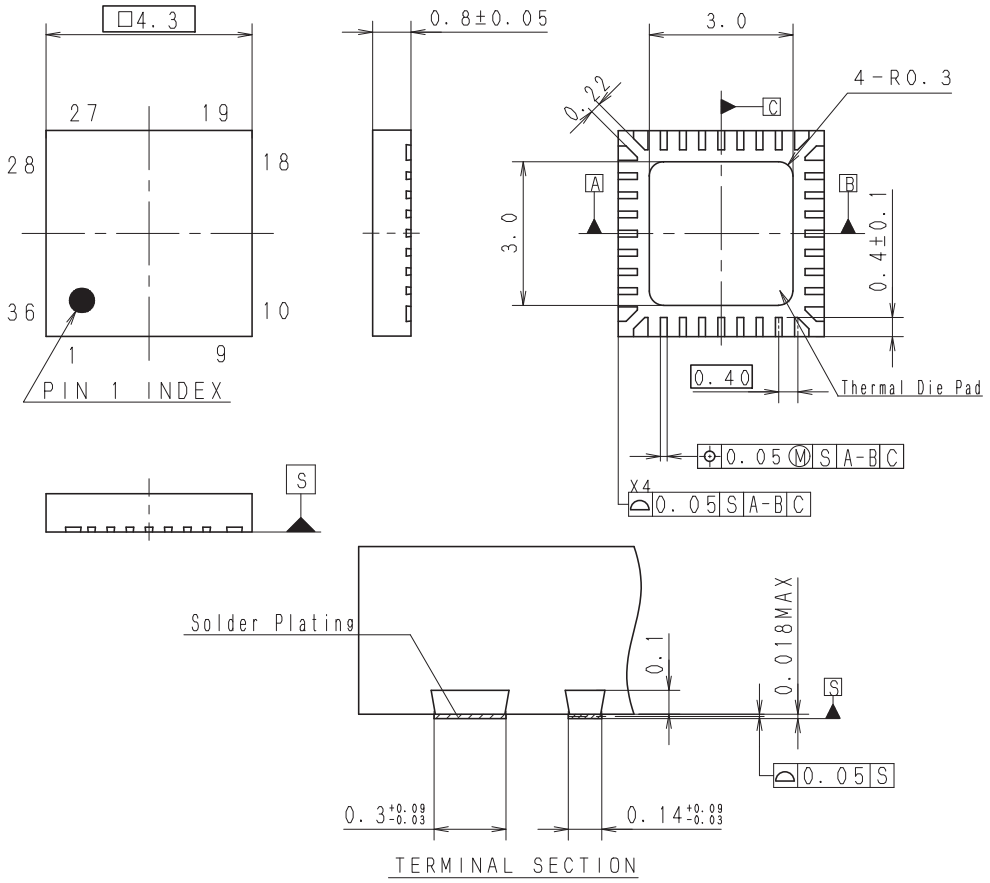
(B: 3 CHARACTERS , B': 4 CHARACTERS.)

Package Outline

(Unit: mm)
Ass'y: SDT



Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	VQFN-36P-08
JEITA CODE	————
JEDEC CODE	————

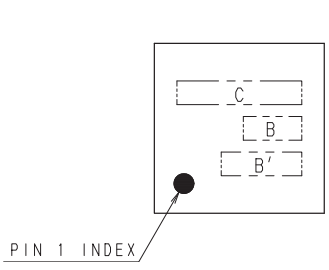
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm

Marking



MARKING C: D2818

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(6文字を超える場合は製品名省略標示規定に従う。)
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