# Video analog input interface — TDA8708

## FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS signal
- No sample-and-hold circuit required

## APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing

## GENERAL DESCRIPTION

The TDA8708 is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz and an input selector.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{CCD}$ | digital supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{CCO}$ | output supply voltage | 4.2 | 5.0 | 5.5 | V |
| $I_{CCA}$ | analog supply current | – | 37 | 45 | mA |
| $I_{CCD}$ | digital supply current | – | 24 | 30 | mA |
| $I_{CCO}$ | output supply current | – | 12 | 16 | mA |
| ILE | DC integral linearity error | – | – | ±1 | LSB |
| DLE | DC differential linearity error | – | – | ±1/2 | LSB |
| $f_{CLK}$ | maximum clock frequency | 30 | – | – | MHz |
| B | maximum −3 dB bandwidth (AGC amplifier) | 12 | 18 | – | MHz |
| $P_{tot}$ | total power dissipation | – | 365 | 500 | mW |

## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TDA8708 | 28 | DIL | plastic | SOT117 |
| TDA8708T | 28 | SO28 | plastic | SOT136A |

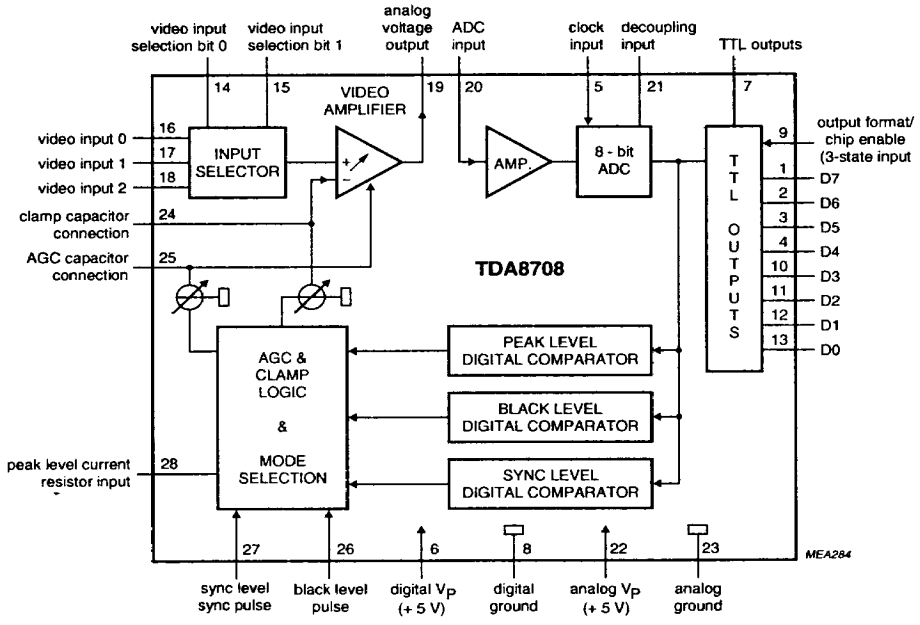



Fig.1 Block diagram.

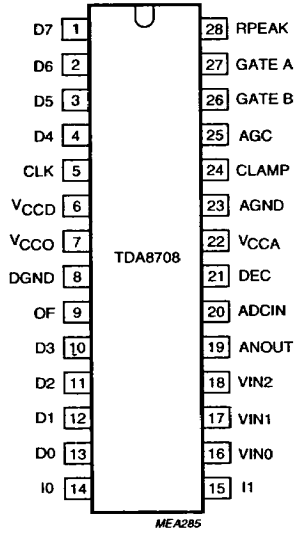



Fig.2 Pin configuration.

**PINNING**

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| D7 | 1 | data output, bit 7 (MSB) |
| D6 | 2 | data output, bit 6 |
| D5 | 3 | data output, bit 5 |
| D4 | 4 | data output, bit 4 |
| CLK | 5 | clock input |
| $V_{CCD}$ | 6 | digital positive supply voltage (5 V) |
| $V_{CCO}$ | 7 | TTL outputs positive supply voltage (5 V) |
| DGND | 8 | digital ground |
| OF | 9 | output format/chip enable (3-state input) |
| D3 | 10 | data output, bit 3 |
| D2 | 11 | data output, bit 2 |
| D1 | 12 | data output, bit 1 |
| D0 | 13 | data output, bit 0 (LSB) |
| I0 | 14 | video input selection bit 0 |
| I1 | 15 | video input selection bit 1 |
| VIN0 | 16 | video input 0 |
| VIN1 | 17 | video input 1 |
| VIN2 | 18 | video input 2 |
| ANOUT | 19 | analog voltage output |
| ADCIN | 20 | analog-to-digital converter input |
| DEC | 21 | decoupling input |
| $V_{CCA}$ | 22 | analog positive supply voltage (+5 V) |
| AGND | 23 | analog ground |
| CLAMP | 24 | clamp capacitor connection |
| AGC | 25 | AGC capacitor connection |
| GATE B | 26 | black level synchronization pulse |
| GATE A | 27 | sync level synchronization pulse |
| RPEAK | 28 | peak level current resistor input |

## FUNCTIONAL DESCRIPTION

The TDA8708 provides a simple interface for decoding video signals.

The TDA8708 operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708 automatically switches to configuration mode 2.

When the TDA8708 is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 240, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{CCA}$ | analog supply voltage range | −0.3 | +7.0 | V |
| $V_{CCD}$ | digital supply voltage range | −0.3 | +7.0 | V |
| $V_{CCO}$ | output supply voltage range | −0.3 | +7.0 | V |
| $V_{CCA} - V_{CCD}$ | supply voltage difference | −1.0 | +1.0 | V |
| $V_{CCO} - V_{CCD}$ | supply voltage difference | −1.0 | +1.0 | V |
| $V_{CCA} - V_{CCO}$ | supply voltage difference | −1.0 | +1.0 | V |
| $V_I$ | input voltage range | −0.3 | $V_{CCA}$ | V |
| $I_O$ | output current | 0 | +10 | mA |
| $T_{stg}$ | storage temperature range | −55 | +150 | °C |
| $T_{amb}$ | operating ambient temperature range | 0 | +70 | °C |
| $T_j$ | junction temperature | 0 | +125 | °C |

## THERMAL RESISTANCE

| SYMBOL | PARAMETER | THERMAL RESISTANCE |
|---|---|---|
| $R_{th\ j-a}$ | from junction to ambient in free air (SOT117) | 55 K/W |
| $R_{th\ j-a}$ | from junction to ambient in free air (SOT136A) | 70 K/W |

## CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CCA}$ | analog supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{CCD}$ | digital supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{CCO}$ | output supply voltage | | 4.2 | 5.0 | 5.5 | V |
| $I_{CCA}$ | analog supply current | | – | 37 | 45 | mA |
| $I_{CCD}$ | digital supply current | | – | 24 | 30 | mA |
| $I_{CCO}$ | output supply current | TTL load (see Fig.8) | – | 12 | 16 | mA |
| **Video amplifier inputs** | | | | | | |
| VIN(0-2) INPUTS | | | | | | |
| $V_{I(p-p)}$ | input voltage (peak-to-peak value) | | 0.45 | 1.0 | 1.6 | V |
| $\|Z_I\|$ | input impedance | f = 6 MHz | 10 | 20 | – | kΩ |
| $C_I$ | input capacitance | f = 6 MHz | – | 1 | – | pF |
| I0 AND I1 TTL INPUTS (SEE TABLE 1) | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_I = 0.4$ V | –400 | – | – | µA |
| $I_{IH}$ | HIGH level input current | $V_I = 2.7$ V | – | – | 20 | µA |
| GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5) | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_I = 0.4$ V | –400 | – | – | µA |
| $I_{IH}$ | HIGH level input current | $V_I = 2.7$ V | – | – | 20 | µA |
| RPEAK INPUT (PIN 28) | | | | | | |
| $I_{28}$ | minimum peak level current | $R_{28} = 0$ Ω | – | 80 | 150 | µA |
| AGC INPUT (PIN 25) | | | | | | |
| $V_{25}$ | AGC voltage for minimum gain | | – | 2.8 | – | V |
| $V_{25}$ | AGC voltage for maximum gain | | – | 4.0 | – | V |
| | AGC output current | see Table 2 | – | – | – | |
| CLAMP INPUT (PIN 24) | | | | | | |
| $V_{24}$ | CLAMP voltage for code 128 output | | – | 3.5 | – | V |
| $I_{24}$ | CLAMP output current | see Table 3 | – | – | – | |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Video amplifier outputs** | | | | | | |
| ANOUT OUTPUT (PIN 19) | | | | | | |
| $V_{19(p-p)}$ | output AC voltage (peak-to-peak value) | $V_{VIN}$ = 1 V (p-p); $V_{25}$ = 3.6 V | – | 1.0 | – | V |
| $I_{19}$ | internal current source | $R_L = \infty$ | 2.0 | 2.5 | – | mA |
| $I_{O(p-p)}$ | output current driven by the load | $V_{ANOUT}$ = 1 V (p-p); note 1 | - | - | 1.0 | mA |
| $V_{19}$ | output DC voltage for black level | note 2 | – | $V_{CCA}$–2.95 | – | V |
| $Z_{19}$ | output impedance | | – | 20 | – | Ω |
| **Video amplifier dynamic characteristics** | | | | | | |
| α | crosstalk between VIN inputs | | – | –60 | –55 | dB |
| $G_{diff}$ | differential gain | $V_{VIN}$ = 1 V (p-p); $V_{25}$ = 3.6 V | – | 2 | – | % |
| $\phi_{diff}$ | differential phase | | – | 2 | – | deg |
| B | –3 dB bandwidth | | 12 | – | – | MHz |
| S/N | signal-to-noise ratio | note 3 | 60 | – | – | dB |
| SVRR | supply voltage ripple rejection | note 4 | – | 45 | – | dB |
| ΔG | gain range | | –4.5 | – | 6.0 | dB |
| **Analog-to-digital converter inputs** | | | | | | |
| CLK INPUT (PIN 5) | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.0 | – | $V_{CCD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{CLK}$ = 0.4 V | –400 | – | – | μA |
| $I_{IH}$ | HIGH level input current | $V_{CLK}$ = 2.7 V | – | – | 100 | μA |
| $\|Z_i\|$ | input impedance | $f_{CLK}$ = 10 MHz | – | 4 | – | kΩ |
| $C_I$ | input capacitance | $f_{CLK}$ = 10 MHz | – | 4.5 | – | pF |
| **OF input (3-state) (see Table 4)** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | – | 0.2 | V |
| $V_{IH}$ | HIGH level input voltage | | 2.6 | – | $V_{CCD}$ | V |
| $V_9$ | input voltage in HIGH-Z state | | – | 1.15 | – | V |
| $I_{IL}$ | LOW level input current | | –370 | –300 | – | μA |
| $I_{IH}$ | HIGH level input current | | – | 360 | 450 | μA |
| ADCIN INPUT (PIN 20) (SEE TABLE 5) | | | | | | |
| $V_{20}$ | input voltage | digital out = 00 | – | $V_{CCA}$ –1.6 | – | V |
| $V_{20}$ | input voltage | digital out = 255 | – | $V_{CCA}$ –1.1 | – | V |
| $V_{20(p-p)}$ | input voltage amplitude (peak-to-peak value) | | – | 0.5 | – | V |
| $I_{20}$ | input current | | – | 1.0 | 10 | μA |
| $\|Z_i\|$ | input impedance | f = 6 MHz | – | 50 | – | MΩ |
| $C_I$ | input capacitance | f = 6 MHz | – | 1 | – | pF |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Analog-to-digital converter outputs** | | | | | | |
| DIGITAL OUTPUTS D(0-7) | | | | | | |
| $V_L$ | LOW level output voltage | $I_O$ = 2 mA | 0 | – | 0.6 | V |
| $V_{OH}$ | HIGH level output voltage | $I_O$ = −0.4 mA | 2.4 | – | $V_{CCD}$ | V |
| $I_{OZ}$ | output current in 3-state mode | 0.4 V < $V_O$ < $V_{CCD}$ | −20 | – | +20 | µA |
| **Switching characteristics** | | | | | | |
| $f_{CLK}$ | CLK input maximum frequency | see Fig.6; note 5 | 30 | – | – | MHz |
| **Analog signal processing ($f_{CLK}$ = 30 MHz; see Fig.8)** | | | | | | |
| $G_{diff}$ | differential gain | $V_{20}$ = 0.5 V (p-p) ; note 6; Fig.3 | – | 2 | – | % |
| $\phi_{diff}$ | differential phase | note 6; Fig.3 | – | 2 | – | deg |
| $f_1$ | fundamental harmonics (full-scale) | $f_i$ = 4.43 MHz; note 6 | – | – | 0 | dB |
| $f_{all}$ | harmonics (full-scale), all components | $f_i$ = 4.43 MHz; note 6 | – | −55 | – | dB |
| SVRR | supply voltage ripple rejection | note 7 | – | 1 | 5 | %/V |
| **Transfer function (see Fig.8)** | | | | | | |
| ILE | DC integral linearity error | | – | – | ±1 | LSB |
| DLE | DC differential linearity error | | – | – | ±0.5 | LSB |
| ILE | AC integral linearity error | note 8 | – | – | ±2 | LSB |
| **Timing ($f_{CLK}$ = 30 MHz; see Figs 7, 8 and 9)** | | | | | | |
| DIGITAL OUTPUTS ($C_L$ = 15 pF; $I_{OL}$ = 2 mA) | | | | | | |
| $t_{dS}$ | sampling delay | | – | 2 | – | ns |
| $t_{HO}$ | output hold time | | 6 | 8 | – | ns |
| $t_d$ | output delay time | | – | 16 | 20 | ns |
| $t_{dEZ}$ | 3-state delay time - output enable | | – | 19 | 25 | ns |
| $t_{dDZ}$ | 3-state delay time - output disable | | – | 14 | 20 | ns |

**Notes to the characteristics**

1. The output current at pin 19 should not exceed 1 mA. The load impedance $R_L$ should be referred to $V_{CC}$ and defined as:

   AC impedance ≥ 1 kΩ and the DC impedance > 2.7 kΩ.

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
2. Control mode 2 is selected.
3. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT(p-p)}}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

**Notes to the characteristics**

4. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

for $V_I$ = 1 V (p-p), 100 kHz gain = 1 and 1 V supply variation.

5. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
6. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
7. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

8. Full-scale sinewave ($f_i$ = 4.4 MHz; $f_{CLK}$, $f_{\overline{CLK}}$ = 27 MHz).

**Table 1** Video input selection (CVBS)

| I1 | I0 | SELECTED INPUT |
|---|---|---|
| 0 | 0 | VIN0 |
| 0 | 1 | VIN1 |
| 1 | 0 | VIN2 |
| 1 | 1 | VIN2 |

**Table 2** AGC output current

| GATE A | GATE B | DIGITAL OUTPUT | $I_{AGC}$ | MODE |
|---|---|---|---|---|
| 1 | 1 | output < 255<br>output > 255 | −2.5 μA<br>$I_{PEAK}$ | 1 |
| 0 | X | output < 240<br>output > 240 | 0<br>$I_{PEAK}$ | 2; note 2 |
| 1 | 0 | output < 0<br>0 < output < 240<br>output > 240 | +2.5 μA<br>−2.5 μA<br>$I_{PEAK}$ | 2; note 2 |

**Notes to Table 2**

1. Where X = don't care
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5)

**Table 3** CLAMP output current

| GATE A | GATE B | DIGITAL OUTPUT | $I_{CLAMP}$ | MODE |
|---|---|---|---|---|
| 1 | 1 | output < 0<br>output > 0 | $I_{PEAK}$<br>−2.5 μA | 1 |
| X | 0 | X | 0 | 2 |
| 0 | 1 | output < 64<br>64 < output | +50 μA<br>−50 μA | 2 |

**Note to Table 3**

1. Where X = don't care

**Table 4** OF input coding

| OF | D0 TO D7 |
|---|---|
| 0 | active, two's complement |
| 1 | high impedance |
| open circuit (note 1) | active, binary |

**Note to Table 4**

1. Use C ≥ 10 pF to DGND

**Table 5** ADC output current

| | | BINARY OUTPUTS | | | | | | | | TWO'S COMPLEMENT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STEP | $V_{ADCIN}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| underflow | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | $V_{CCA}$ - 1.6 V | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| . | | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 254 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 255 | $V_{CCA}$ - 1.1 V | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| overflow | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

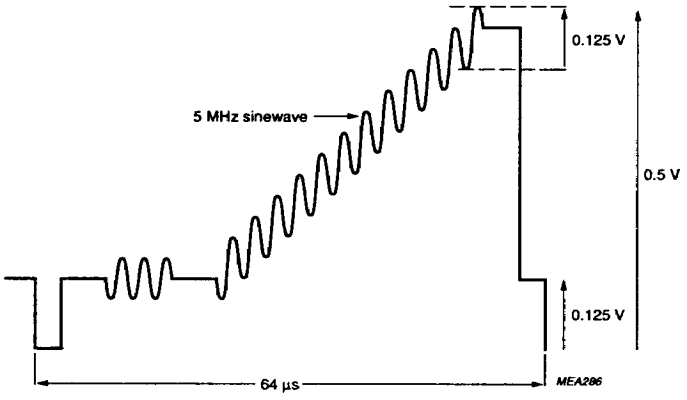



Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

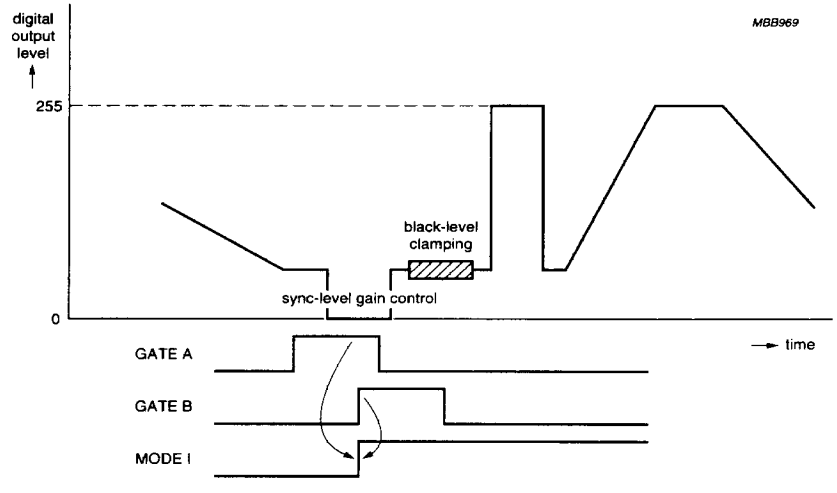



Fig.4 Control mode 1.

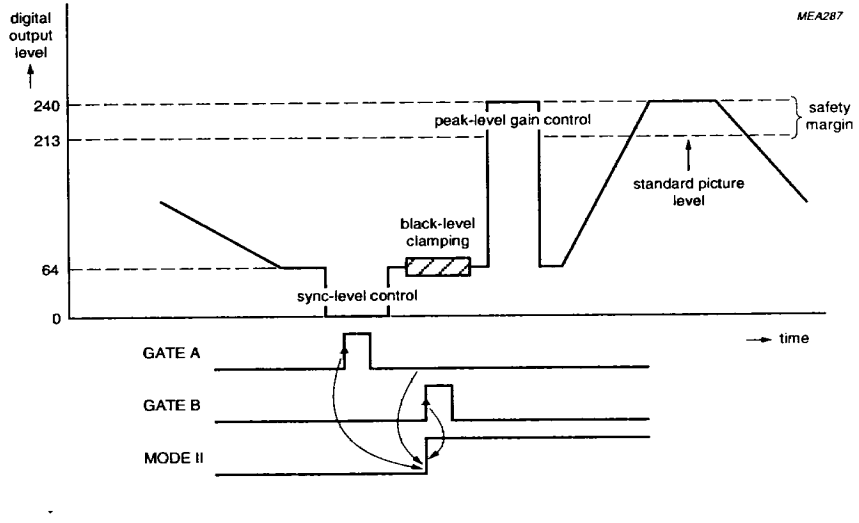



Fig.5 Control mode 2.

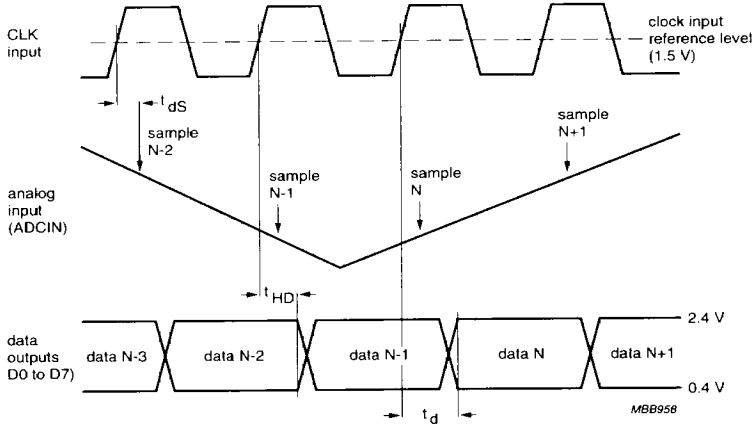



Fig.6 Timing diagram.

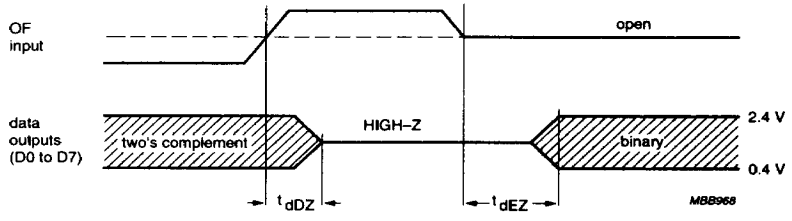



Fig.7 Output format timing diagram.

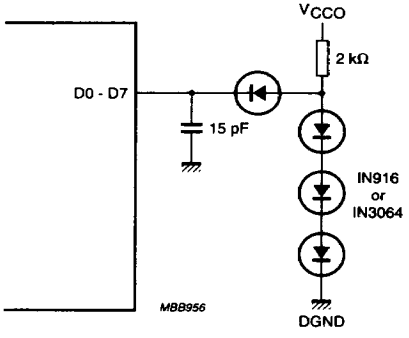



Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

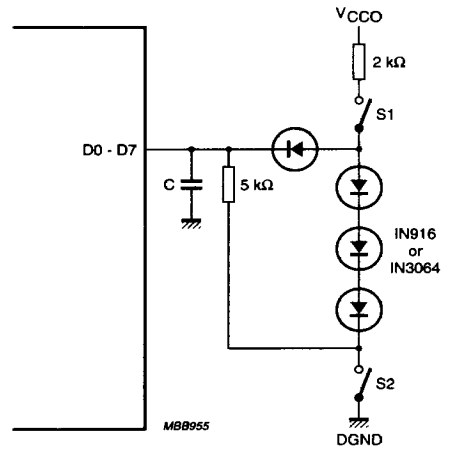



Fig.9 Load circuit for timing measurement; 3-state outputs (OF: $f_i$ = 1 MHz; $V_{OF}$ = 3 V).

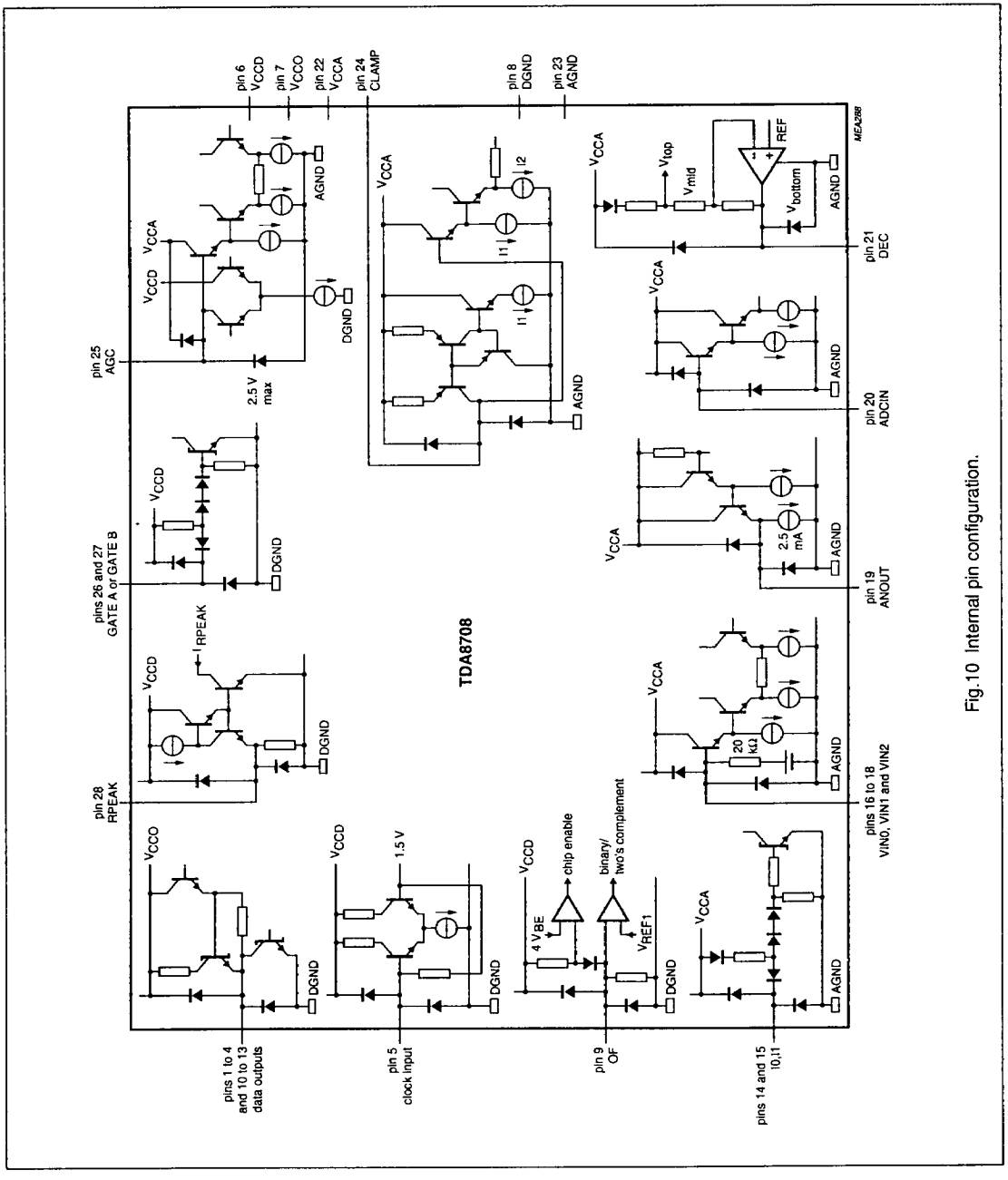
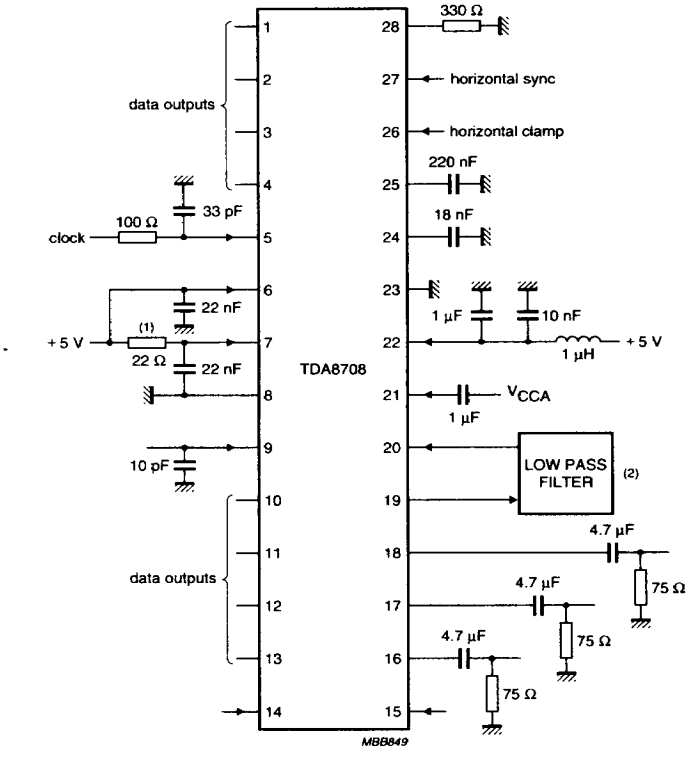



Fig.10 Internal pin configuration.

## APPLICATION INFORMATION

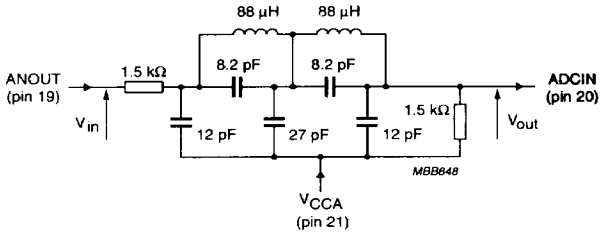
Additional information can be found in the laboratory report FTV/8902.




(1) It is recommended to decouple $V_{CCO}$ through a 22 Ω resistor especially when the output data of TDA8708 interfaces with a capacitive CMOS load device.

(2) See Fig.12 for an example of the low pass filter.

Fig.11 Application diagram.




These filters can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 1.5 kΩ must in any case be applied.

Fig.12 Example of a low pass filter for CVBS signal.