REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R084-93.	93-02-26	Monica L. Poelking
B	Add vendor CAGE F8859. Add device class V criteria. Changes to table I. Editorial changes throughout. - gap	00-01-25	Raymond Monnin
C	Add case outline X. Add delta limits for class V devices. Editorial changes throughout - gap.	00-07-31	Raymond Monnin
D	Change the delta limit for the V_{OH} parameter in table III. Update boilerplate to latest MIL-PRF-38535 requirements. - CFS	01-01-17	Thomas M. Hess
E	Add section 1.5, radiation features. Update the boilerplate to include radiation hardness assured requirements. Editorial changes throughout. - jak	03-12-09	Thomas M. Hess
F	Update the radiation features in section 1.5. Add SEP limits table IB. Update boilerplate paragraphs to current MIL-PRF-38535 requirements – jak.	10-06-16	Thomas M. Hess

REV																				
SHEET																				
REV	F	F																		
SHEET	15	16																		

REV STATUS OF SHEETS															
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Ray Monnin

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
Michael A. Frye

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, QUAD 2-INPUT EXCLUSIVE OR GATE, MONOLITHIC SILICON

DRAWING APPROVAL DATE
89-02-28

AMSC N/A

REVISION LEVEL
F

SIZE	CAGE CODE	
A	**67268**	**5962-89550**

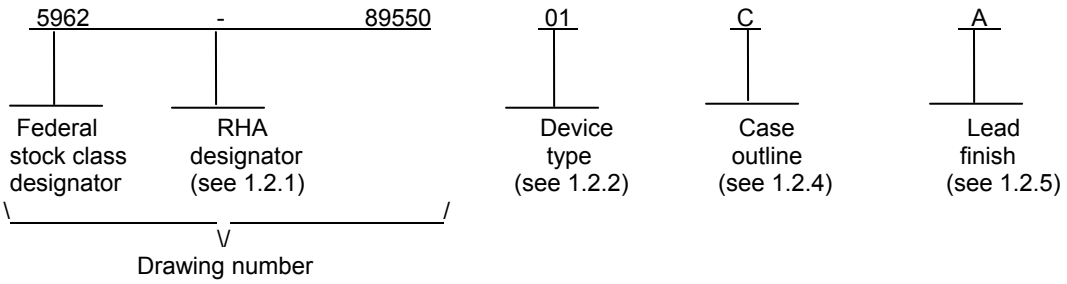
SHEET
1 OF 16

1. SCOPE

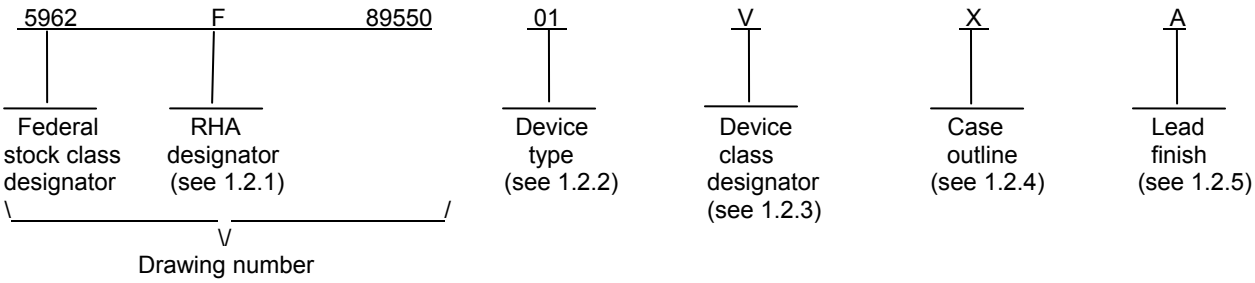
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC86	Quad 2-input exclusive OR gate

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
X	CDFP3-F14	14	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (per output pin) ..... ±50 mA
DC V_{CC} or GND current (per output pin) ..... ±50 mA
Maximum power dissipation (P_D) ..... 500 mW
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 4/

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC}) ..... +2.0 V dc to +6.0 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall times (t_r, t_f):
V_{CC} = 3.6 V and 5.5 V ..... 0 to 8 ns/V

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s) ..... 300 krads (Si)
Single event effects(SEE):
effective LET, no SEL ..... ≤ 93 MeV-cm^2/mg
effective LET, no SEU ..... ≤ 93 MeV-cm^2/mg

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back-up systems. Data retention implies no input transition and no stored data loss with the following conditions: $V_{IH} \geq 70\%\ V_{CC}$, $V_{IL} \leq 30\%\ V_{CC}$, $V_{OH} \geq 70\%\ V_{CC}$ at –20 μA, $V_{OL} \leq 30\%\ V_{CC}$ at 20 μA.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ Unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 1.0 mA	All Q, V	0.0 V	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -1.0 mA	All Q, V	Open	1	-0.4	-1.5	V
High level output voltage 3006	V_{OH} 5/	V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OH} = -50 µA	All All	3.0 V	1, 2, 3	2.9		V
				4.5 V		4.4		
				5.5 V		5.4		
		V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OH} = -12 mA	All All	3.0 V	1	2.56		
					2, 3	2.40		
		V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OH} = -24 mA	All All	4.5 V	1	3.86		
					2, 3	3.70		
				5.5 V	1	4.86		
					2, 3	4.70		
		V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85		
Low level output voltage 3007	V_{OL} 5/	V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OL} = 50 µA	All All	3.0 V	1, 2, 3		0.1	V
				4.5 V			0.1	
				5.5 V			0.1	
		V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OL} = 12 mA	All All	3.0 V	1		0.36	
					2, 3		0.50	
		V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OL} = 24 mA	All All	4.5 V	1		0.36	
					2, 3		0.50	
				5.5 V	1		0.36	
					2, 3		0.50	
		V_{IN} = V_{IH} minimum or V_{IL} maximum I_{OL} = 50 mA	All All	5.5 V	1, 2, 3		1.65	
High level input voltage	V_{IH} 6/		All All	3.0 V	1, 2, 3	2.1		V
				4.5 V		3.15		
				5.5 V		3.85		
Low level input voltage	V_{IL} 6/		All All	3.0 V	1, 2, 3		0.9	V
				4.5 V			1.35	
				5.5 V			1.65	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ Unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Input leakage current low 3009	I_{IL}	V_{IN} = 0.0 V	All	5.5 V	1		-0.1	µA
			All		2, 3		-1.0	
Input leakage current high 3010	I_{IH}	V_{IN} = 5.5 V	All	5.5 V	1		0.1	µA
			All		2, 3		1.0	
Quiescent supply current, output high 3005	I_{CCH}	V_{IN} = V_{CC} or GND	All	5.5 V	1		2.0	µA
			All		2, 3		40	
		M, D, P, L, R, F 7/	01 Q, V		1		50	
Quiescent supply current, output low 3005	I_{CCL}	V_{IN} = V_{CC} or GND	All	5.5 V	1		2.0	µA
			All		2, 3		40	
		M, D, P, L, R, F 7/	01 Q, V		1		50	
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C	All	5.0 V	4		8.0	pF
			All					
Power dissipation capacitance	C_{PD} 8/	See 4.4.1c T_C = +25°C, f = 1 MHz	All	5.0 V	4		60	pF
			All					
Functional tests 3014	9/	V_{IN} = V_{IH} or V_{IL} Verify output V_{OUT} See 4.4.1b	All	3.0 V	7, 8	L	H	
			All					
				5.5 V	7, 8	L	H	
Propagation delay time, An or Bn to Yn 3003	t_{PHL} 10/	C_L = 50 pF minimum R_L = 500Ω See figure 4	All	3.0 V	9	1.0	11.5	ns
			All		10, 11	1.0	14.0	
			All	4.5 V	9	1.0	8.5	
			All		10, 11	1.0	10.0	
	t_{PLH} 10/		All	3.0 V	9	1.0	11.5	ns
			All		10, 11	1.0	14.0	
			All	4.5 V	9	1.0	8.5	
			All		10, 11	1.0	10.0	

See footnotes on next sheet.

TABLE IA. Electrical performance characteristics – Continued.

1/ For tests not listed in the referenced MIL-STD-883, [e.g. V_{IH}, V_{IL}], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.
b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.
c. All I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 01 meet all levels M, D, P, L, R, and F of irradiation. However, these parts are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = 25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table IA, as applicable, at 3.0 V $\leq V_{CC} \leq$ 3.6 V and 4.5 V $\leq V_{CC} \leq$ 5.5 V.

5/ The V_{OH} and V_{OL} tests shall be tested at V_{CC} = 3.0 V and 4.5 V. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for other values of V_{CC}. Limits shown apply to operation at V_{CC} = 3.3 V ±0.3 V and V_{CC} = 5.0 V ±0.5 V. Tests with input current at +50 mA or -50 mA are performed on only one input at a time with duration not to exceed 2 ms. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = V_{IH}$ minimum and V_{IL} maximum. Values for subgroup 1 shall be guaranteed, if not tested, to the limits specified in table IA, herein.

6/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.

7/ The maximum limit for this parameter at 100 krads (Si) is 2 μA.

8/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where:

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$

f is the frequency of the input signal and C_L is the external output load capacitance.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels may be incorporated. For V_{OUT} measurements, L $\leq 0.3V_{CC}$ and H $\geq 0.7V_{CC}$.

10/ For propagation delay tests, all paths must be tested. AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. AC limits at V_{CC} = 3.6 V are equal to limits at V_{CC} = 3.0 V and guaranteed by testing at V_{CC} = 3.0 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns.

TABLE IB. SEP test limits. 1/ 2/

Device type	V_{CC} = 4.5 V 3/	Bias for Single event latch-up (SEL) test V_{CC} = 4.5 V No SEL at effective LET = 4/ 5/ [MeV/(mg/cm^2)]
	Effective LET No single event upsets (SEU) [MeV/(mg/cm^2)]	
01	LET = 93 6/	LET = 93

1/ For SEP test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for SEU at worse case temperature, T_C = +25°C ± 10°C.
4/ Tested for SEL at worst case temperature, T_C = +125°C ± 10°C
5/ Tested to effective LET of 93 MeV/(mg/cm^2) with no SEL.
6/ Tested to a LET of 93 MeV/(mg/cm^2) with no SEU.

Device type All		
Case outlines	C, D, and X	2
Terminal number	Terminal symbol	
1	A1	NC
2	B1	A1
3	Y1	B1
4	A2	Y1
5	B2	NC
6	Y2	A2
7	GND	NC
8	Y4	B2
9	B4	Y2
10	A4	GND
11	Y3	NC
12	B3	Y4
13	A3	B4
14	V_{CC}	A4
15	---	NC
16	---	Y3
17	---	NC
18	---	B3
19	---	A3
20	---	V_{CC}

NC = No internal connection

FIGURE 1. Terminal connections.

Inputs		Outputs
An	Bn	Yn
L	L	L
L	H	H
H	L	H
H	H	L

L = Low voltage level
H = High voltage level

FIGURE 2. Truth table.

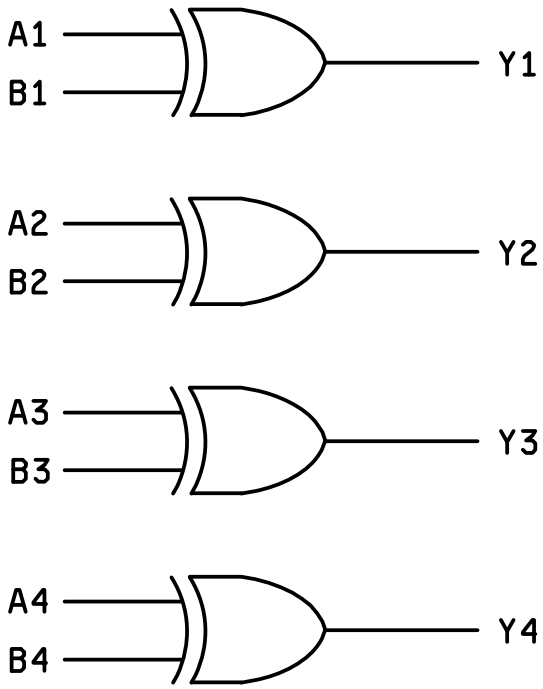
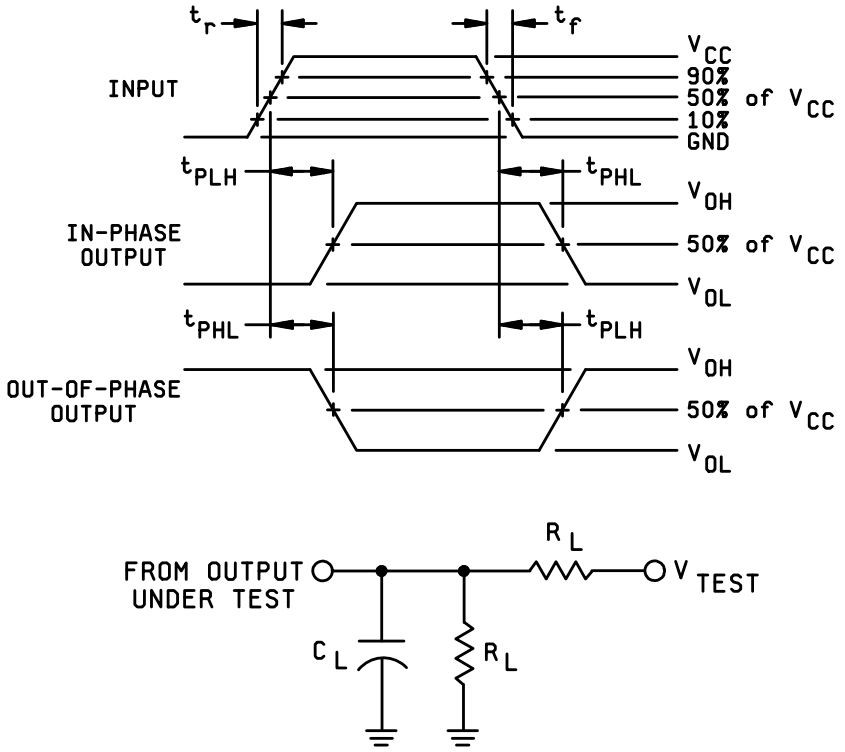


FIGURE 3. Logic diagram.



Notes :

1. V_{TEST} = open for t_{PLH} and t_{PHL}.
2. C_L = 50 pF or equivalent, (includes probe and jig capacitance).
3. R_L = 500Ω or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 1 MHz; Z_O = 50Ω, t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1MHz.
6. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9	1/ 1, 2, 3, 7, 8, 9	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	3/ 1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table III, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, Delta parameters (+25°C). 1/

Parameter 2/	Symbol	Delta Limits
Quiescent supply current	I_{CCH}, I_{CCL}	±150 nA
Input current low level	I_{IL}	±20 nA
Input current high level	I_{IH}	±20 nA
Output voltage low level (V_{CC} = 5.5 V, I_{OL} = 24 mA)	V_{OL}	±0.04 V
Output voltage high level (V_{CC} = 5.5 V, I_{OH} = -24 mA)	V_{OH}	±0.20 V

1/ This table is representation of what vendor CAGE F8859 has experienced and is guaranteed and not meant to be construed as a quality assurance requirement for any other vendor.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. RHA tests for device classes M, Q, and V for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table IA for subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

b. Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing shall be performed on classes M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.3 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates that differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-06-16

Approved sources of supply for SMD 5962-89550 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/SMCR/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/
5962-8955001CA	0C7V7	54AC86DMQB
	01295	SNJ54AC86J
5962-8955001DA	0C7V7	54AC86FMQB
	01295	SNJ54AC86W
5962-89550012A	0C7V7	54AC86LMQB
	01295	SNJ54AC86FK
5962-8955001VDA	3/	54AC86
5962-8955001XA	F8859	54AC86K02Q
5962-8955001XC	F8859	54AC86K01Q
5962-8955001VXA	F8859	54AC86K02V
5962-8955001VXC	F8859	54AC86K01V
5962F8955001XA	F8859	RHFAC86K02Q
5962F8955001XC	F8859	RHFAC86K01Q
5962F8955001VXA	F8859	RHFAC86K02V
5962F8955001VXC	F8859	RHFAC86K01V
5962F8955001CA	F8859	RHF54AC86D04Q
5962F8955001CC	F8859	RHF54AC86D03Q
5962F8955001VCA	F8859	RHF54AC86D04V
5962F8955001VCC	F8859	RHF54AC86D03V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - FRANCE
01295	Texas Instruments Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493