

Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	- 60
R _{DS(on)} (Ω)	V _{GS} = - 10 V 0.28
Q _g max. (nC)	19
Q _{gs} (nC)	5.4
Q _{gd} (nC)	11
Configuration	Single

FEATURES

- Advanced process technology
- Surface mount (IRF9Z24S, SiHF9Z24S)
- 175 °C operating temperature
- Fast switching
- P-channel
- Fully avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

**HALOGEN
FREE**
Available

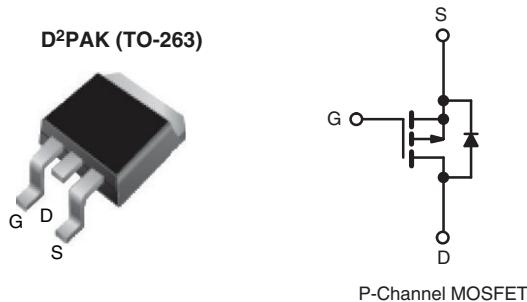
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.



ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF9Z24S-GE3	SiHF9Z24STR-GE3 ^a	SiHF9Z24STR-GE3 ^a
Lead (Pb)-free	IRF9Z24SPbF	IRF9Z24STRLPbF ^a	IRF9Z24STRRPbF ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current ^e	V _{GS} at -10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^{a, e}	I _{DM}	-44	
Linear Derating Factor		0.40	W/°C
Single Pulse Avalanche Energy ^{b, e}	E _{AS}	240	mJ
Repetitive Avalanche Current ^a	I _{AR}	-11	A
Repetitive Avalanche Energy ^a	E _{AR}	6.0	mJ
Maximum Power Dissipation	T _A = 25 °C	3.7	W
		60	W
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	-4.5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Soldering Recommendations (Peak temperature) ^d	for 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = - 25 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = - 11 A (see fig. 12).
- I_{SD} ≤ - 11 A, dI/dt ≤ 140 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
- 1.6 mm from case.
- Uses IRF9Z24, SiHF9Z24 data and test conditions.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mount) ^a	R_{thJA}	-	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	2.5	

Note

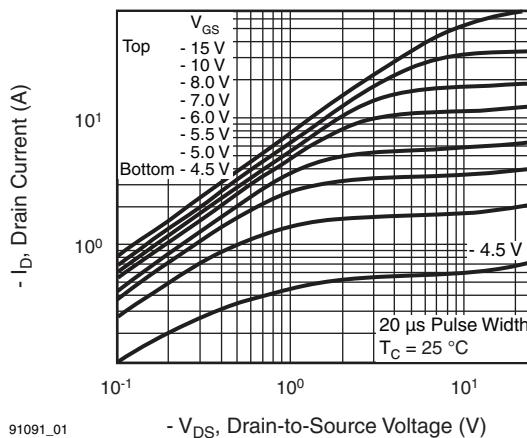
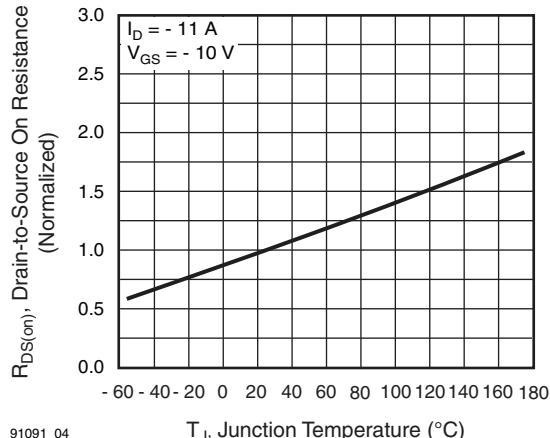
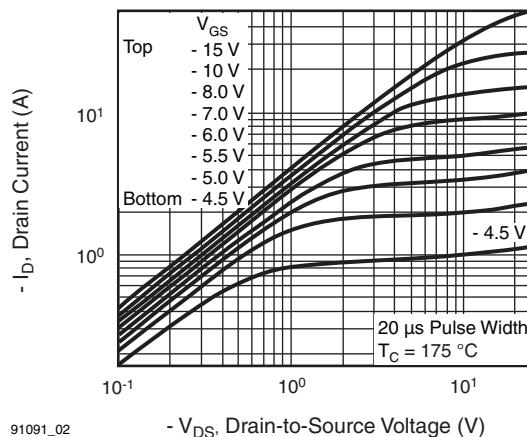
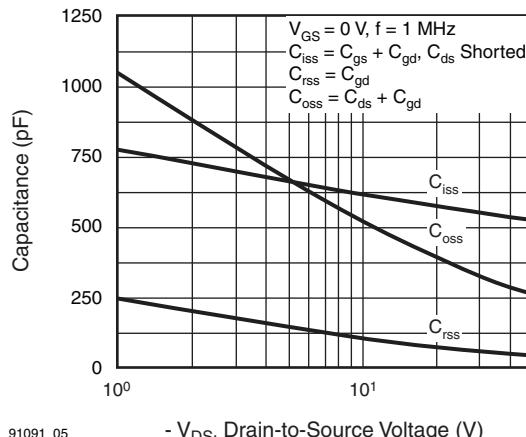
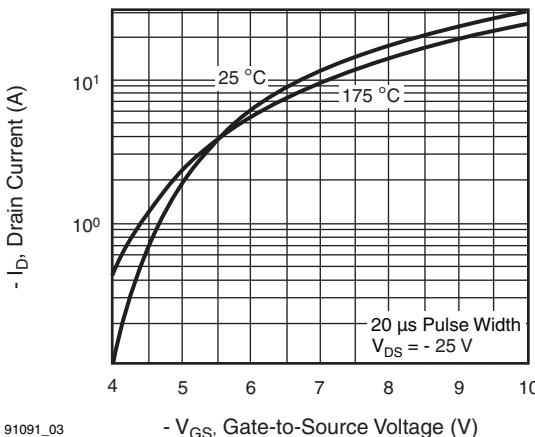
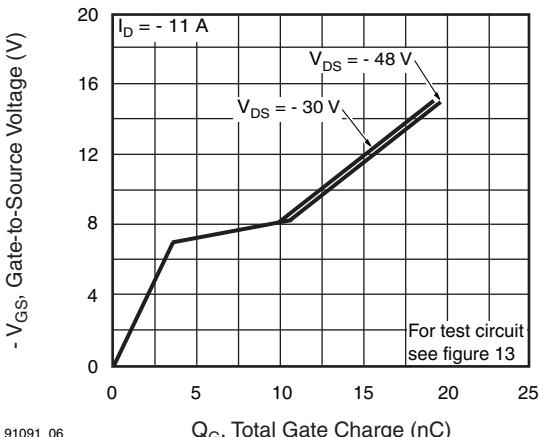
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = -250 \mu A$		-60	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = -1 \text{ mA}^c$		-	-0.056	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$		-2.0	-	-4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	-100	μA	
		$V_{DS} = -48 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 150 \text{ °C}$		-	-	-500		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10 \text{ V}$	$I_D = -6.6 \text{ A}^b$	-	-	0.28	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = -25 \text{ V}$, $I_D = -6.6 \text{ A}^c$		1.4	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = -25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5 ^c		-	570	-	pF	
Output Capacitance	C_{oss}			-	360	-		
Reverse Transfer Capacitance	C_{rss}			-	65	-		
Total Gate Charge	Q_g	$V_{GS} = -10 \text{ V}$	$I_D = -11 \text{ A}$, $V_{DS} = -48 \text{ V}$, see fig. 6 and 13 ^{b, c}	-	-	19	nC	
Gate-Source Charge	Q_{gs}			-	-	5.4		
Gate-Drain Charge	Q_{gd}			-	-	11		
Turn-On Delay Time	$t_{d(on)}$			-	13	-		
Rise Time	t_r	$V_{DD} = -30 \text{ V}$, $I_D = -11 \text{ A}$, $R_g = 18 \Omega$, $R_D = 2.5 \Omega$, see fig. 10 ^b		-	68	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	15	-		
Fall Time	t_f			-	29	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-11	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-44		
Body Diode Voltage	V_{SD}	$T_J = 25 \text{ °C}$, $I_S = -11 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	-6.3	V	
Drain-Source Body Diode Characteristics								
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25 \text{ °C}$, $I_F = -11 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^{b, c}$		-	100	200	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	320	640	nC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.
c. Uses IRF9Z24, SiHF9Z24 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

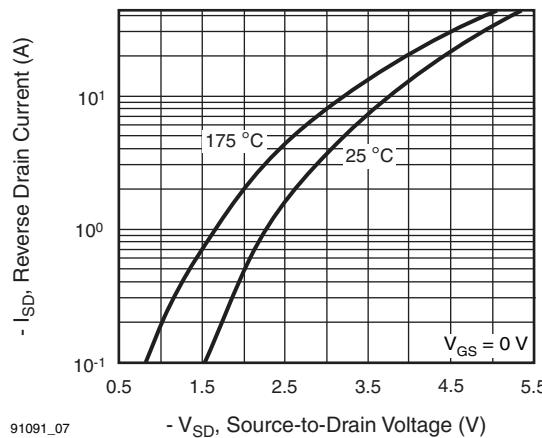


Fig. 7 - Typical Source-Drain Diode Forward Voltage

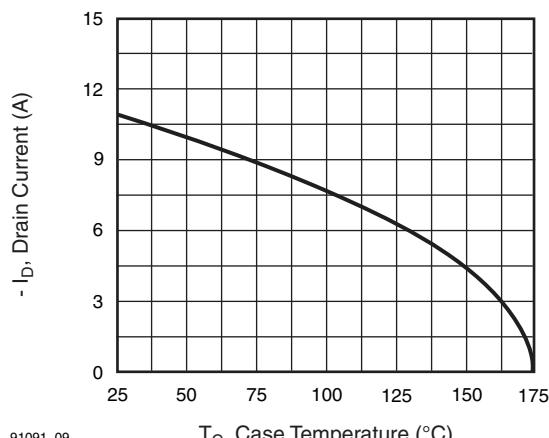


Fig. 9 - Maximum Drain Current vs. Case Temperature

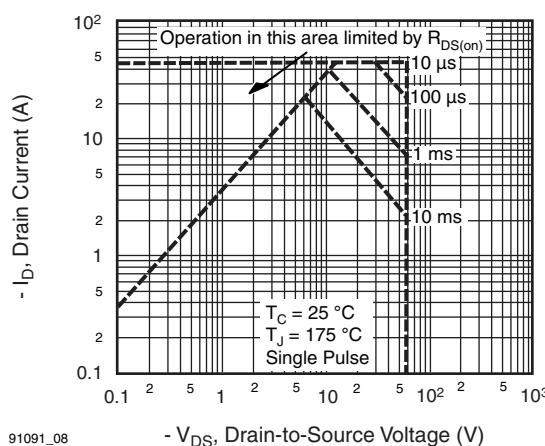


Fig. 8 - Maximum Safe Operating Area

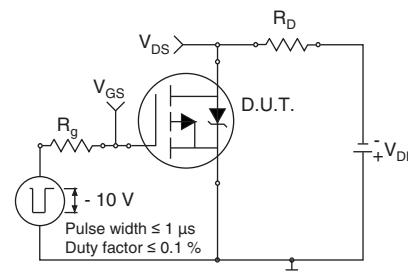


Fig. 10a - Switching Time Test Circuit

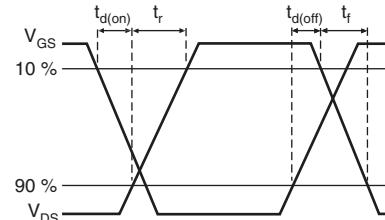


Fig. 10b - Switching Time Waveforms

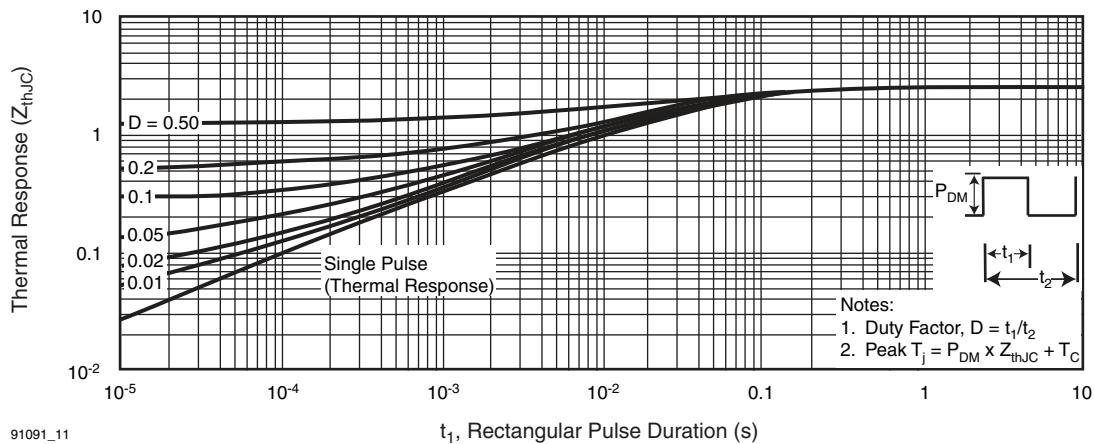
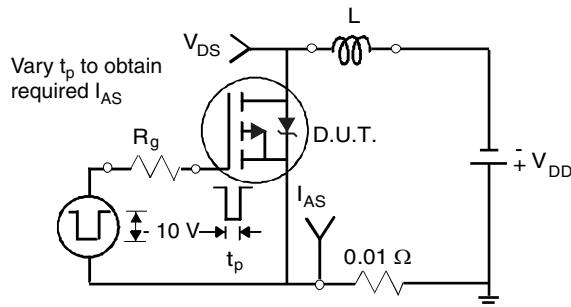
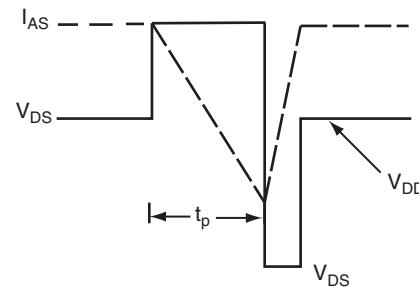
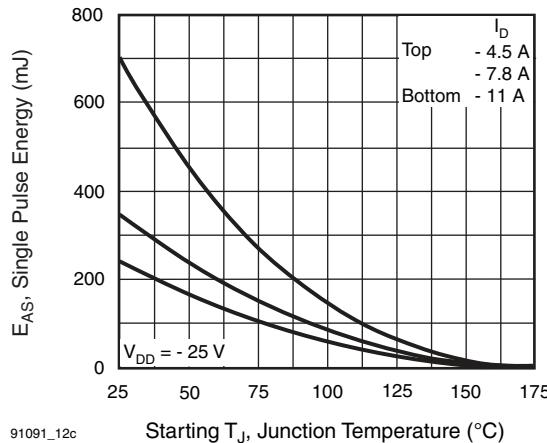
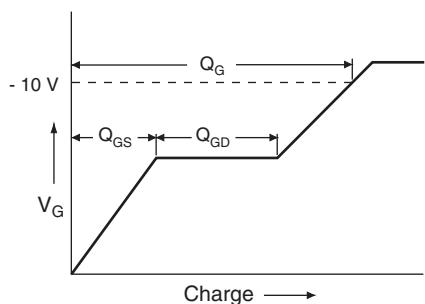
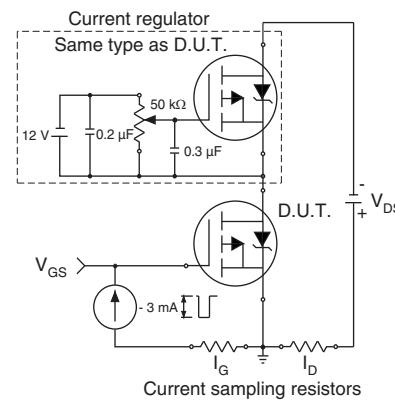
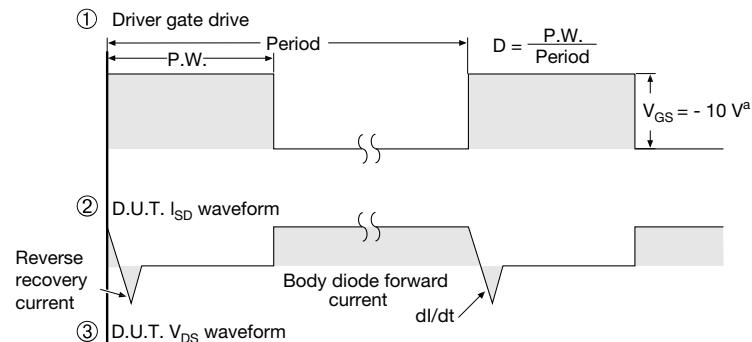
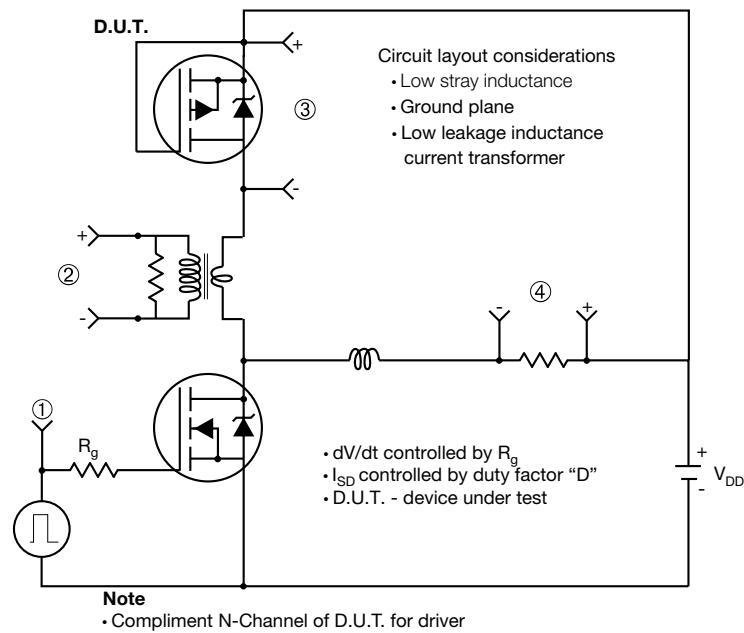


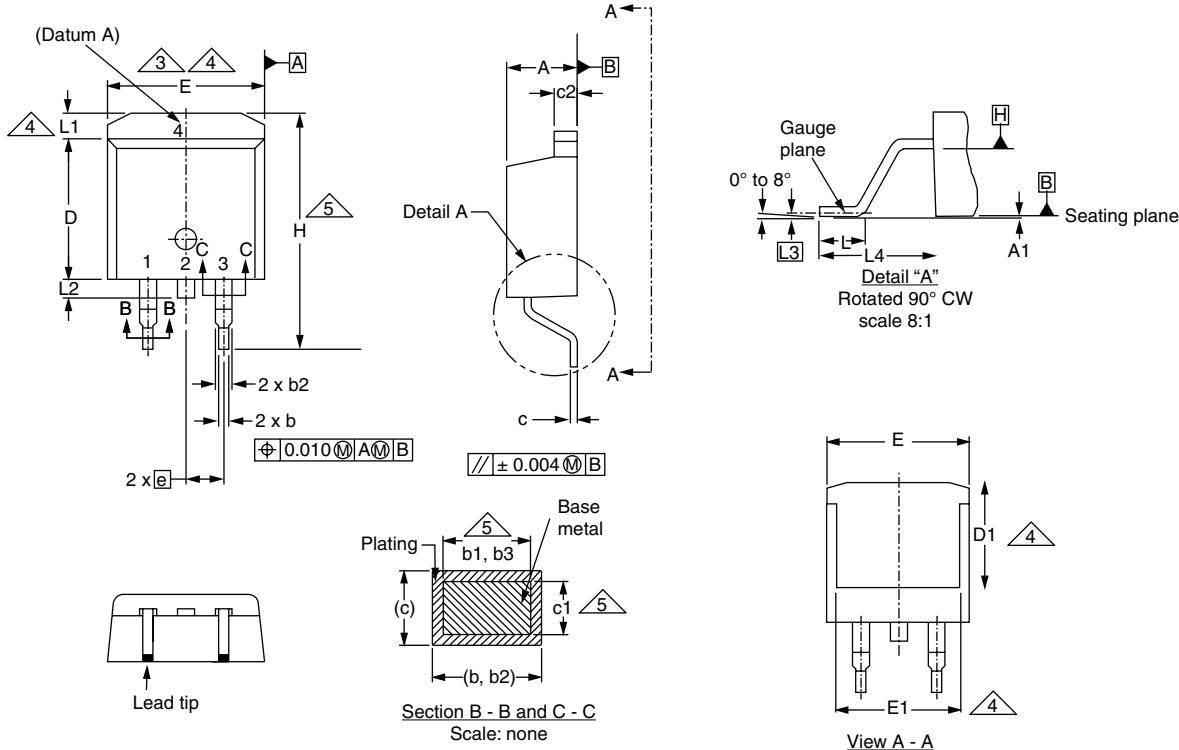
Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Fig. 14 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91091.

TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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