

DESCRIPTION

This family is a 16M bit dynamic RAM organized 4,194,304 x 4-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50, 60 or 70ns) and refresh cycle(2K ref. or 4K ref.) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Fast Page mode operation
- Read-modify-write Capability
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- JEDEC standard pinout
- 24/26-pin Plastic SOJ (300mil)
- 24/26-pin plastic TSOP-II (300mil)
- Single power supply of 5.0V $\pm$ 10%
- Early write or output enable controlled write
- Max. Active power dissipation
- Fast access time and cycle time

Speed	2K refresh	4K refresh
50	798mW	605mW
60	660mW	495mW
70	550mW	440mW

Speed	tRAC	tCAC	tPC
50	50ns	13ns	35ns
60	60ns	15ns	40ns
70	70ns	18ns	45ns

- Refresh cycle

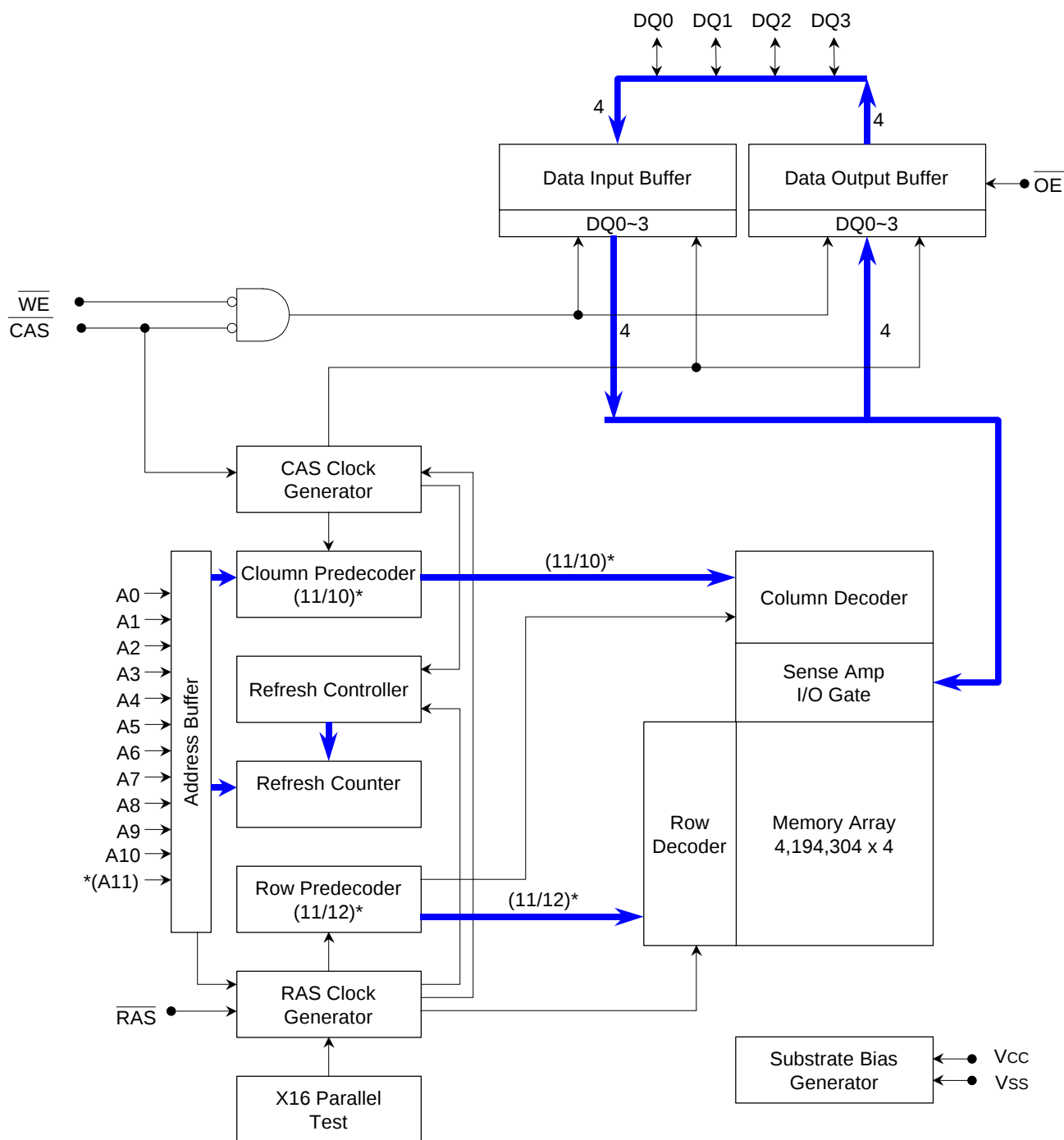
Part number	Refresh	Normal	SL-part
HY5117400C	2K	32ms	256ms
HY5116400C	4K	64ms	

ORDERING INFORMATION

Part Name	Refresh	Power	Package
HY5117400CJ	2K		24/26Pin SOJ
HY5117400CSLJ	2K	SL-part	24/26Pin SOJ
HY5117400CT	2K		24/26Pin TSOP-II
HY5117400CSLT	2K	SL-part	24/26Pin TSOP-II
HY5116400CJ	4K		24/26Pin SOJ
HY5116400CSLJ	4K	SL-part	24/26Pin SOJ
HY5116400CT	4K		24/26Pin TSOP-II
HY5116400CSLT	4K	SL-part	24/26Pin TSOP-II

*SL : Low power with self refresh

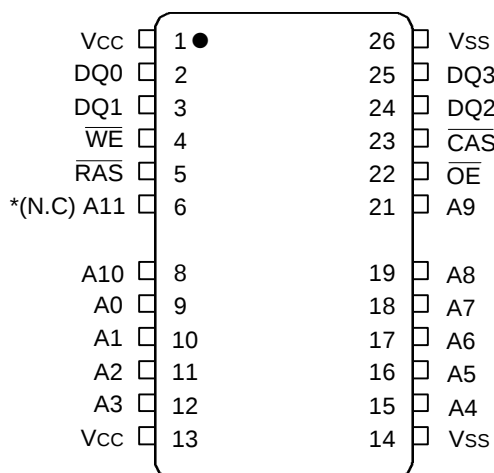
FUNCTIONAL BLOCK DIAGRAM



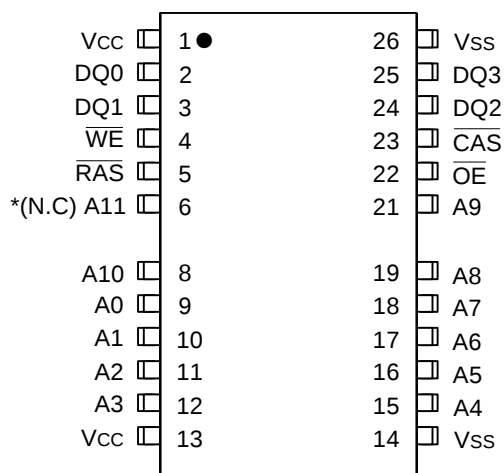
$^*(A11)$ for 4K refresh part

(2K Refresh / 4K Refresh)*

PIN CONFIGURATION (Marking Side)



24/26Pin Plastic SOJ (300mil)



24/26Pin Plastic TSOP-II (300mil)

(N.C)* : For 2K refresh product

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A11	Address Input (4K Refresh Product)
A0~A10	Address Input (2K Refresh Product)
DQ0~DQ3	Data In/Out
Vcc	Power (3.3V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature	0 to 70	°C
T _{STG}	Storage Temperature	-55 to 150	°C
V _{IN} , V _{OUT}	Voltage on Any Pin relative to V _{SS}	-1.0 to 7.0	V
V _{CC}	Voltage on V _{CC} relative to V _{SS}	-1.0 to 7.0	V
I _{OS}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTIC

Symbol	Parameter	Test condition	Min	Max	Unit
I _{LI}	Input Leakage Current (Any input)	V _{SS} ≤ V _{IN} ≤ V _{CC} + 1.0 All other pins not under test = V _{SS}	-10	10	μA
I _{LO}	Output Leakage Current (Any input)	V _{SS} ≤ V _{OUT} ≤ V _{CC} /RAS & /CAS at V _{IH}	-10	10	μA
V _{OL}	Output Low Voltage	I _{OL} = 4.2mA	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -5.0mA	2.4	-	V

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5.0V ± 10%, VSS = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max. Current		Unit
				2K Ref	4K Ref	
Icc1	Operating Current	/RAS, /CAS Cycling tRC = tRC(min.)	50 60 70	145 120 100	110 90 80	mA
Icc2	TTL Standby Current	/RAS, /CAS ≥ VIH Other inputs ≥ VSS	SL-part	2 1	2 1	mA
Icc3	/RAS-only Refresh Current	/RAS Cycling, /CAS = VIH tRC = tRC(min.)	50 60 70	145 120 100	110 90 80	mA
Icc4	Fast Page Mode Current	/CAS Cycling, /RAS = VIL tPC = tPC(min.)	50 60 70	90 80 70	80 70 60	mA
Icc5	CMOS Standby Current	/RAS = /CAS ≥ VCC - 0.2V	SL-part	1 300	1 300	mA μA
Icc6	/CAS-before-/RAS Refresh Current	/RAS & /CAS = 0.2V tRC = tRC(min.)	50 60 70	145 120 100	110 90 80	mA
Icc7	Battery Back-up Current (SL-part)	tRC=125μs (2K Ref), 62.5μs (4K Ref) /CAS = CBR cycling or 0.2V /OE & /WE = VCC - 0.2V Address = VCC-0.2V or 0.2V DQ0~DQ3 = VCC-0.2, 0.2V or Open	tRAS ≤ 300ns	300	300	μA
			tRAS ≤ 1μs	500	500	
Icc8	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as Icc7		300	300	μA

Note

1. Icc1, Icc3, Icc4 and Icc6 depend on output loading and cycle rates(tRC and tPC).
2. Specified values are obtained with output unloaded.
3. Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=VIH within one Fast Page mode cycle time tPC.
4. Only /RAS(max.)=1μs is applied to refresh of battery backup but tRAS(max.) = 10 μs is to applied to normal functional operation.
5. Icc5(max.) = 300 μA, Icc7 and Icc8 are applied to SL-part only.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	50ns		60ns		70ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RC}	Random read or write cycle time	90	-	110	-	130	-	ns	
t _{RWC}	Read-modify-write cycle time	140	-	160	-	180	-	ns	
t _{PC}	Fast Page mode cycle time	35	-	40	-	45	-	ns	
t _{PRWC}	Fast Page mode read-modify-write cycle time	80	-	85	-	90	-	ns	
t _{RAC}	Access time from /RAS	-	50	-	60	-	70	ns	4,5,6
t _{CAC}	Access time from /CAS	-	13	-	15	-	18	ns	4,5
t _{AA}	Access time from column address	-	25	-	30	-	35	ns	4,6
t _{CPA}	Access time from column precharge	-	30	-	35	-	40	ns	4
t _{CLZ}	/CAS to output low impedance	0	-	0	-	0	-	ns	4
t _{OFF}	Output buffer turn-off delay from /CAS	0	10	0	13	0	15	ns	7
t _T	Transition time(rise and fall)	3	50	3	50	3	50	ns	2
t _{RP}	/RAS precharge time	30	-	40	-	50	-	ns	
t _{RAS}	/RAS pulse width	50	10K	60	10K	70	10K	ns	
t _{RASP}	/RAS pulse width(Fast Page cycle)	50	200K	60	200K	70	200K	ns	
t _{RSH}	/RAS hold time	13	-	15	-	18	-	ns	
t _{CSH}	/CAS hold time	50	-	60	-	70	-	ns	
t _{CAS}	/CAS pulse width	13	10K	15	10K	18	10K	ns	
t _{RCD}	/RAS to /CAS delay time	18	37	20	45	20	52	ns	5
t _{RAD}	/RAS to column address delay time	10	25	15	30	15	35	ns	6
t _{CRP}	/CAS to /RAS precharge time	5	-	5	-	5	-	ns	10
t _{CP}	/CAS precharge time	8	-	10	-	10	-	ns	
t _{ASR}	Row address set-up time	0	-	0	-	0	-	ns	
t _{RAH}	Row address hold time	8	-	10	-	10	-	ns	
t _{ASC}	Column address set-up time	0	-	0	-	0	-	ns	
t _{CAH}	Column address hold time	10	-	10	-	10	-	ns	
t _{RAL}	Column address to /RAS lead time	25	-	30	-	35	-	ns	
t _{RCS}	Read command set-up time	0	-	0	-	0	-	ns	
t _{RCH}	Read command hold time referenced to /CAS	0	-	0	-	0	-	ns	8
t _{RRH}	Read command hold time referenced to /RAS	0	-	0	-	0	-	ns	8
t _{WCH}	Write command hold time	8	-	10	-	10	-	ns	
t _{WP}	Write command pulse width	8	-	10	-	10	-	ns	
t _{RWL}	Write command to /RAS lead time	13	-	15	-	18	-	ns	
t _{CWL}	Write command to /CAS lead time	13	-	15	-	18	-	ns	

AC CHARACTERISTICS

Continued

Symbol	Parameter	50ns		60ns		70ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tDS	Data-in set-up time	0	-	0	-	0	-	ns	9
tDH	Data-in hold time	10	-	10	-	10	-	ns	9
tREF	Refresh period(2048 cycles)	-	32	-	32	-	32	ms	
	Refresh period(4096 cycles)	-	64	-	64	-	64	ms	
	Refresh period(SL-part)	-	256	-	256	-	256	ms	
twCS	Write command set-up time	0	-	0	-	0	-	ns	9,10
tcWD	/CAS to /WE delay time	33	-	38	-	43	-	ns	10
trWD	/RAS to /WE delay time	70	-	83	-	95	-	ns	10
tAWD	Column address to /WE delay time	45	-	53	-	60	-	ns	10
tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	5	-	ns	9
tCHR	/CAS hold time(CBR cycle)	10	-	10	-	10	-	ns	9
trPC	/RAS to /CAS precharge time	5	-	5	-	5	-	ns	9
tcPT	/CAS precharge time(CBR counter test)	15	-	20	-	25	-	ns	
tROH	/RAS hold time referenced to /OE	10	-	10	-	10	-	ns	
toEA	/OE access time	-	13	-	15	-	18	ns	
toED	/OE to data delay Time	13	-	15	-	15	-	ns	
toEZ	Output buffer turn-off delay time from /OE	0	10	0	13	0	15	ns	7
toEH	/OE command hold time	10	-	10	-	10	-	ns	
tcpWD	/WE delay time from /CAS precharge	30	-	35	-	40	-	ns	10
trHCP	/RAS hold time from /CAS precharge	30	-	35	-	40	-	ns	
tWRP	/WE to /RAS precharge time(CBR cycle)	10	-	10	-	10	-	ns	
tWRH	/WE to /RAS hold time(CBR cycle)	10	-	10	-	10	-	ns	
trASS	/RAS pulse width(self refresh)	100K	-	100K	-	100K	-	ns	
trPS	/RAS Precharge Time (Self refresh)	90	-	110	-	130	-	ns	
tCHS	/CAS Hold Time (Self refresh)	-50	-	-50	-	-50	-	ns	

TEST MODE

Symbol	Parameter	50ns		60ns		70ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RC}	Random read or write cycle time	95	-	115	-	135	-	ns	
t _{RWC}	Read-modify-write cycle time	145	-	165	-	185	-	ns	
t _{PC}	Fast Page mode cycle time	40	-	45	-	50	-	ns	
t _{PRWC}	Fast Page mode read-modify-write cycle time	85	-	90	-	95	-	ns	
t _{RAC}	Access time from /RAS	-	55	-	65	-	75	ns	4,5,6
t _{CAC}	Access time from /CAS	-	18	-	20	-	23	ns	4,5
t _{AA}	Access time from column address	-	30	-	35	-	40	ns	4,6
t _{CPA}	Access time from /CAS precharge	-	35	-	40	-	45	ns	4
t _{RAS}	/RAS pulse width	55	10K	65	10K	75	10K	ns	
t _{RASP}	/RAS pulse width(Fast Page cycle)	55	200K	65	200K	75	200K	ns	
t _{RSH}	/RAS hold time	18	-	20	-	23	-	ns	
t _{CSH}	/CAS hold time	55	-	65	-	75	-	ns	
t _{CAS}	/CAS pulse width	18	10K	20	10K	23	10K	ns	
t _{RAL}	Column address to /RAS lead time	30	-	35	-	40	-	ns	
t _{CWD}	/CAS to /WE delay time	38	-	43	-	48	-	ns	10
t _{RWD}	/RAS to /WE delay time	75	-	88	-	100	-	ns	10
t _{AWD}	Column address to /WE delay time	50	-	58	-	65	-	ns	10
t _{OEa}	/OE access time	-	18	-	20	-	23	ns	
t _{OEaD}	/OE to data delay Time	18	-	20	-	20	-	ns	
t _{OEh}	/OE command hold time	15	-	15	-	15	-	ns	
t _{CPWD}	/WE delay time from /CAS precharge	35	-	40	-	45	-	ns	10

In test mode, data are written into 16 sectors (each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4sectors connected to one DQ pin are equal (all `1`s or `0`s), the DQ pin indicates a `1`. If they are not equal, the DQ indicates a `0`. The 4Mx4 DRAM can be tested in the same way as a 1Mx4 DRAM is tested.

/WE (when in /CAS-before-/RAS cycle) puts the 4Mx4 DRAM into Test Mode and a /CAS-before-/RAS or a /RAS-only refresh cycle put it back into Normal Mode. /WE (when in /CAS-before-/RAS cycle) shall be used for the refresh operation in the test mode. The test mode function reduces test time(1/4 in case of N test pattern).

NOTE

1. An initial pause of 200 μ s is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA=0 to 70 $^{\circ}$ C) is assured.
4. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 2TTL loads and 100pF.
5. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
6. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
7. tOFF and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles.
10. twCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD $\geq$ tRWD(min.), tCWD $\geq$ tCWD(min.), tAWD $\geq$ tAWD(min.), and tCPWD $\geq$ tCPWD(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

CAPACITANCE

(TA = 25 $^{\circ}$ C, VCC = 5.0V $\pm$ 10%, VSS = 0V and f=1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
CIN1	Input Capacitance (A0~A11)	-	5	pF
CIN2	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
CDQ	Data Input / Output Capacitance (DQ0~DQ3)	-	7	pF