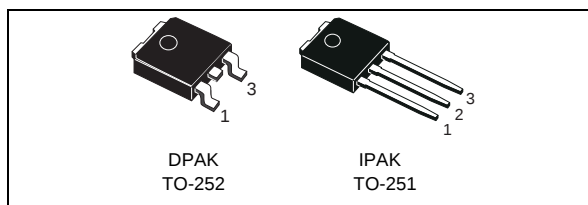


OMNIFET II fully autoprotected Power MOSFET

Datasheet - production data



Description

The VND5N07-E is a monolithic device designed using STMicroelectronics® VIPower® M0 technology, intended for replacement of standard Power MOSFETs from DC to 50 KHz applications. Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Features

Max. on-state resistance (per ch.)	$R_{DS(on)}$	0.2Ω
Current limitation (typ)	I_{LIMH}	5 A
Drain-Source clamp voltage	V_{CLAMP}	70V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the power mosfet (analog driving)
- Compatible with standard Power MOSFET

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
DPAK	VND5N07-E	VND5N07TR-E
IPAK	VND5N07-1-E	

Contents

1	Block diagram and pin description	5
2	Electrical specifications	6
2.1	Absolute maximum ratings	6
2.2	Thermal data	6
2.3	Electrical characteristics	7
2.4	Electrical characteristics curves	13
3	Protection features	17
3.1	Overvoltage clamp protection	17
3.2	Linear current limiter circuit	17
3.3	Overtemperature and short circuit protection	17
3.4	Status feedback	17
4	Package and packing information	18
4.1	ECOPACK® packages	18
4.2	DPAK mechanical data	18
4.3	IPAK mechanical data	20
5	Revision history	21

List of tables

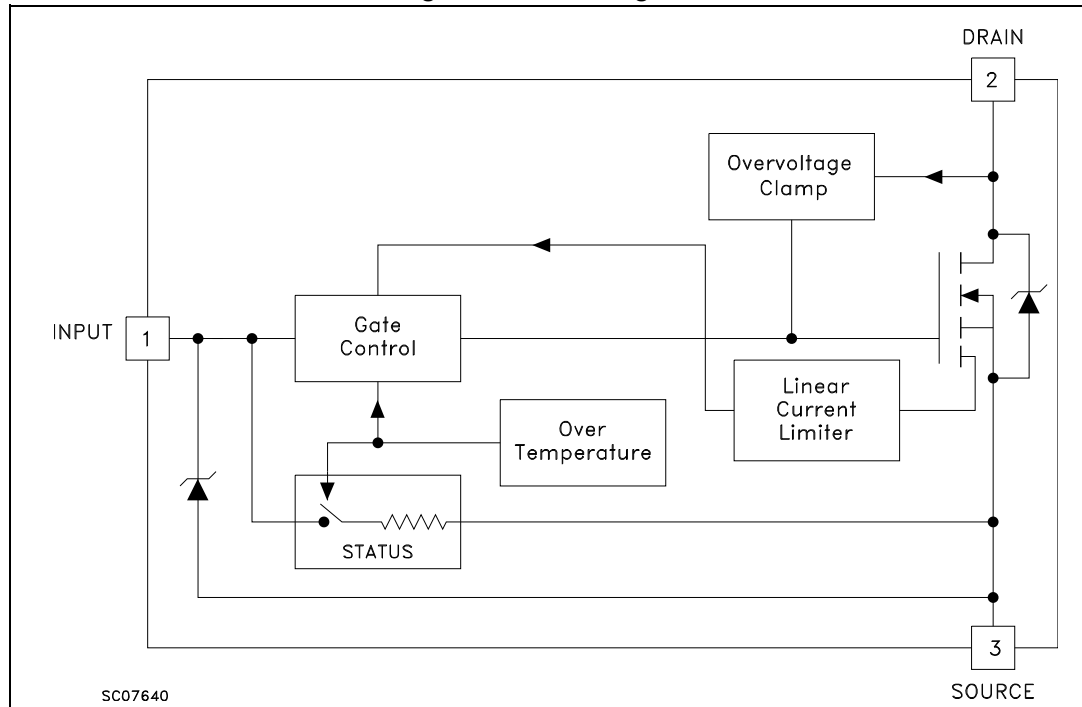
Table 1.	Device summary	1
Table 2.	Absolute maximum ratings	6
Table 3.	Thermal data.	6
Table 4.	Off	7
Table 5.	On	7
Table 6.	Dynamic	7
Table 7.	Switching	7
Table 8.	Source drain diode	8
Table 9.	Protections ($-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise specified)	8
Table 10.	DPAK mechanical data.	19
Table 11.	IPAK mechanical data	20
Table 12.	Document revision history	21

List of figures

Figure 1.	Block diagram	5
Figure 2.	Switching time test circuit for resistive load	9
Figure 3.	Test circuit for diode recovery times	9
Figure 4.	Unclamped inductive load test circuits	10
Figure 5.	Input charge test circuit.	10
Figure 6.	Unclamped inductive waveforms	11
Figure 7.	Switching waveforms	11
Figure 8.	Thermal impedance for DPAK / IPAK	12
Figure 9.	Source-drain diode forward characteristics	13
Figure 10.	Static drain-source on resistance	13
Figure 11.	Derating curve	13
Figure 12.	Static drain-source on resistance vs. input voltage	13
Figure 13.	Normalized on resistance Vs temperature	13
Figure 14.	Transconductance	13
Figure 15.	Static drain-source on resistance Vs. I_d	14
Figure 16.	Switching time resistive load.	14
Figure 17.	Turn-on current slope ($V_{IN} = 10\text{ V}$)	14
Figure 18.	Turn-on current slope ($V_{IN} = 5\text{ V}$)	14
Figure 19.	Input voltage vs. input charge.	14
Figure 20.	Turn-off drain source voltage slope	14
Figure 21.	Turn-off drain-source voltage slope	15
Figure 22.	Capacitance variations	15
Figure 23.	Switching time resistive load.	15
Figure 24.	Step response current limit.	15
Figure 25.	Output characteristics	15
Figure 26.	Normalized on resistance vs. temperature	15
Figure 27.	Normalized input threshold voltage vs. temperature	16
Figure 28.	Normalized current limit vs. junction temperature.	16
Figure 29.	DPAK package dimensions	18
Figure 30.	IPAK mechanical data and package outline	20

1 Block diagram and pin description

Figure 1. Block diagram



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-Source voltage ($V_{INn} = 0\text{ V}$)	Internally clamped	V
V_{INn}	Input voltage	18	V
I_{Dn}	Drain current	Internally limited	A
I_{Rn}	Reverse DC output current	-7	A
V_{ESD}	Electrostatic discharge ($R = 1.5\text{ K}\Omega$, $C = 100\text{ pF}$)	2000	V
P_{tot}	Total dissipation at $T_c = 25^\circ\text{C}$	60	W
T_j	Operating junction temperature	Internally limited	$^\circ\text{C}$
T_c	Case operating temperature	Internally limited	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.75	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	100	$^\circ\text{C/W}$

2.3 Electrical characteristics

T_{case} = 25 °C unless otherwise stated.

Table 4. Off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CLAMP}	Drain-Source clamp voltage	V _{IN} = 0 V; I _D = 200 mA	60	70	80	V
V _{CLTH}	Drain-Source threshold voltage	V _{IN} = 0 V; I _D = 2 mA	55			V
I _{ISS}	Supply current from input pin	V _{DS} = 0 V; V _{IN} = 10 V		250	500	μA
V _{INCL}	Input-Source reverse clamp voltage	I _{IN} = 1 mA	-1.0		-0.3	V
I _{DSS}	Zero input voltage drain current (V _{IN} = 0 V)	V _{DS} = 13 V; V _{IN} = 0 V			50	μA
		V _{DS} = 25 V; V _{IN} = 0 V			200	μA

Table 5. On⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R _{DS(on)}	Static drain-source on resistance	V _{IN} = 10 V; I _D = 2.5 A			200	mΩ
		V _{IN} = 5 V; I _D = 2.5 A			280	mΩ
V _{IN(th)}	Input threshold voltage	V _{DS} = V _{in} ; I _D + I _{in} = 1 mA	0.8		3	V

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%.

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 13 V; I _D = 2.5 A	3	4		S
C _{OSS}	Output capacitance	V _{DS} = 13 V; f = 1 MHz; V _{IN} = 0 V		200	300	pF

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%.

Table 7. Switching⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 15 V; I _D = 2.5 A; V _{gen} = 10 V; R _{gen} = 10 Ω		50	100	ns
t _r	Rise time			60	100	ns
t _{d(off)}	Turn-off delay time			150	300	ns
t _f	Fall time			40	80	ns

Table 7. Switching⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 2.5\text{ A};$ $V_{gen} = 10\text{ V}; R_{gen} = 1\text{ k}\Omega$		150	250	ns
t_r	Rise time			400	600	ns
$t_{d(off)}$	Turn-off delay time			3900	5000	ns
t_f	Fall time			1100	1600	ns
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15\text{ V}; I_D = 2.5\text{ A};$ $V_{in} = 10\text{ V}; R_{gen} = 10\text{ }\Omega$		80		A/ μ S
Q_i	Total input charge	$V_{DD} = 12\text{ V}; I_D = 2.5\text{ A};$ $V_{IN} = 10\text{ V}$		18		nC

1. Parameters guaranteed by design / characterization.

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 2.5\text{ A}; V_{IN} = 0\text{ V}$			1.6	V
$t_{rr}^{(2)}$	Reverse recovery time	$I_{SD} = 2.5\text{ A}; di/dt = 100\text{ A}/\mu\text{s};$ $V_{DD} = 30\text{ V}$		150		ns
$Q_{rr}^{(2)}$	Reverse recovery charge			0.3		μ C
$I_{RRM}^{(2)}$	Reverse recovery current			5.7		A

1. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.

2. Parameters guaranteed by design / characterization.

Table 9. Protections ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain current limit	$V_{IN} = 10\text{ V}; V_{DS} = 13\text{ V}$	3.5	5	7	A
		$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$	3.5	5	7	A
$t_{dlim}^{(1)}$	Step response current limit	$V_{IN} = 10\text{ V}$		15	20	μ S
		$V_{IN} = 5\text{ V}$		40	60	μ S
$T_{jsh}^{(1)}$	Overtemperature shutdown		150			$^\circ\text{C}$
$T_{jrs}^{(1)}$	Overtemperature reset		135			$^\circ\text{C}$
$I_{gf}^{(1)}$	Fault sink current	$V_{IN} = 10\text{ V}; V_{DS} = 13\text{ V}$		50		mA
		$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$		20		mA
$E_{as}^{(1)}$	Single pulse avalanche energy	Starting $T_j = 25^\circ\text{C}; V_{DD} = 20\text{ V};$ $V_{IN} = 10\text{ V}; R_{gen} = 1\text{ k}\Omega;$ $L = 10\text{ mH}$	0.2			J

1. Parameters guaranteed by design / characterization.

Figure 2. Switching time test circuit for resistive load

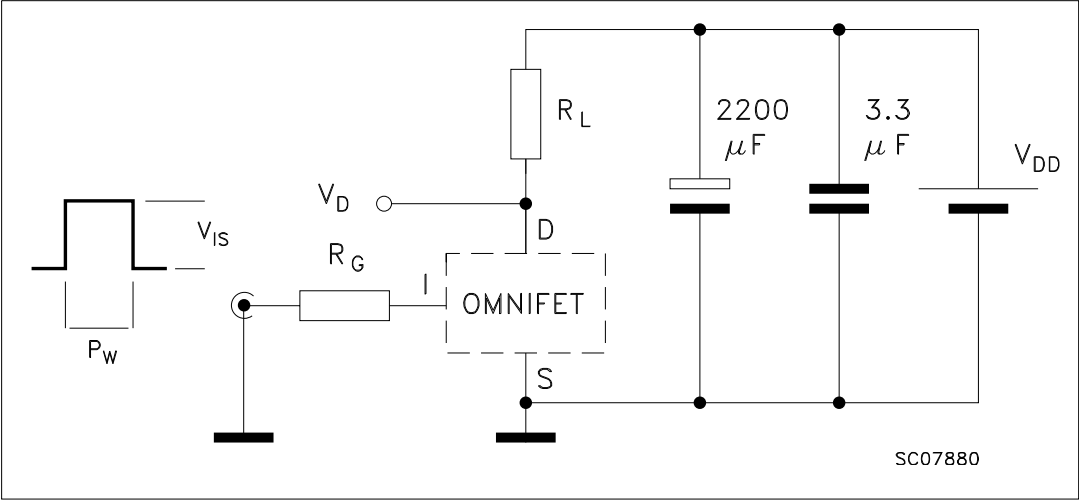


Figure 3. Test circuit for diode recovery times

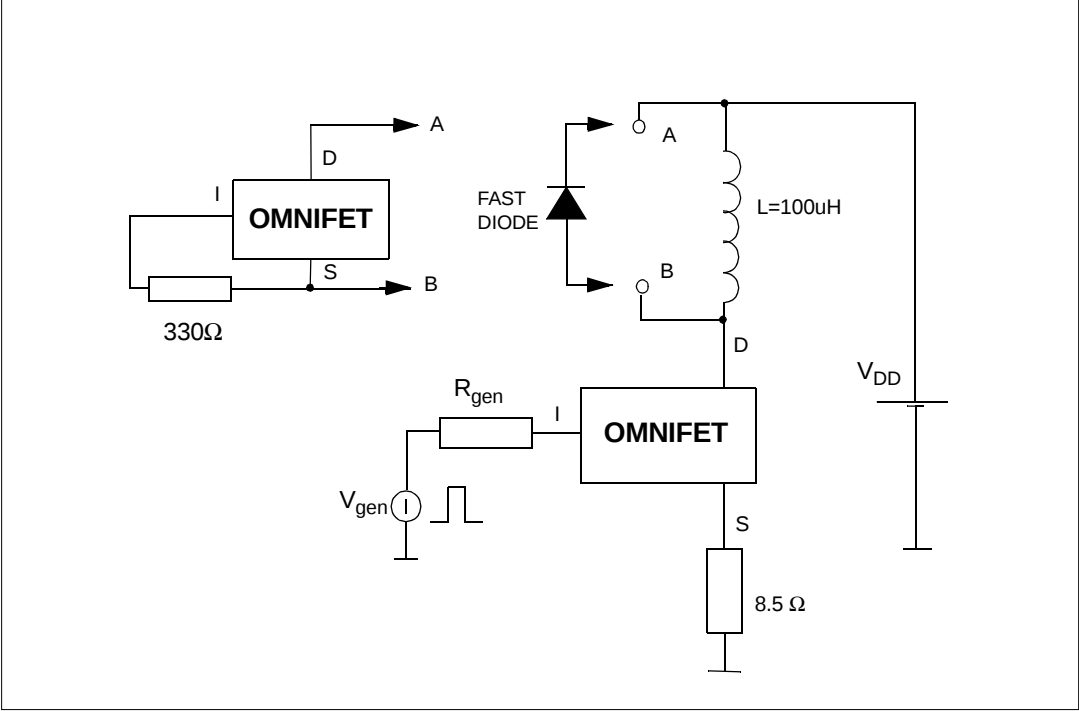


Figure 4. Unclamped inductive load test circuits

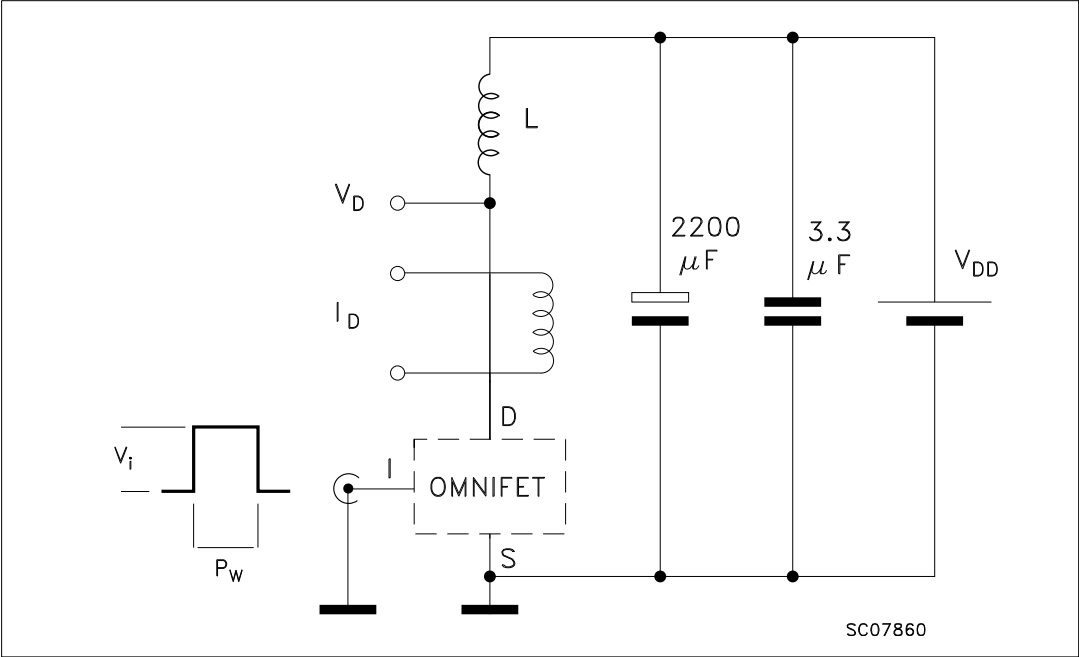


Figure 5. Input charge test circuit

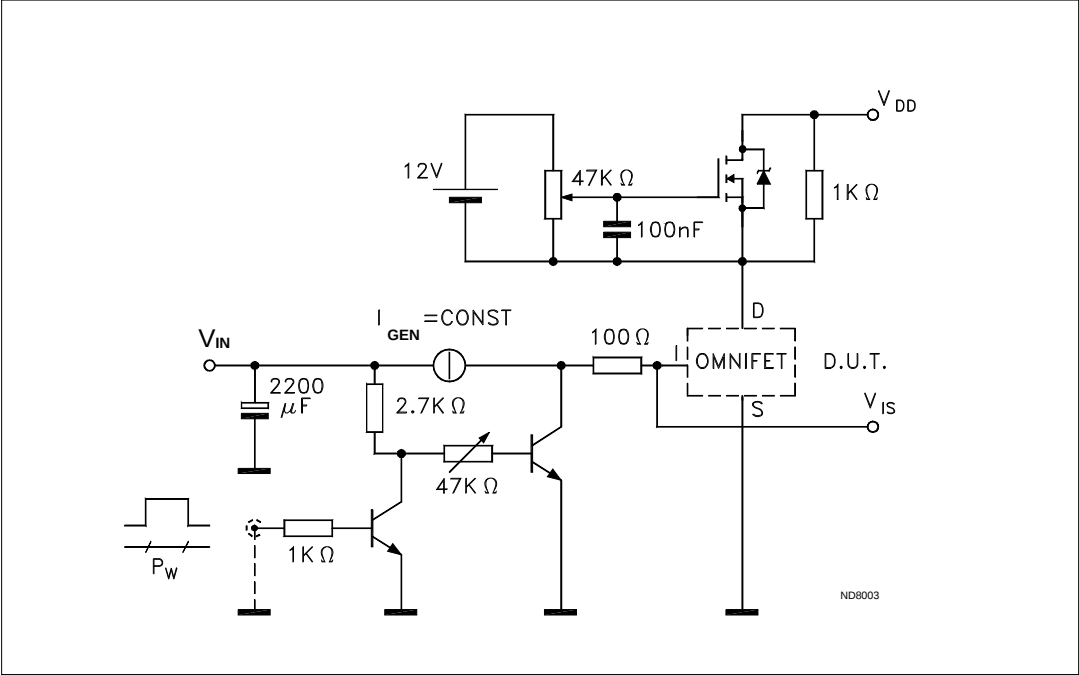


Figure 6. Unclamped inductive waveforms

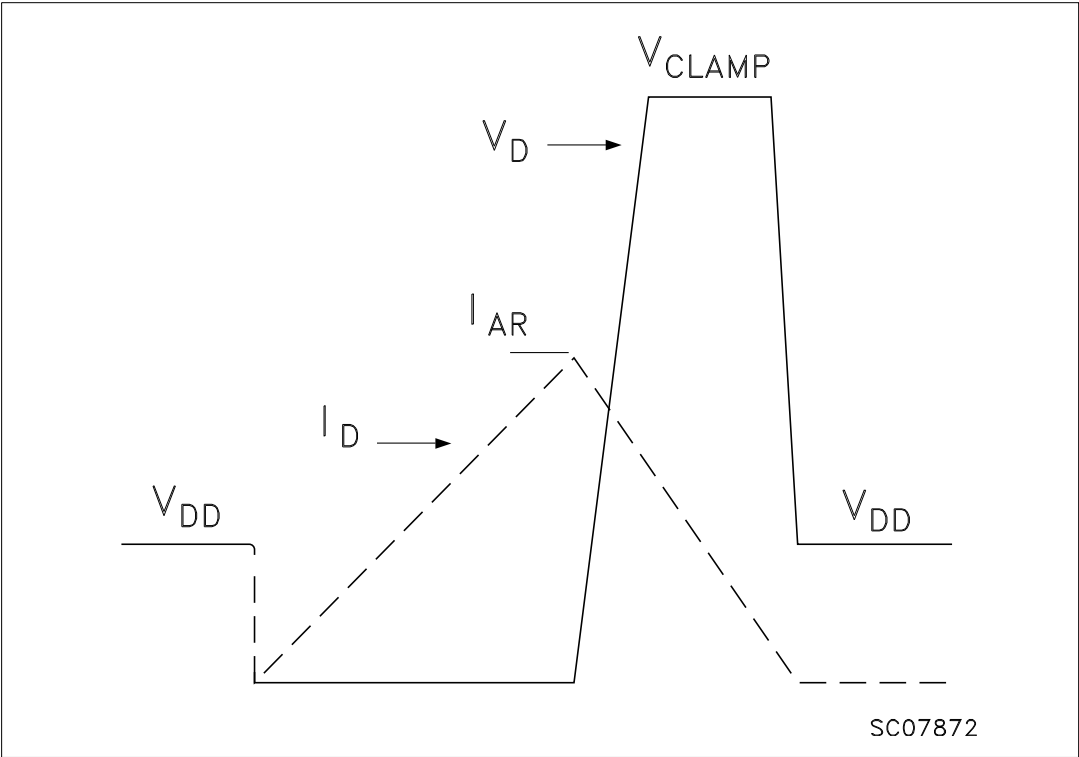


Figure 7. Switching waveforms

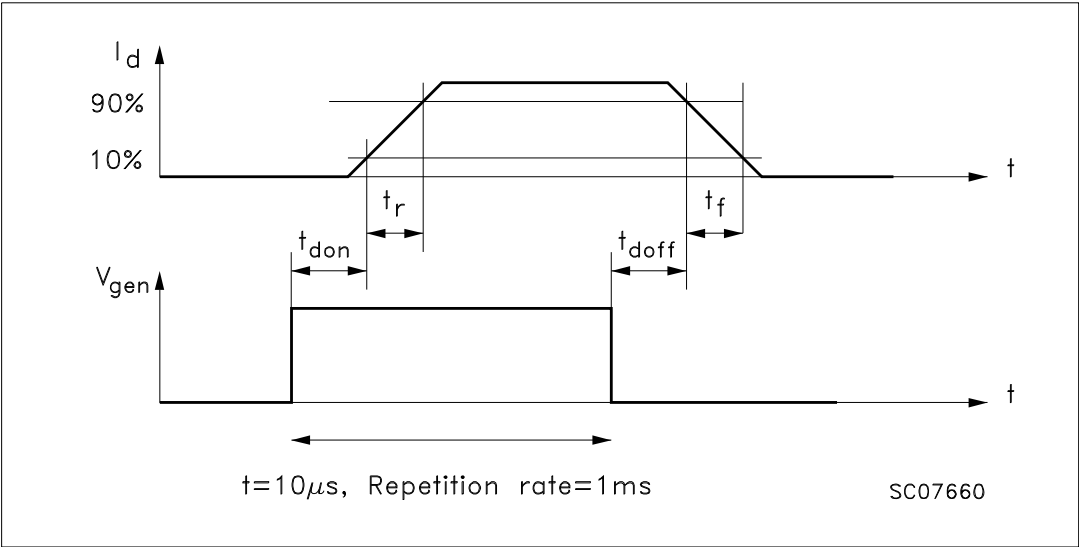
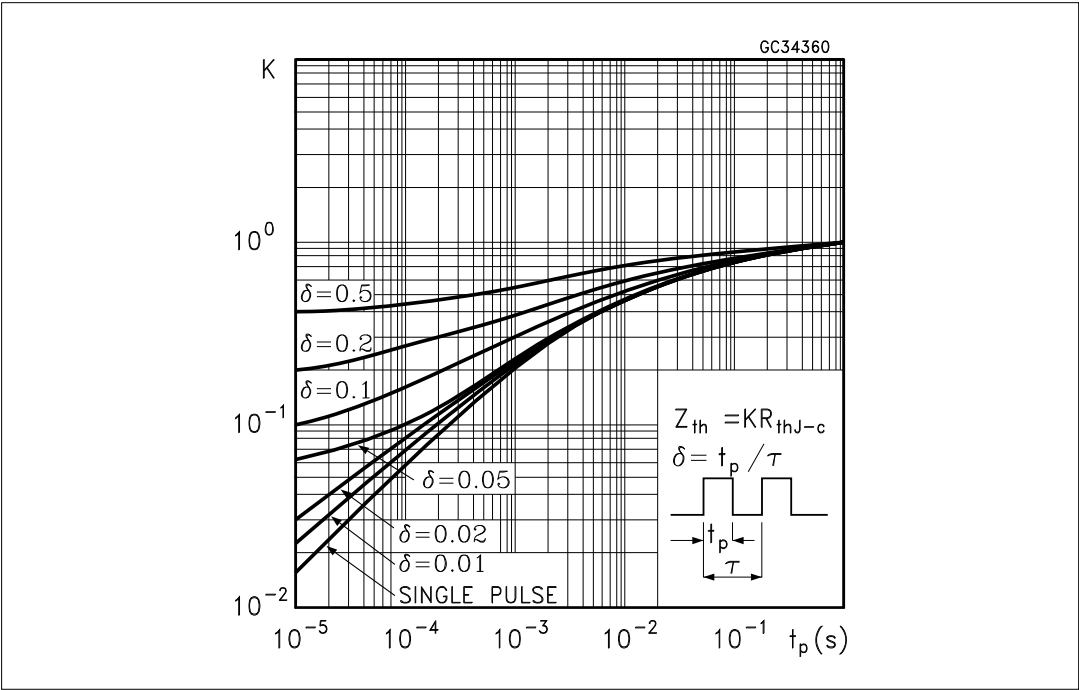


Figure 8. Thermal impedance for DPAK / IPAK



2.4 Electrical characteristics curves

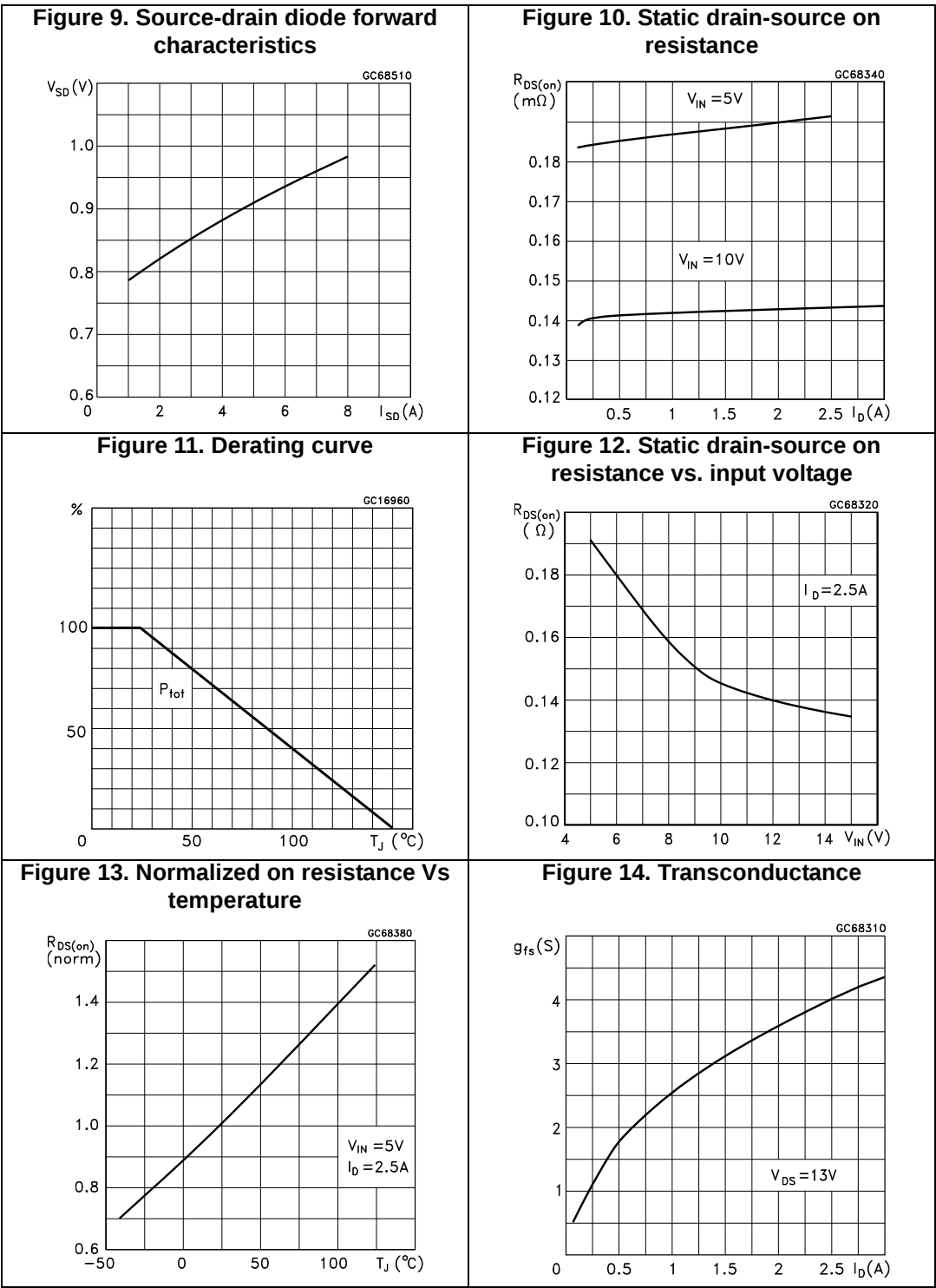


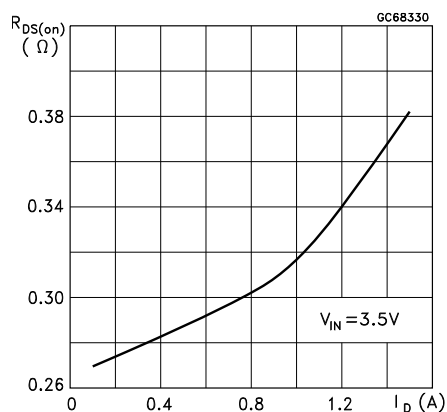
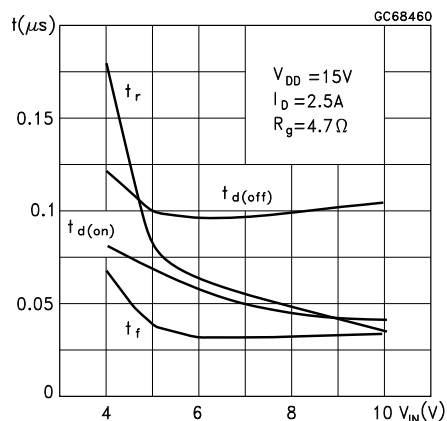
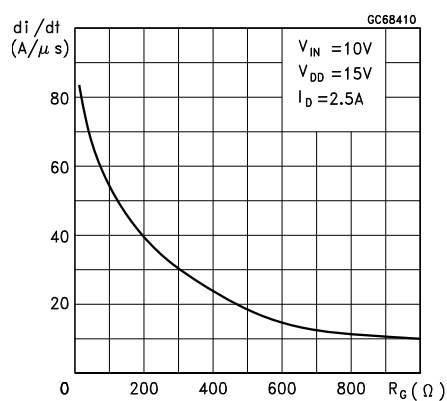
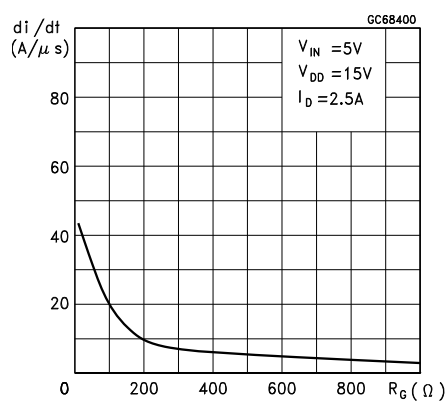
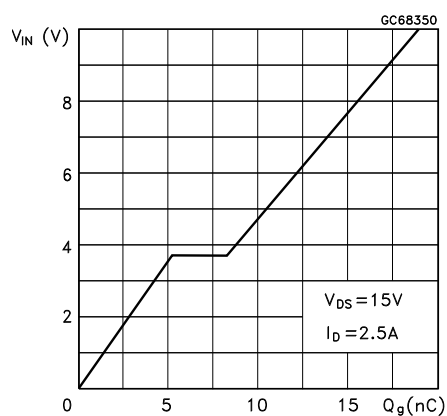
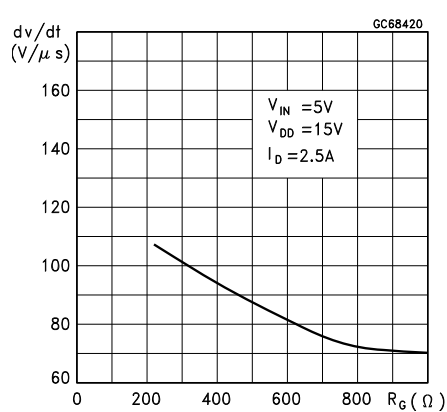
Figure 15. Static drain-source on resistance Vs. Id**Figure 16. Switching time resistive load****Figure 17. Turn-on current slope ($V_{IN} = 10V$)****Figure 18. Turn-on current slope ($V_{IN} = 5V$)****Figure 19. Input voltage vs. input charge****Figure 20. Turn-off drain source voltage slope**

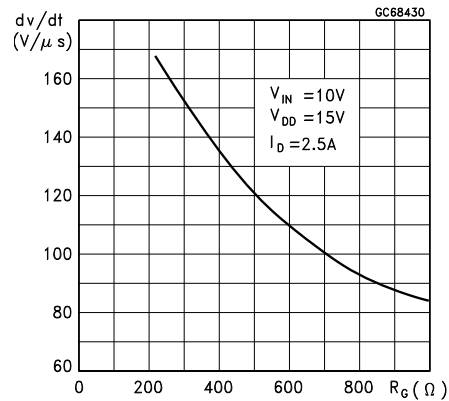
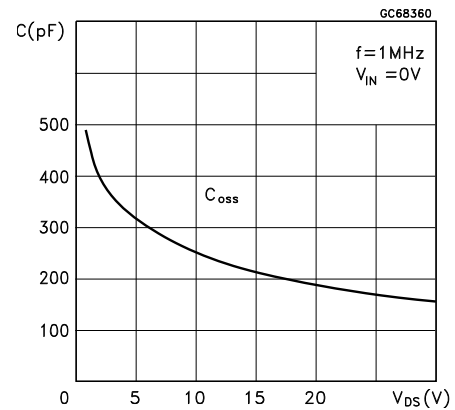
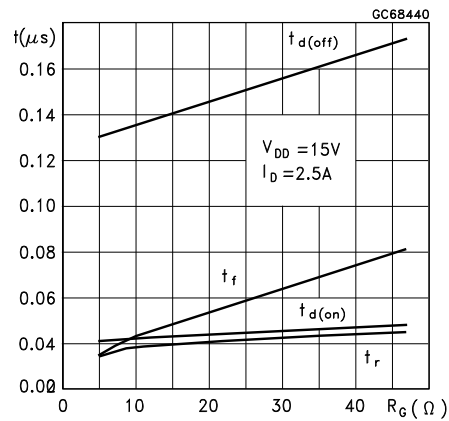
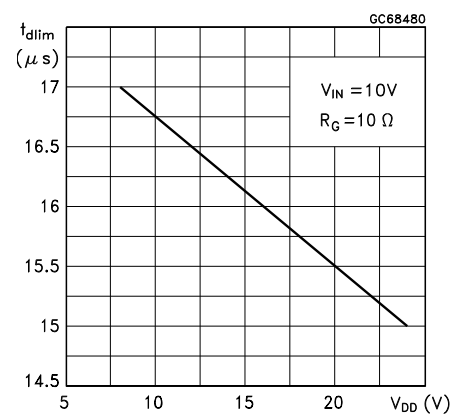
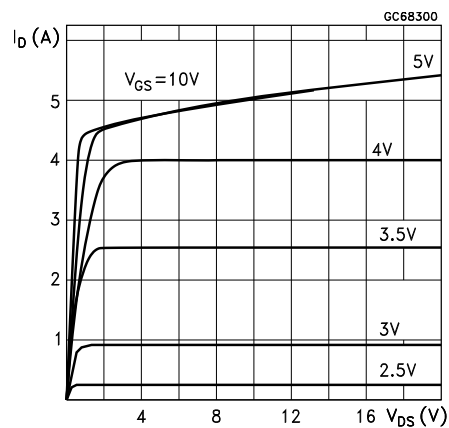
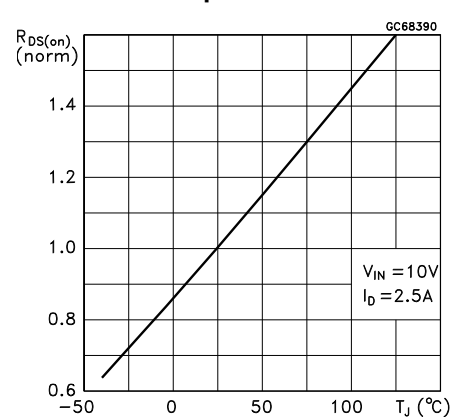
Figure 21. Turn-off drain-source voltage slope**Figure 22. Capacitance variations****Figure 23. Switching time resistive load****Figure 24. Step response current limit****Figure 25. Output characteristics****Figure 26. Normalized on resistance vs. temperature**

Figure 27. Normalized input threshold voltage vs. temperature

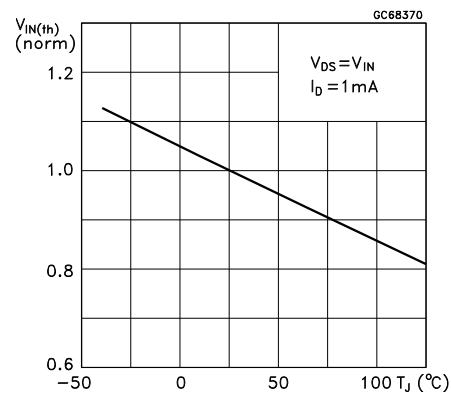
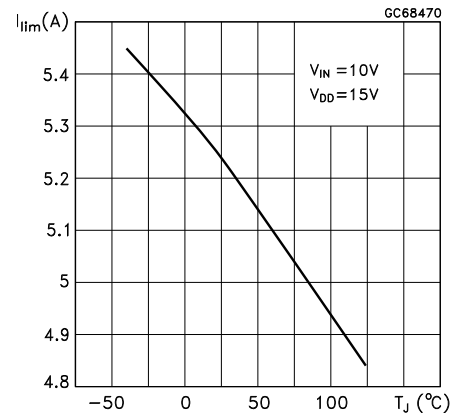


Figure 28. Normalized current limit vs. junction temperature



3 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal Power MOSFET.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC to 50KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

3.1 Overvoltage clamp protection

Internally set at 70 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivaled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

3.2 Linear current limiter circuit

Limits the drain current I_D to I_{lim} whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

3.3 Overtemperature and short circuit protection

These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150 °C. The device is automatically restarted when the chip temperature falls below 135 °C.

3.4 Status feedback

In case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω . The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 DPAK mechanical data

Figure 29. DPAK package dimensions

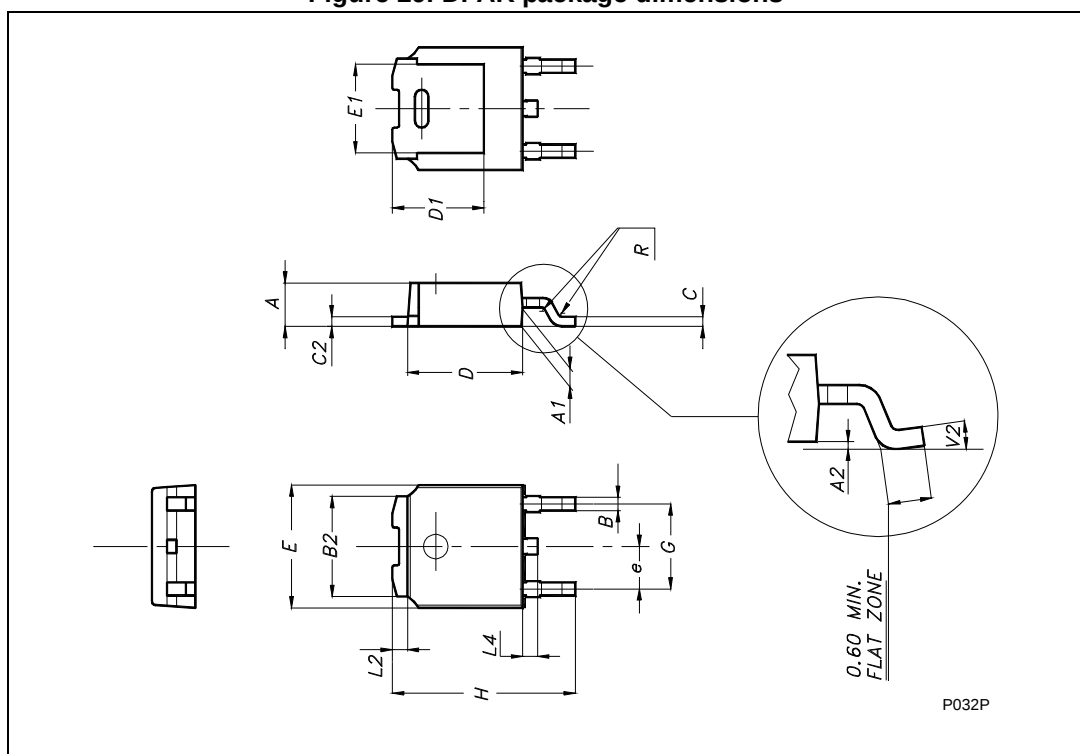


Table 10. DPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package weight	Gr. 0.29		

4.3 IPAK mechanical data

Figure 30. IPAK mechanical data and package outline

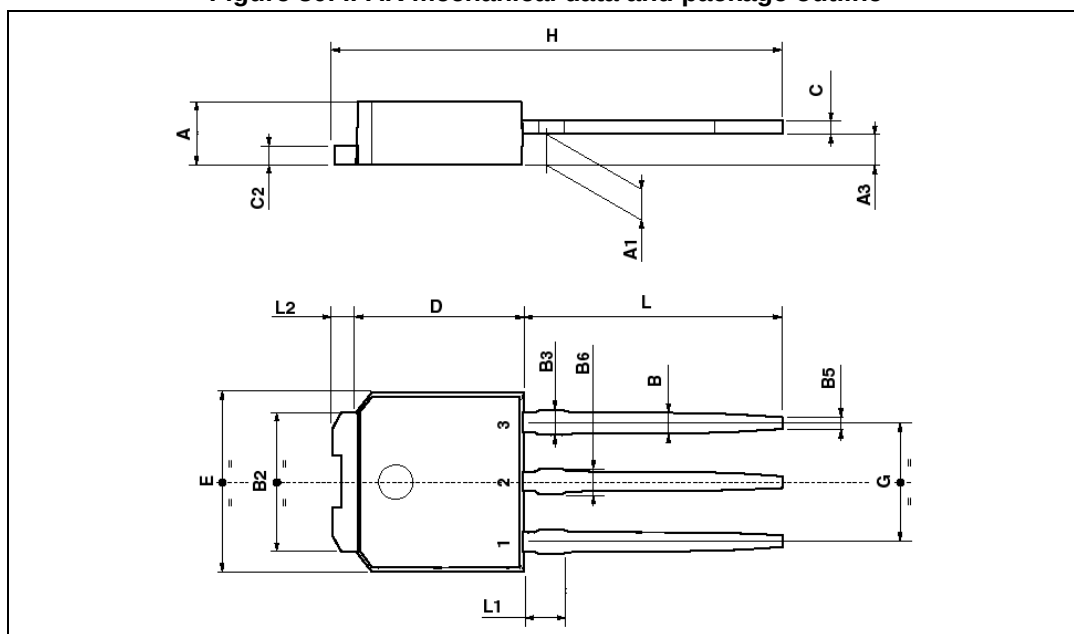


Table 11. IPAK mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A3	0.7		1.3
B	0.64		0.9
B2	5.2		5.4
B3			0.85
B5		0.3	
B6			0.95
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
E	6.4		6.6
G	4.4		4.6
H	15.9		16.3
L	9		9.4
L1	0.8		1.2
L2		0.8	1

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
01-Aug-2013	1	Initial release.
16-Sep-2013	2	Updated disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com