

# Decade Counter

## MC14017B

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

### Features

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage Range (DC or Transient)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient) per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 1)	500	mW
T <sub>A</sub>	Ambient Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

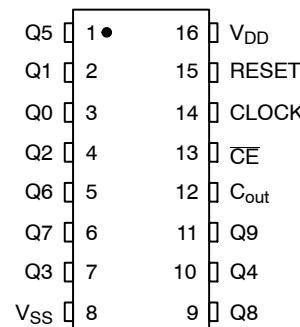
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

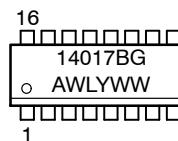


SOIC-16  
D SUFFIX  
CASE 751B

### PIN ASSIGNMENT



### MARKING DIAGRAM



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G = Pb-Free Indicator

### ORDERING INFORMATION

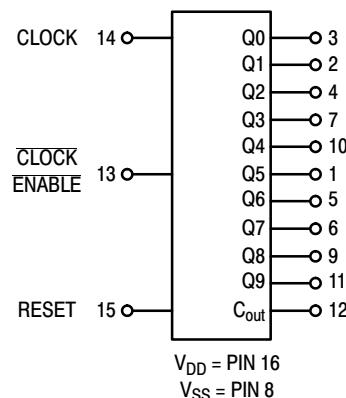
See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

## FUNCTIONAL TRUTH TABLE (Positive Logic)

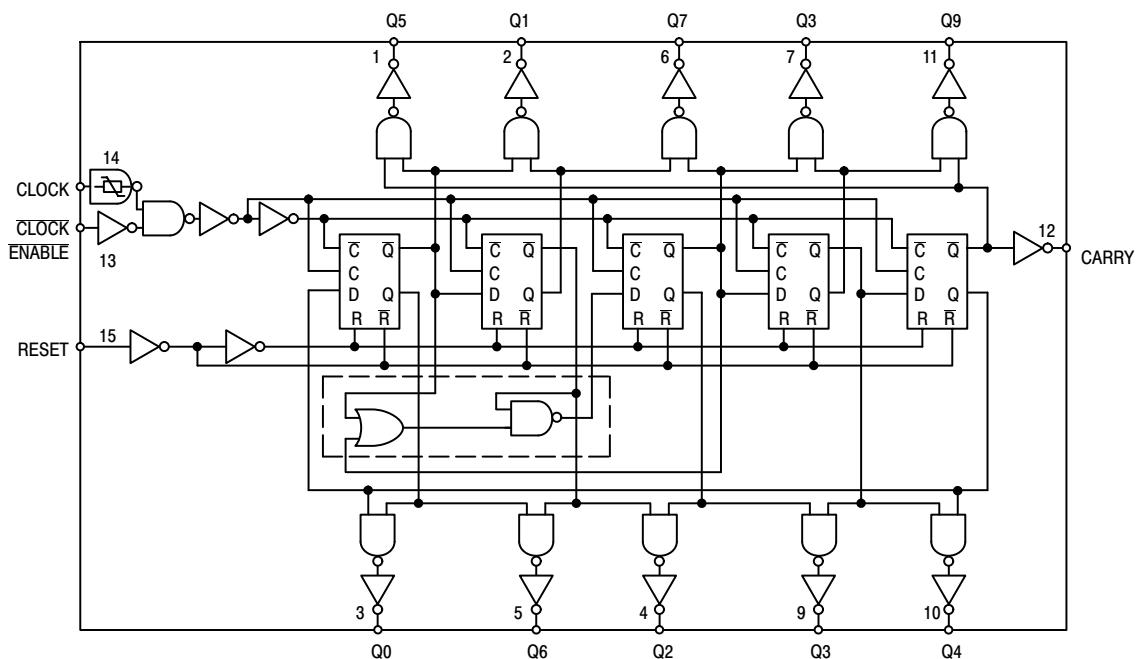
Clock	Clock Enable	Reset	Decode Output=n
0	X	0	n
X	1	0	n
X	X	1	Q0
✓	0	0	n+1
✓	X	0	n
X	✓	0	n
1	✓	0	n+1

X = Don't Care. If n < 5 Carry = "1",  
Otherwise = "0".

## BLOCK DIAGRAM



## LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	V <sub>OH</sub>	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	V <sub>IH</sub>	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	-3.0	–	-2.4	-4.2	–	-1.7	mA
			5.0	-0.64	–	-0.51	-0.88	–	-0.36	
			10	-1.6	–	-1.3	-2.25	–	-0.9	
			15	-4.2	–	-3.4	-8.8	–	-2.4	
	Sink	I <sub>OL</sub>	5.0	0.64	–	0.51	0.88	–	0.36	mA
			10	1.6	–	1.3	2.25	–	0.9	
			15	4.2	–	3.4	8.8	–	2.4	–
Input Current	I <sub>in</sub>	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	–	5.0	–	0.005	5.0	–	150	μA
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.27 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.55 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.83 μA/kHz) f + I <sub>DD</sub>						μA	
		10								
		15								

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25 °C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.0011.

# MC14017B

## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ \text{C}$ )

Characteristic	Symbol	$V_{DD}$ $V_{dc}$	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Reset to Decode Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Propagation Delay Time Clock to $C_{out}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Propagation Delay Time Clock to Decode Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Turn-Off Delay Time Reset to $C_{out}$ $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Clock Pulse Width	$t_{w(H)}$	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	$f_{cl}$	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	$t_{w(H)}$	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0 10 15	No Limit			—
Clock Enable Setup Time	$t_{su}$	5.0 10 15	350 150 115	175 75 52	— — —	ns
Clock Enable Removal Time	$t_{rem}$	5.0 10 15	420 200 140	260 100 70	— — —	ns

5. The formulas given are for the typical characteristics only at  $25^\circ \text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

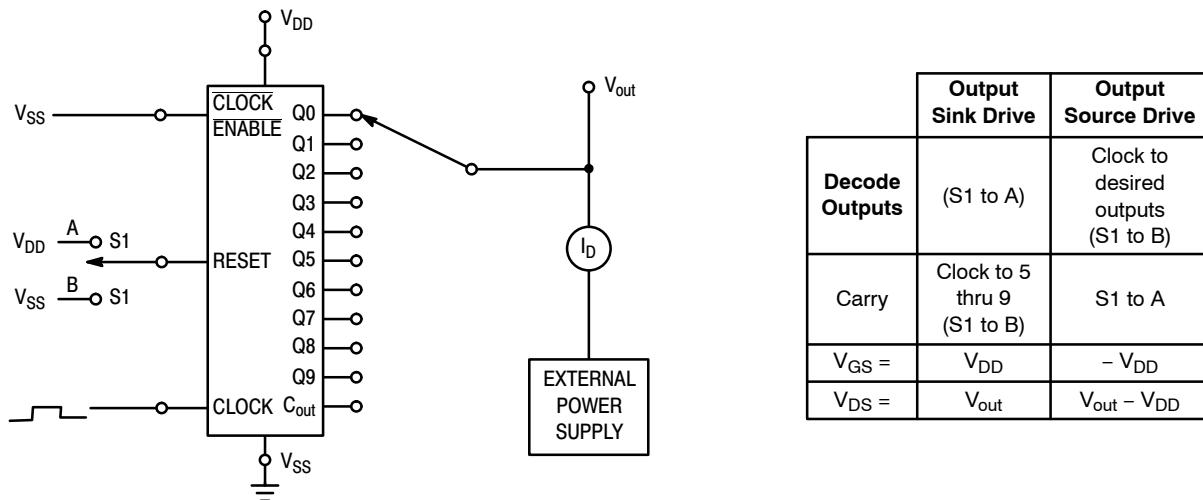


Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

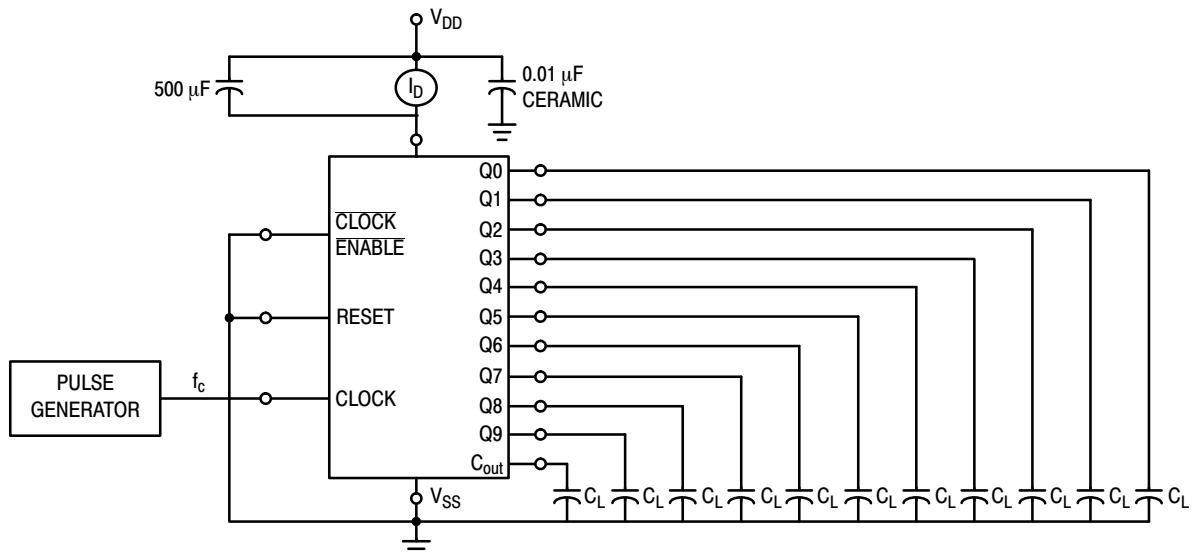
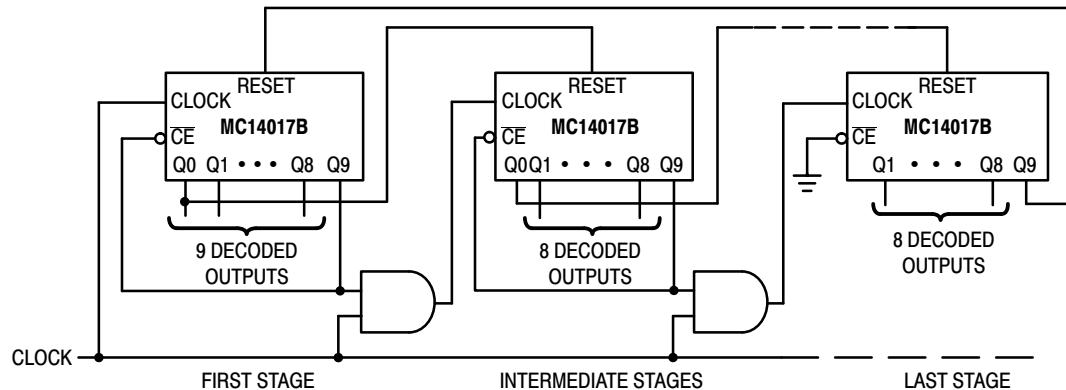


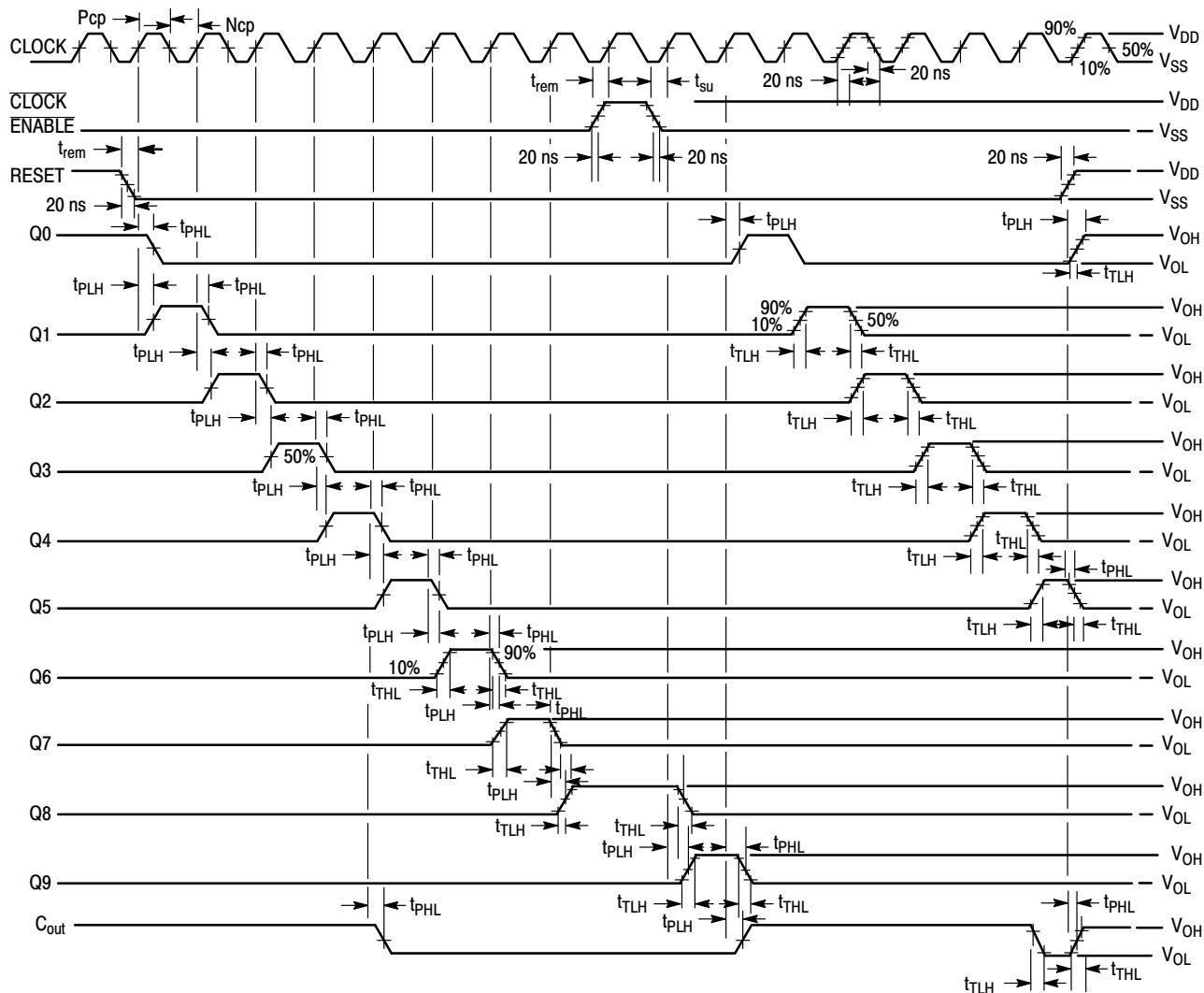
Figure 2. Typical Power Dissipation Test Circuit

## APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



**Figure 3. Counter Expansion**



**Figure 4. AC Measurement Definition and Functional Waveforms**

# MC14017B

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14017BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14017BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14017BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

## DISCONTINUED (Note 7)

Device	Package	Shipping <sup>†</sup>
NLV14017BDG	SOIC-16 (Pb-Free)	48 Units / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#)

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

7. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](#).

**REVISION HISTORY**

Revision	Description of Changes	Date
10	NLV14017BDG OPN Marked as Discontinued + Rebranded the Data Sheet to <b>onsemi</b> format	8/26/2025

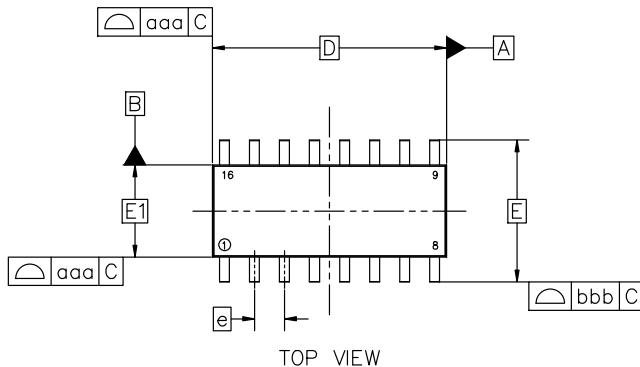
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.


**SOIC-16 9.90x3.90x1.37 1.27P**  
CASE 751B  
ISSUE M

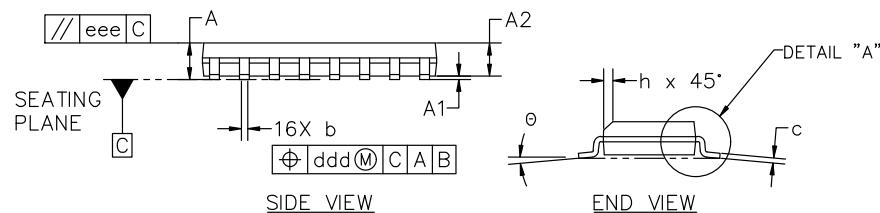
DATE 18 OCT 2024

## NOTES:

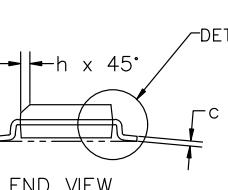
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



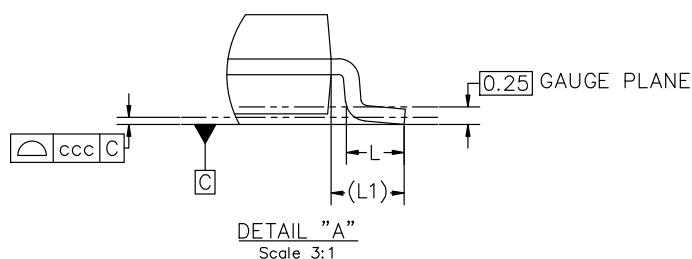
TOP VIEW



SIDE VIEW



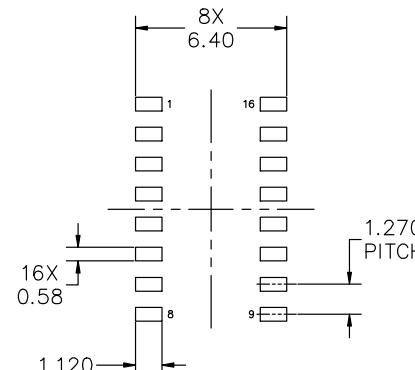
END VIEW

Detail "A"  
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°

TOLERANCE OF FORM AND POSITION	
aaa	0.10
bbb	0.20
ccc	0.10
ddd	0.25
eee	0.10



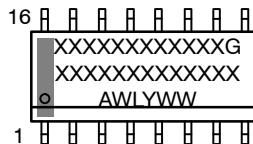
## RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE onsemi SOLDERING  
AND MOUNTING TECHNIQUES REFERENCE  
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DESCRIPTION:	SOIC-16 9.90x3.90x1.37 1.27P	PAGE 1 OF 2

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**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot

Y = Year

WW = Work Week

G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**  
 PIN 1. COLLECTOR  
 2. BASE  
 3. Emitter  
 4. NO CONNECTION  
 5. Emitter  
 6. BASE  
 7. COLLECTOR  
 8. COLLECTOR  
 9. BASE  
 10. Emitter  
 11. NO CONNECTION  
 12. Emitter  
 13. BASE  
 14. COLLECTOR  
 15. Emitter  
 16. COLLECTOR

**STYLE 2:**  
 PIN 1. CATHODE  
 2. ANODE  
 3. NO CONNECTION  
 4. CATHODE  
 5. CATHODE  
 6. NO CONNECTION  
 7. ANODE  
 8. CATHODE  
 9. CATHODE  
 10. ANODE  
 11. NO CONNECTION  
 12. CATHODE  
 13. CATHODE  
 14. NO CONNECTION  
 15. ANODE  
 16. CATHODE

**STYLE 3:**  
 PIN 1. COLLECTOR, DYE #1  
 2. BASE, #1  
 3. Emitter, #1  
 4. COLLECTOR, #1  
 5. COLLECTOR, #2  
 6. BASE, #2  
 7. Emitter, #2  
 8. COLLECTOR, #2  
 9. COLLECTOR, #3  
 10. BASE, #3  
 11. Emitter, #3  
 12. COLLECTOR, #3  
 13. COLLECTOR, #4  
 14. BASE, #4  
 15. Emitter, #4  
 16. COLLECTOR, #4

**STYLE 4:**  
 PIN 1. COLLECTOR, DYE #1  
 2. COLLECTOR, #1  
 3. COLLECTOR, #2  
 4. COLLECTOR, #2  
 5. COLLECTOR, #3  
 6. COLLECTOR, #3  
 7. COLLECTOR, #4  
 8. COLLECTOR, #4  
 9. BASE, #4  
 10. Emitter, #4  
 11. BASE, #3  
 12. Emitter, #3  
 13. BASE, #2  
 14. Emitter, #2  
 15. BASE, #1  
 16. Emitter, #1

**STYLE 5:**  
 PIN 1. DRAIN, DYE #1  
 2. DRAIN, #1  
 3. DRAIN, #2  
 4. DRAIN, #2  
 5. DRAIN, #3  
 6. DRAIN, #3  
 7. DRAIN, #4  
 8. DRAIN, #4  
 9. GATE, #4  
 10. SOURCE, #4  
 11. GATE, #3  
 12. SOURCE, #3  
 13. GATE, #2  
 14. SOURCE, #2  
 15. GATE, #1  
 16. SOURCE, #1

**STYLE 6:**  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. CATHODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE  
 15. ANODE  
 16. ANODE

**STYLE 7:**  
 PIN 1. SOURCE N-CH  
 2. COMMON DRAIN (OUTPUT)  
 3. COMMON DRAIN (OUTPUT)  
 4. GATE P-CH  
 5. COMMON DRAIN (OUTPUT)  
 6. COMMON DRAIN (OUTPUT)  
 7. COMMON DRAIN (OUTPUT)  
 8. SOURCE P-CH  
 9. SOURCE P-CH  
 10. COMMON DRAIN (OUTPUT)  
 11. COMMON DRAIN (OUTPUT)  
 12. COMMON DRAIN (OUTPUT)  
 13. GATE N-CH  
 14. COMMON DRAIN (OUTPUT)  
 15. COMMON DRAIN (OUTPUT)  
 16. SOURCE N-CH

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<b>DESCRIPTION:</b>	SOIC-16 9.90x3.90X1.37 1.27P	<b>PAGE 2 OF 2</b>

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