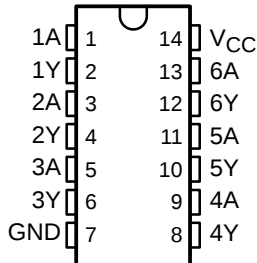


SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

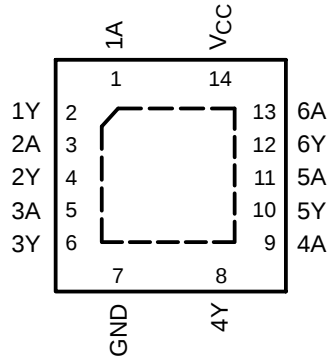
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- Operate From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages Up to 5.5 V
- Max t_{pd} of 2.6 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

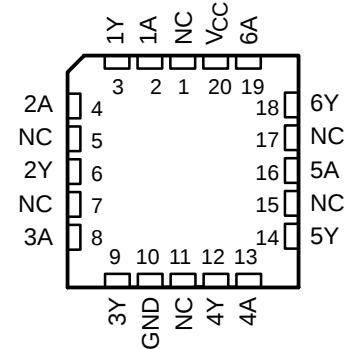
SN54LVC07A ... J OR W PACKAGE
SN74LVC07A ... D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC07A ... RGY PACKAGE
(TOP VIEW)



SN54LVC07A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These hex buffers/drivers are designed for 1.65-V to 5.5-V V_{CC} operation.

The outputs of the 'LVC07A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of these devices as translators in a mixed-system environment.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC07ARGYR	LC07A
	SOIC – D	Tube of 50	SN74LVC07AD	LVC07A
		Reel of 2500	SN74LVC07ADR	
		Reel of 250	SN74LVC07ADT	
	SOP – NS	Reel of 2000	SN74LVC07ANSR	LVC07A
	SSOP – DB	Reel of 2000	SN74LVC07ADBR	LC07A
	TSSOP – PW	Tube of 90	SN74LVC07APW	LC07A
		Reel of 2000	SN74LVC07APWR	
		Reel of 250	SN74LVC07APWT	
TVSOP – DGV	Reel of 2000	SN74LVC07ADGVR	LC07A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC07AJ	SNJ54LVC07AJ
	CFP – W	Tube of 150	SNJ54LVC07AW	SNJ54LVC07AW
	LCCC – FK	Tube of 55	SNJ54LVC07AFK	SNJ54LVC07AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

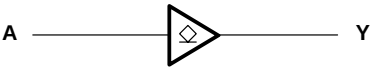
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FUNCTION TABLE
(each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L

logic diagram, each buffer/driver (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O	–0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		SN54LVC07A		SN74LVC07A		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage		1.65	5.5	1.65	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		0.3 × V _{CC}		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	5.5	0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		mA
		V _{CC} = 2.3 V	12		12		
		V _{CC} = 2.7 V	12		12		
		V _{CC} = 3 V	24		24		
		V _{CC} = 4.5 V	24		24		
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC07A			SN74LVC07A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V			0.2			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45			0.45	
	I _{OL} = 12 mA	2.3 V			0.7			0.7	
		2.7 V			0.4			0.4	
	I _{OL} = 24 mA	3 V			0.55			0.55	
		4.5 V							
I _I	V _I = 5.5 V or GND	3.6 V			±5			±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10			10	μA
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500			500	μA
C _i	V _I = V _{CC} or GND	3.3 V			5			5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN54LVC07A, SN74LVC07A

HEX BUFFERS/DRIVERS

WITH OPEN-DRAIN OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC07A										UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	3.5	1	2.8		3	1	2.9	1	2.6	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

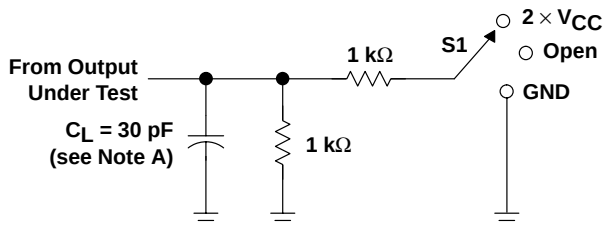
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC07A										UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	3.5	1	2.8	3		1	2.9	1	2.6	ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	$f = 10\text{ MHz}$	1.8	2	2.5	3.78	pF

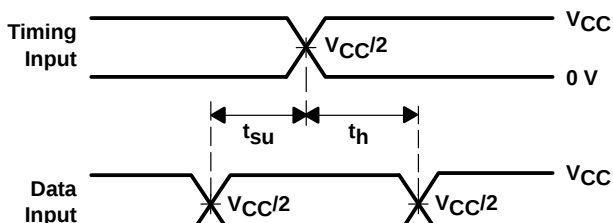
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

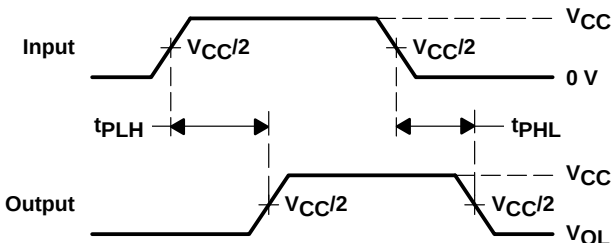


LOAD CIRCUIT

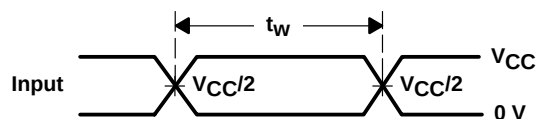
TEST	S1
t_{pZL} (see Note F)	$2 \times V_{CC}$
t_{pLZ} (see Note G)	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	$2 \times V_{CC}$



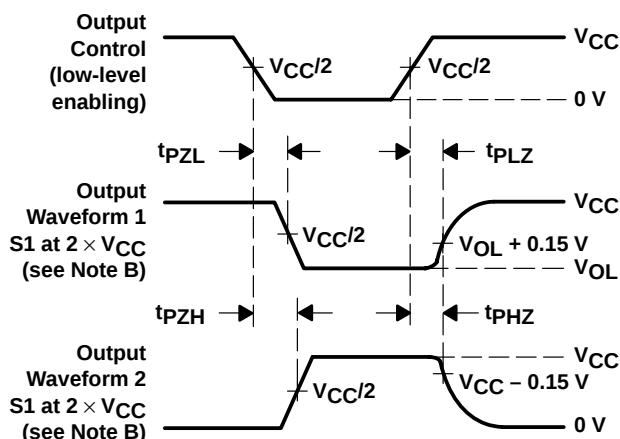
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at $V_{CC}/2$.
 - t_{pLZ} is measured at $V_{OL} + 0.15 \text{ V}$.
 - All parameters and waveforms are not applicable to all devices.

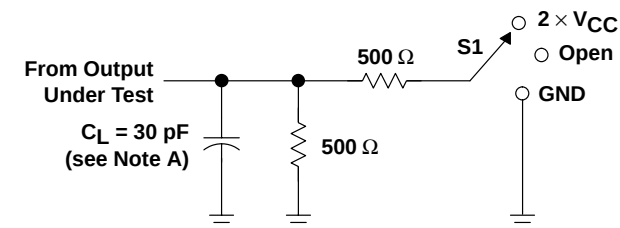
Figure 1. Load Circuit and Voltage Waveforms

SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCAS595N – OCTOBER 1997 – REVISED JULY 2003

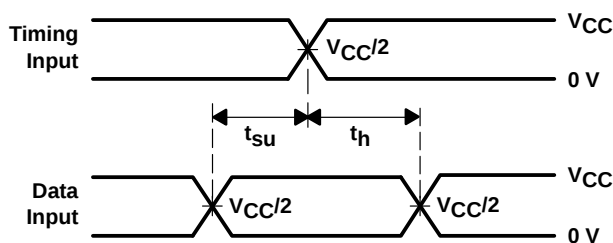
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

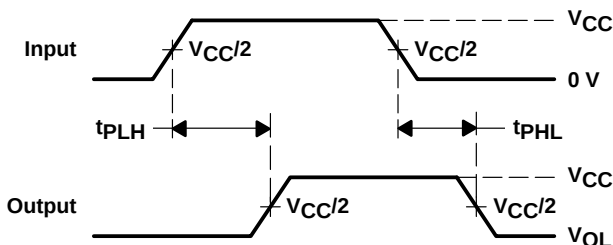


LOAD CIRCUIT

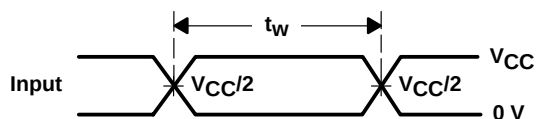
TEST	S1
t_{pZL} (see Note F)	2 $\times V_{CC}$
t_{pLZ} (see Note G)	2 $\times V_{CC}$
t_{PHZ}/t_{PHZ}	2 $\times V_{CC}$



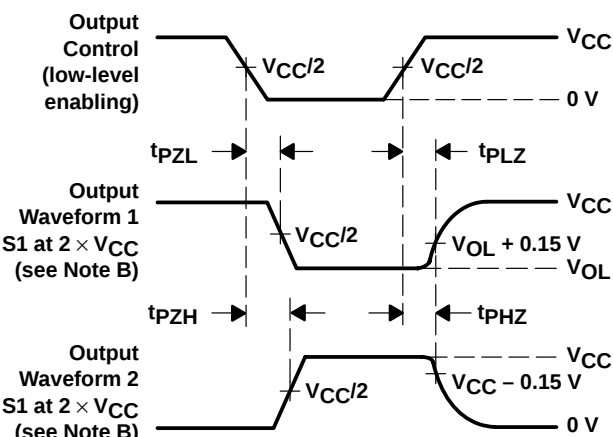
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



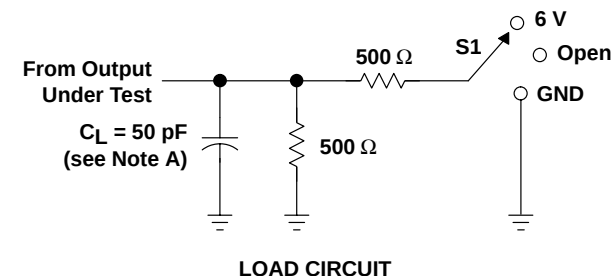
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at $V_{CC}/2$.
 - t_{pLZ} is measured at $V_{OL} + 0.15 \text{ V}$.
 - All parameters and waveforms are not applicable to all devices.

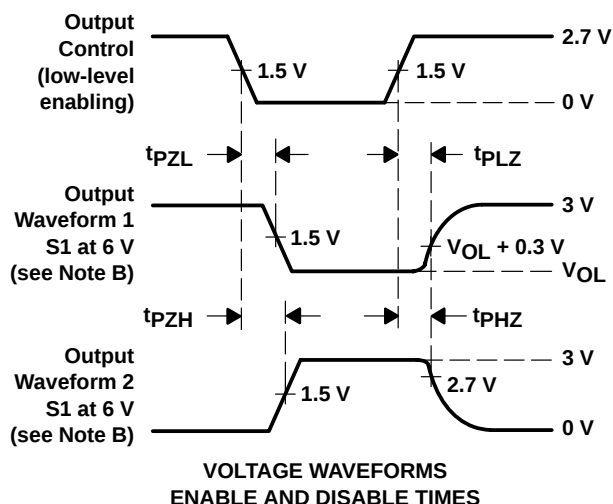
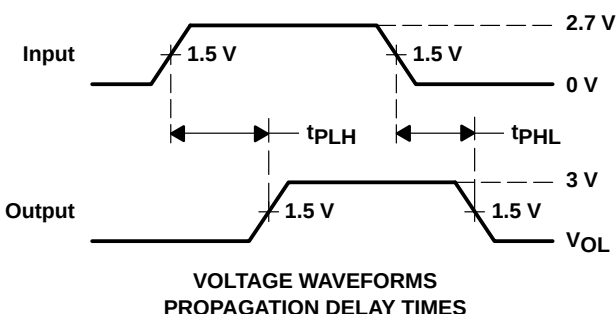
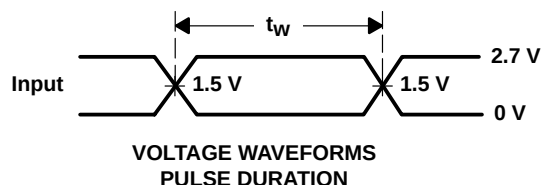
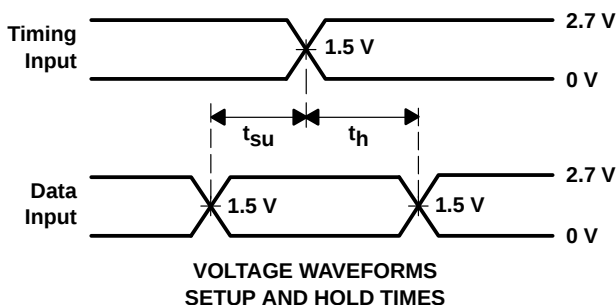
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



TEST	S1
t_{PZL} (see Note F)	6 V
t_{PLZ} (see Note G)	6 V
t_{PHZ}/t_{PHL}	6 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 - F. t_{PZL} is measured at 1.5 V.
 - G. t_{PLZ} is measured at $V_{OL} + 0.3 \text{ V}$.
 - H. All parameters and waveforms are not applicable to all devices.

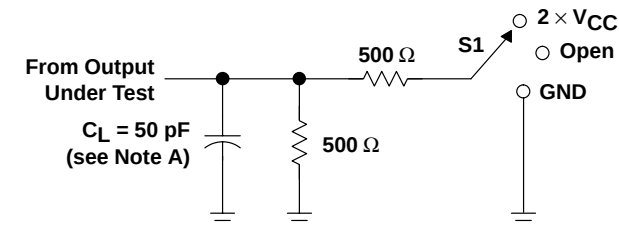
Figure 3. Load Circuit and Voltage Waveforms

SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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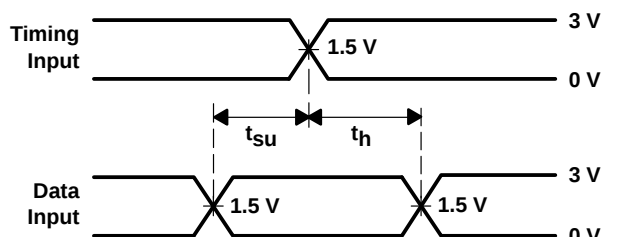
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$$

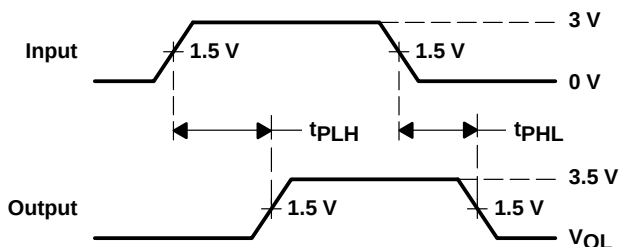


LOAD CIRCUIT

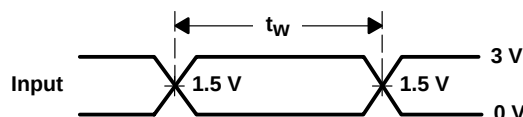
TEST	S1
t_{pZL} (see Note F)	$2 \times V_{CC}$
t_{pLZ} (see Note G)	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	7 V



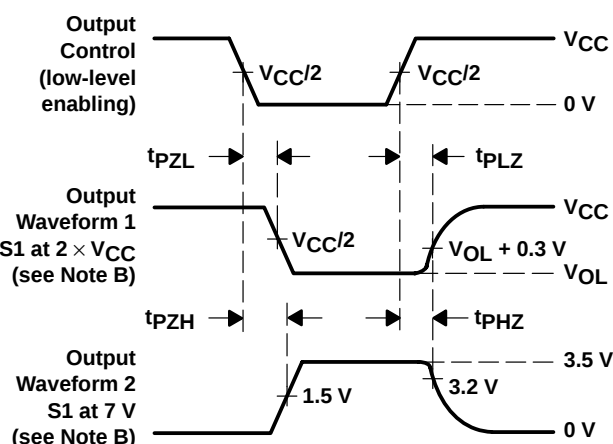
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at $V_{CC}/2$.
 - t_{pLZ} is measured at $V_{OL} + 0.3\text{ V}$.
 - All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

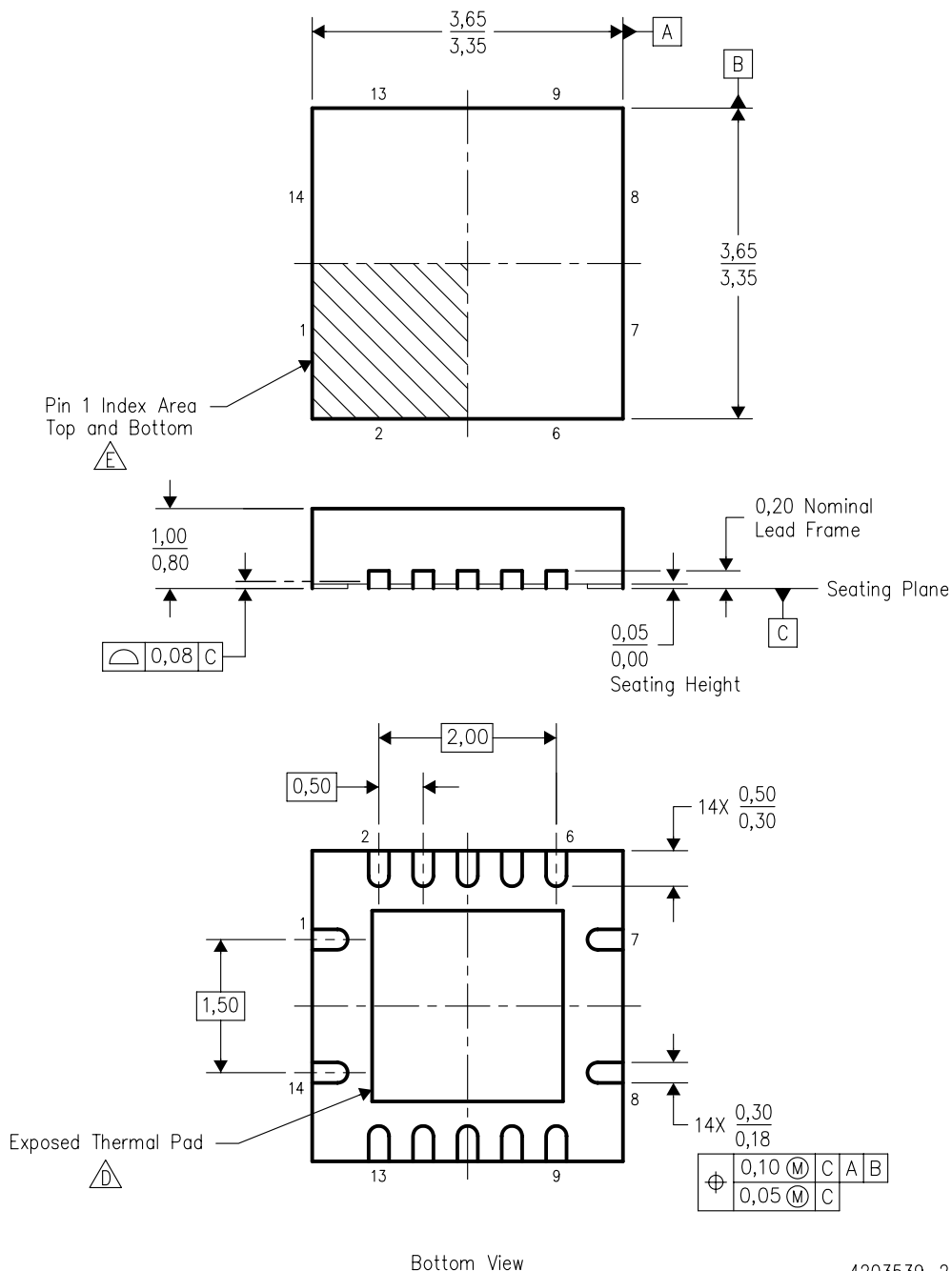
PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/F 07/2004

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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