BLF8G27LS-140

Power LDMOS transistor

Rev. 2 — 5 June 2013

Product data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for base station applications at frequencies from 2500 MHz to 2700 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25$ °C in a common source class-AB production test circuit.

Test signal	f	I _{Dq}	V_{DS}	P _{L(AV)}	Gp	η_{D}	ACPR
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	2600 to 2700	1300	32	45	17.4	32	-30 <u>[1]</u>
2-carrier W-CDMA	2600 to 2700	1300	28	35	17.0	29	-31 [<u>1]</u>

^[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

RF power amplifier for W-CDMA base stations and multi carrier applications in the 2500 MHz to 2700 MHz frequency range



2. Pinning information

Table 2. Pinning

	3			
Pin	Description	Siı	mplified outline	Graphic symbol
1	drain			,
2	gate		1 1	ئے
3	source [1]	<u>[1]</u>	2	2
				3 sym112

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	Package				
	Name	Description	Version			
BLF8G27LS-140	-	earless flanged ceramic package; 2 leads	SOT502B			

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V _{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		<u>[1]</u> _	225	°C

^[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 55 W	0.27	K/W

6. Characteristics

Table 6. DC characteristics

 $T_i = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS} \\$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 2.16 \text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_{D} = 216 \text{ mA}$	1.5	1.9	2.3	V
I _{DSS}	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	4.5	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	40	-	Α
I _{GSS}	gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	450	nΑ
9 _{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_{D} = 10.8 \text{ A}$	-	16	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 7.56 \text{ A}$	-	0.06	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR 8.4 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; f_1 = 2622.5 MHz; f_2 = 2627.5 MHz; f_3 = 2682.5 MHz; f_4 = 2687.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 1300 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	$P_{L(AV)} = 45 \text{ W}$	15.8	17.4	-	dB
RLin	input return loss	$P_{L(AV)} = 45 \text{ W}$	-	-18	-8	dB
η_{D}	drain efficiency	$P_{L(AV)} = 45 \text{ W}$	27	32	-	%
ACPR _{5M}	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 45 \text{ W}$	-	-30	-27	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G27LS-140 is capable to withstand a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 1300 mA; P_{L} = 180 W (CW); f = 2620 MHz.

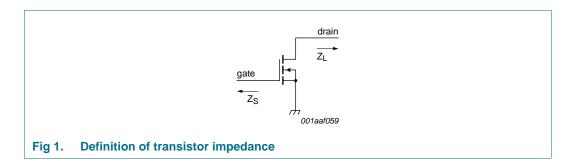
7.2 Impedance information

Table 8. Typical impedance

 $I_{Da} = 1300 \text{ mA}; V_{DS} = 32 \text{ V}.$

29		
f	Z _S [1]	Z _L [1]
(MHz)	(Ω)	(Ω)
2600	2.30 - j4.90	1.40 – j3.10
2700	3.80 – j4.50	1.40 – j3.10

^[1] Z_S and Z_L defined in Figure 1.



7.3 Test circuit

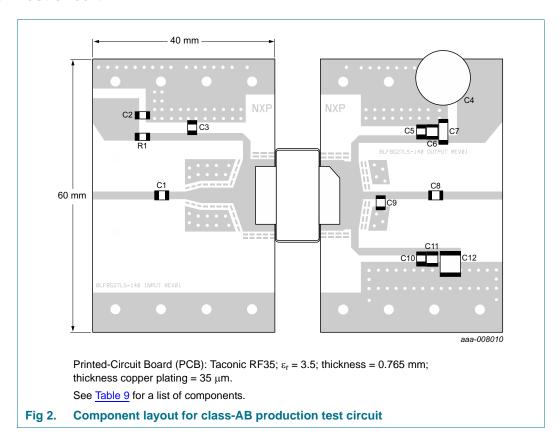


Table 9. List of components

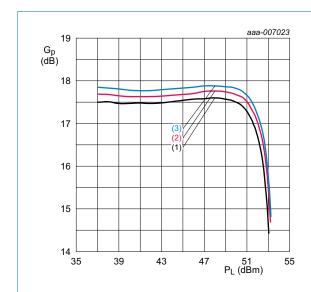
For test circuit see Figure 2.

Component	Description	Value		Remarks
C1, C3, C5, C8, C10	multilayer ceramic chip capacitor	10 pF	<u>[1]</u>	ATC100B
C2	multilayer ceramic chip capacitor	1 μF, 25 V	[2]	Murata
C4	electrolytic capacitor	470 μF, 63 V		
C6, C11	multilayer ceramic chip capacitor	1 μF, 50 V	[2]	Murata
C7, C12	multilayer ceramic chip capacitor	10 μF, 50 V	[2]	Murata
C9	multilayer ceramic chip capacitor	0.5 pF	<u>[1]</u>	ATC100B
R1	chip resistor	$3.9~\Omega$, 1% tolerance		Philips SMD 1206

- [1] American Technical Ceramics type 100B or capacitor of same quality.
- [2] Murata or capacitor of same quality.

7.4 Graphical data

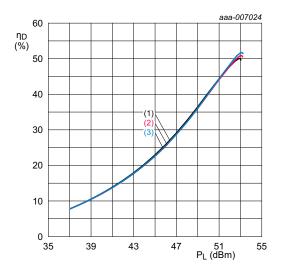
7.4.1 Pulsed CW



 $V_{DS}=32$ V; $I_{Dq}=1300$ mA; f=860 MHz; $t_p=100~\mu s;$ $\delta=10$ %.

- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

Fig 3. Power gain as a function of output power; typical values

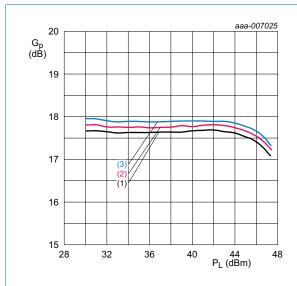


 V_{DS} = 32 V; I_{Dq} = 1300 mA; f = 860 MHz; t_p = 100 $\mu s;$ δ = 10 %.

- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

Fig 4. Drain efficiency as a function of output power; typical values

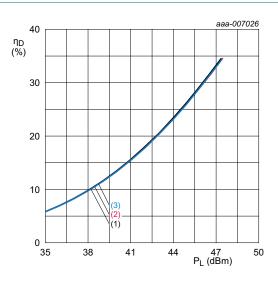
7.4.2 IS-95



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

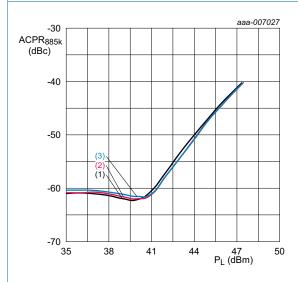
Fig 5. Power gain as a function of output power; typical values



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

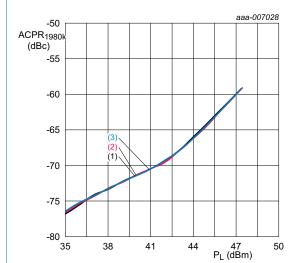
Fig 6. Drain efficiency as a function of output power; typical values



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

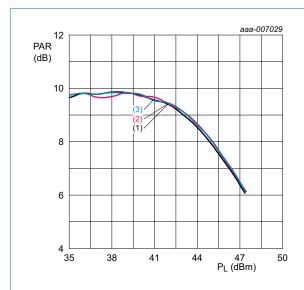
- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

Fig 7. Adjacent channel power ratio (885 kHz) as a function of output power; typical values



- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

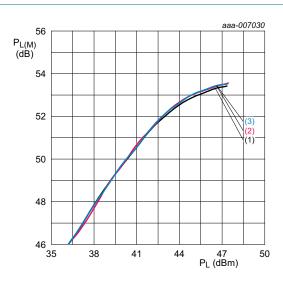
Fig 8. Adjacent channel power ratio (1980 kHz) as a function of output power; typical values



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

Fig 9. Peak-to-average power ratio as a function of output power; typical values

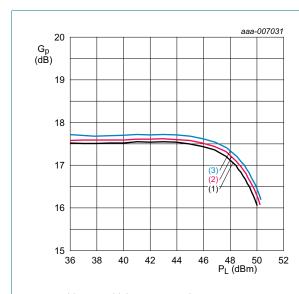


 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2620 MHz
- (2) f = 2655 MHz
- (3) f = 2690 MHz

Fig 10. Peak output power as a function of output power; typical values

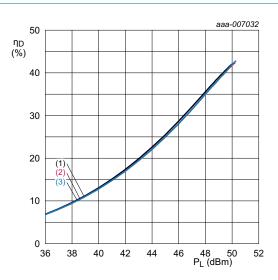
7.4.3 1-Carrier W-CDMA



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

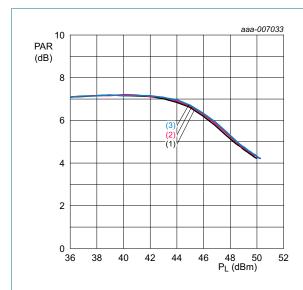
- (1) f = 2622.5 MHz
- (2) f = 2655 MHz
- (3) f = 2687.5 MHz

Fig 11. Power gain as a function of output power; typical values



- (1) f = 2622.5 MHz
- (2) f = 2655 MHz
- (3) f = 2687.5 MHz

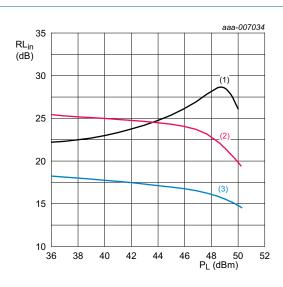
Fig 12. Drain efficiency as a function of output power; typical values



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2622.5 MHz
- (2) f = 2655 MHz
- (3) f = 2687.5 MHz

Fig 13. Peak-to-average power ratio as a function of output power; typical values

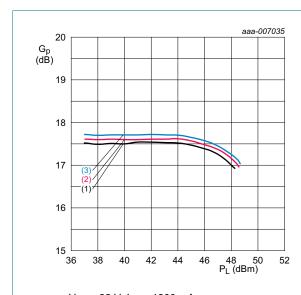


 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2622.5 MHz
- (2) f = 2655 MHz
- (3) f = 2687.5 MHz

Fig 14. Input return loss as a function of output power; typical values

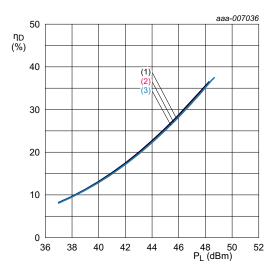
7.4.4 2-Carrier W-CDMA



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

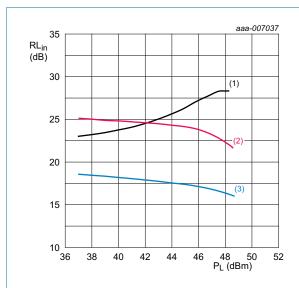
- (1) f = 2625 MHz
- (2) f = 2655 MHz
- (3) f = 2685 MHz

Fig 15. Power gain as a function of output power; typical values



- (1) f = 2625 MHz
- (2) f = 2655 MHz
- (3) f = 2685 MHz

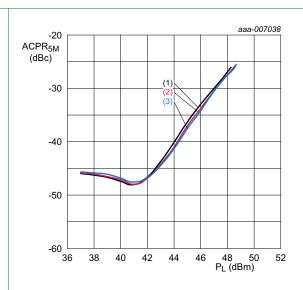
Fig 16. Drain efficiency as a function of output power; typical values



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2625 MHz
- (2) f = 2655 MHz
- (3) f = 2685 MHz

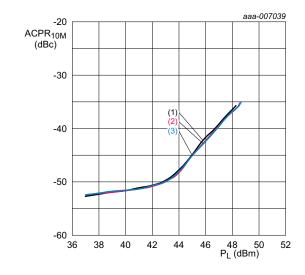
Fig 17. Input return loss as a function of output power; typical values



 $V_{DS} = 32 \text{ V}; I_{Dq} = 1300 \text{ mA}.$

- (1) f = 2625 MHz
- (2) f = 2655 MHz
- (3) f = 2685 MHz

Fig 18. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



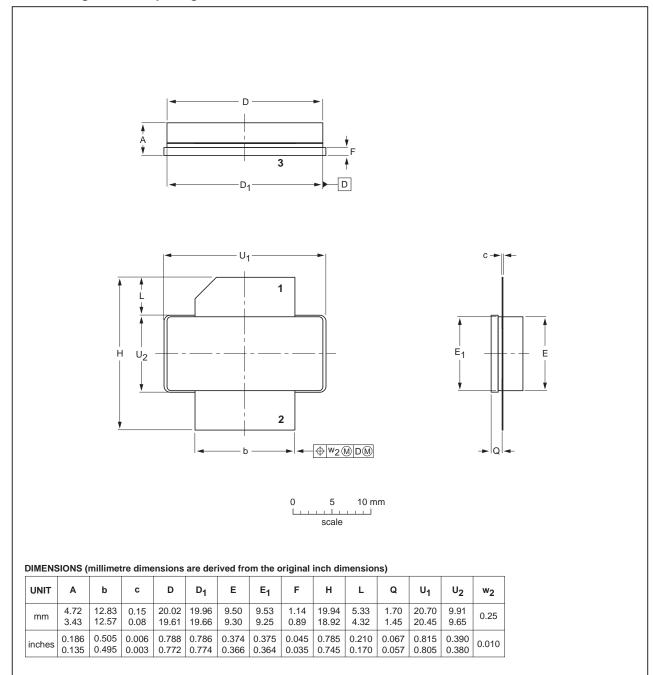
- (1) f = 2625 MHz
- (2) f = 2655 MHz
- (3) f = 2685 MHz

Fig 19. Adjacent channel power ratio (10 MHz) as a function of output power; typical values

8. Package outline

Earless flanged ceramic package; 2 leads

SOT502B



OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT502B					-07-05-09 12-05-02	

Fig 20. Package outline SOT502B

BLF8G27LS-140

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
BLF8G27LS-140 v.2	20130605	Product data sheet	-	BLF8G27LS-140 v.1			
Modifications:	Modifications: • Table 7 on page 3: table has been updated.						
	 Section 7.2 or 	n page 3: section has been	added.				
 Section 7.3 on page 4: section has been added. 							
BLF8G27LS-140 v.1	20130328	Objective data sheet	-	-			

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

BLF8G27LS-140

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

BLF8G27LS-140

Power LDMOS transistor

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1	Product profile
1.1	General description 1
1.2	Features and benefits 1
1.3	Applications
2	Pinning information 2
3	Ordering information 2
4	Limiting values
5	Thermal characteristics 2
6	Characteristics
7	Test information
7.1	Ruggedness in class-AB operation 3
7.2	Impedance information
7.3	Test circuit4
7.4	Graphical data 5
7.4.1	Pulsed CW
7.4.2	IS-956
7.4.3	1-Carrier W-CDMA
7.4.4	2-Carrier W-CDMA 8
8	Package outline
9	Handling information 11
10	Abbreviations
11	Revision history 11
12	Legal information
12.1	Data sheet status
12.2	Definitions
12.3	Disclaimers
12.4	Trademarks
13	Contact information
14	Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

BLF8G27LS-140,118 BLF8G27LS-140,112