Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

October 2015

FDMD8530

Dual N-Channel PowerTrench® MOSFET

Q1: 30 V, 201 A, 1.25 mΩ Q2: 30 V, 201 A, 1.25 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 1.25 mΩ at V_{GS} = 10 V, I_D = 35 A
- Max $r_{DS(on)}$ = 1.5 mΩ at V_{GS} = 4.5 V, I_D = 32 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.25 mΩ at V_{GS} = 10 V, I_D = 35 A
- Max $r_{DS(on)}$ = 1.5 mΩ at V_{GS} = 4.5 V, I_D = 32 A
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- RoHS Compliant

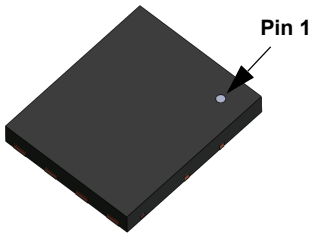
General Description

This device includes two 30V N-Channel MOSFETs in a dual power (5 mm X 6 mm) package. HS source and LS drain internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}$/Qg FOM silicon.

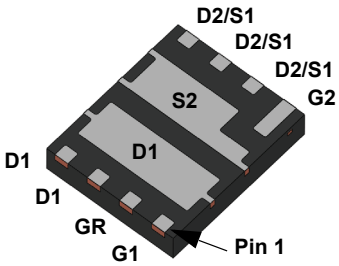
Applications

- POL Synchronous Dual
- One Phase Motor Half Bridge
- Half/Full Bridge Secondary Synchronous Rectification

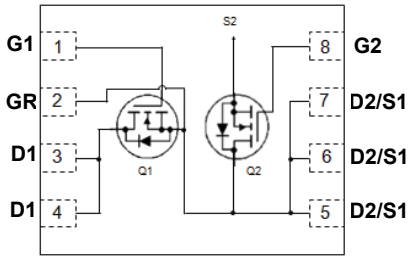
Top



Bottom



Power 5 x 6



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter				Q1	Q2	Units
V_{DS}	Drain to Source Voltage				30	30	V
V_{GS}	Gate to Source Voltage				±20	±20	V
I_D	Drain Current	-Continuous	T_C = 25 °C	(Note 5)	201	201	A
		-Continuous	T_C = 100 °C	(Note 5)	127	127	
	Drain Current	-Continuous	T_A = 25 °C		35[1a]	35[1b]	
		-Pulsed		(Note 4)	1047	1047	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	661	661	mJ
P_D	Power Dissipation		T_C = 25 °C		78	78	W
	Power Dissipation		T_A = 25 °C		2.2[1a]	2.2[1b]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +150		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.6	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	55[1a]	55 [1b]	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMD8530	FDMD8530	Power 5 x 6	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

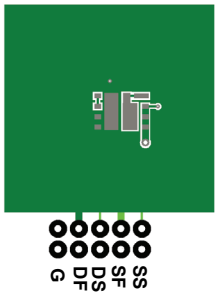
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C	Q1 Q2		20 20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	Q1 Q2	1.0 1.0	1.5 1.5	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C	Q1 Q2		-5 -5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 35 A	Q1		0.77	1.25	mΩ
		V_{GS} = 4.5 V, I_D = 32 A			0.96	1.5	
		V_{GS} = 10 V, I_D = 35 A, T_J = 125 °C			1.1	1.8	
		V_{GS} = 10 V, I_D = 35 A	Q2		0.77	1.25	
		V_{GS} = 4.5 V, I_D = 32 A			0.96	1.5	
		V_{GS} = 10 V, I_D = 35 A, T_J = 125 °C			1.1	1.8	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 35 A	Q1 Q2		259 259		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	Q1 Q2		7425 7425	10395 10395	pF
C_{oss}	Output Capacitance		Q1 Q2		2190 2190	3070 3070	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		220 220	310 310	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	1.9 1.9	3.8 3.8	Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 35 A V_{GS} = 10 V, R_{GEN} = 6 Ω	Q1 Q2		14 14	25 25	ns
t_r	Rise Time		Q1 Q2		13 13	24 24	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		71 71	114 114	ns
t_f	Fall Time		Q1 Q2		21 21	34 34	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D =35 A	Q1 Q2		106 106	149 149	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 15 V, I_D =35 A	Q1 Q2		50 50	70 70	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D =35 A	Q1 Q2		16 16		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 15 V, I_D =35 A	Q1 Q2		13 13		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted.

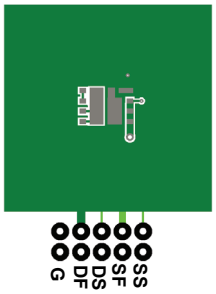
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 35 A (Note 2)	Q1 Q2		0.8 0.8	1.3 1.3	V
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	Q1 Q2		0.7 0.7	1.2 1.2	V
t_{rr}	Reverse Recovery Time	I_F = 35 A, di/dt = 100 A/μs	Q1 Q2		54 54	87 87	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2		39 39	63 63	nC

NOTES:

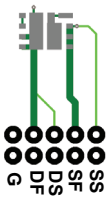
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



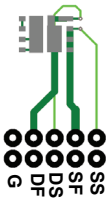
a. 55 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 155 °C/W when mounted on a minimum pad of 2 oz copper



d. 155 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Q1: E_{AS} of 661 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 21 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 65 A.
   Q2: E_{AS} of 661 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 21 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 65 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

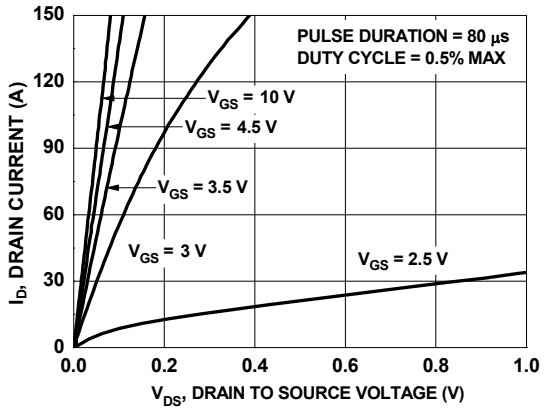


Figure 1. On Region Characteristics

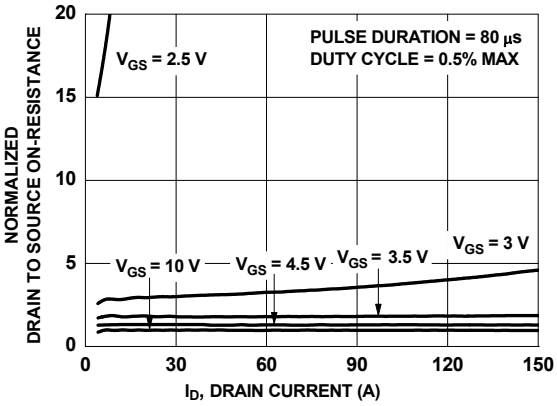


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

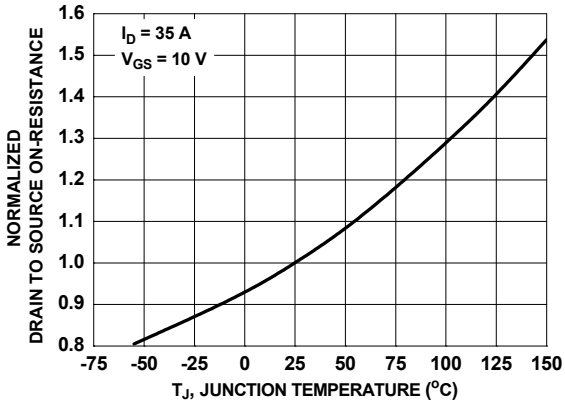


Figure 3. Normalized On Resistance vs. Junction Temperature

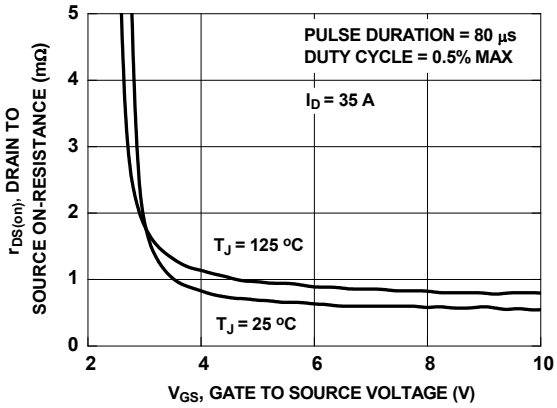


Figure 4. On-Resistance vs. Gate to Source Voltage

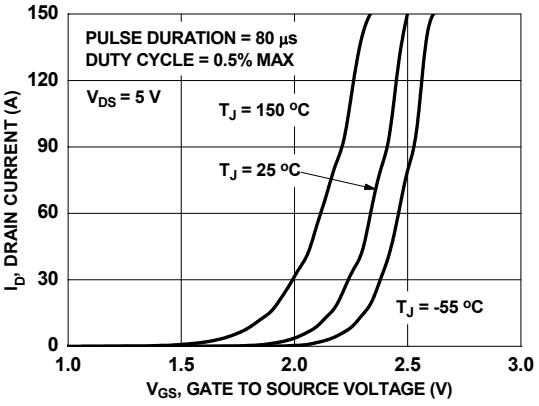


Figure 5. Transfer Characteristics

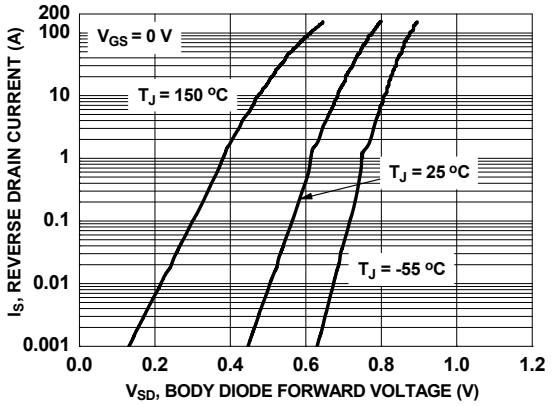


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

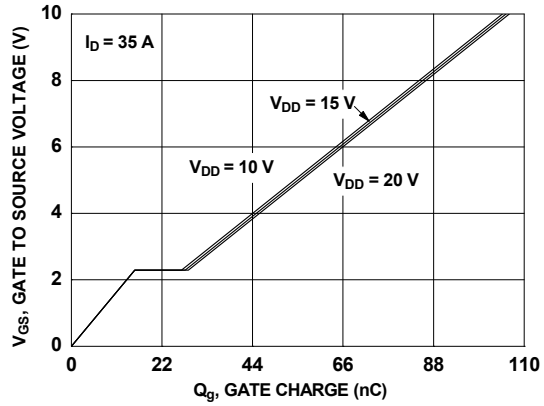


Figure 7. Gate Charge Characteristics

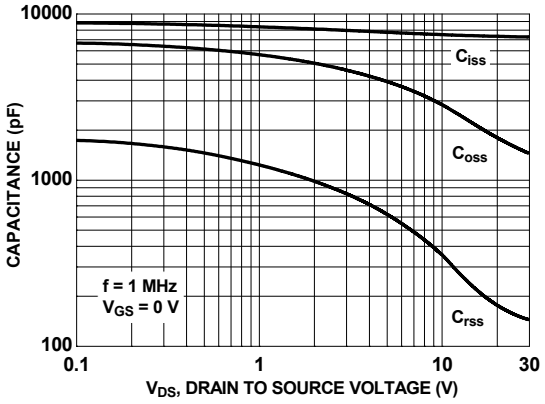


Figure 8. Capacitance vs. Drain to Source Voltage

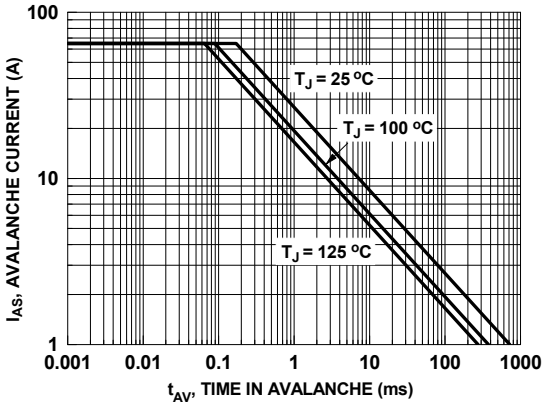


Figure 9. Unclamped Inductive Switching Capability

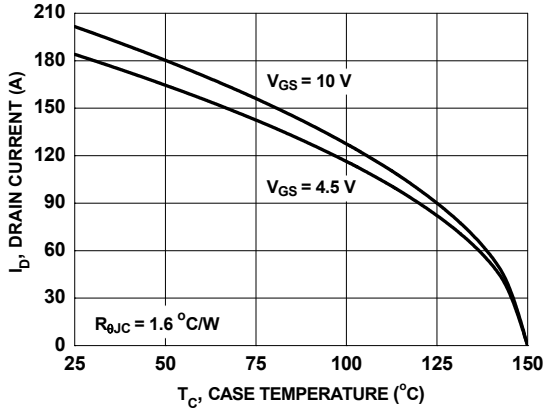


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

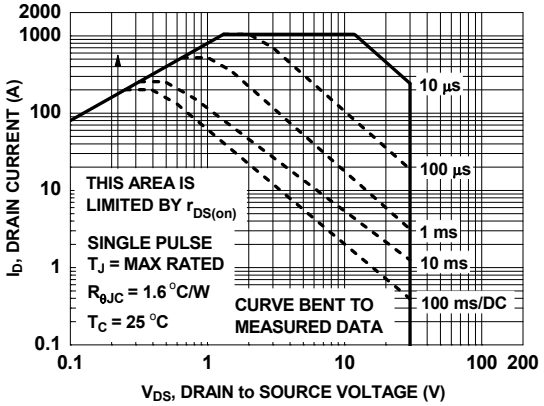


Figure 11. Forward Bias Safe Operating Area

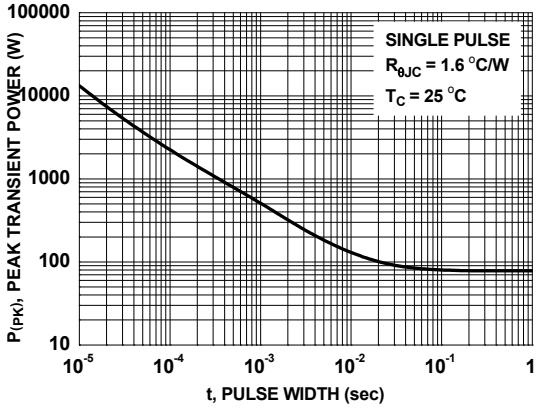


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

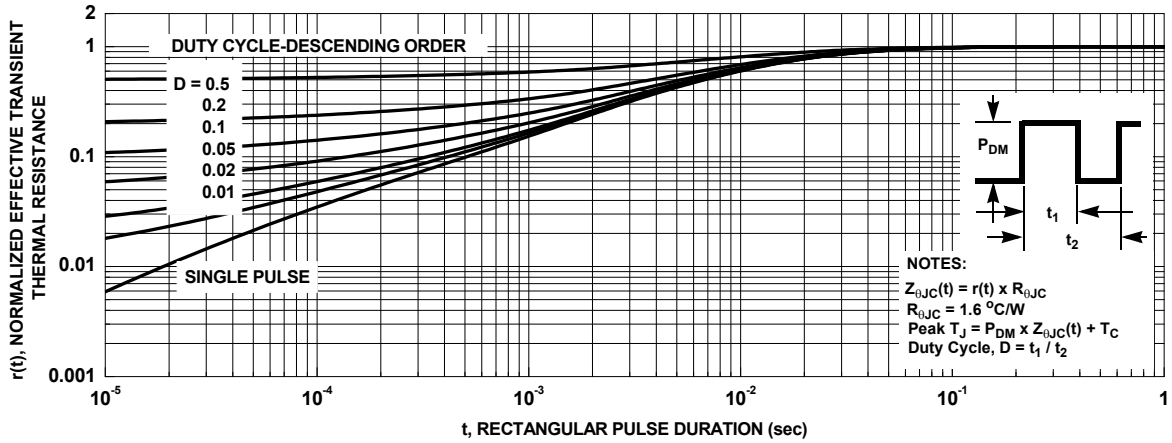


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

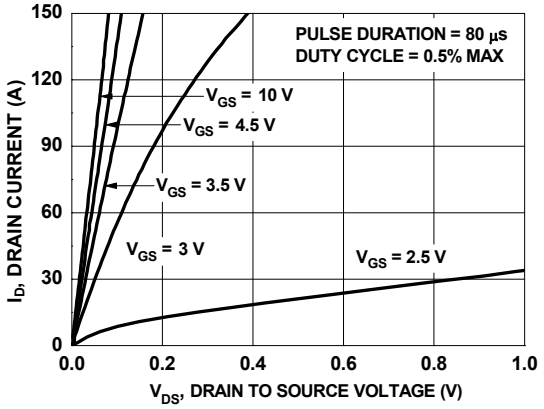


Figure 14. On- Region Characteristics

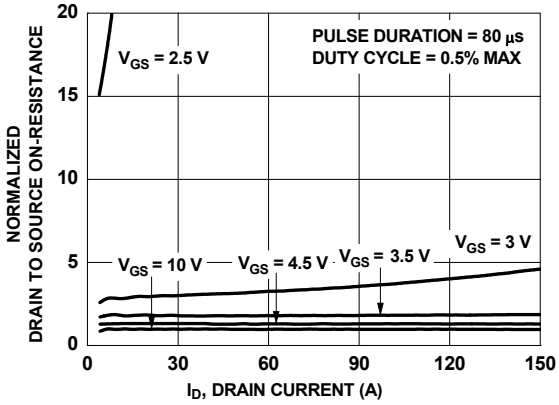


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

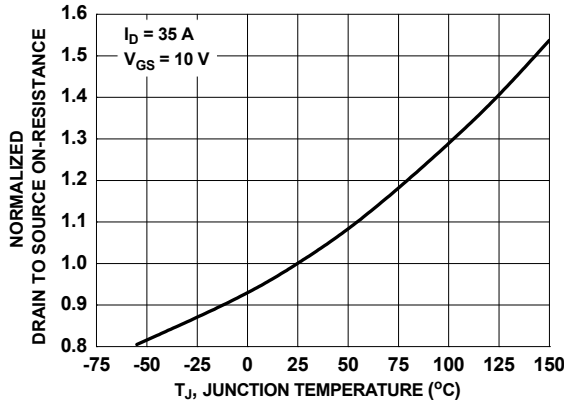


Figure 16. Normalized On-Resistance vs. Junction Temperature

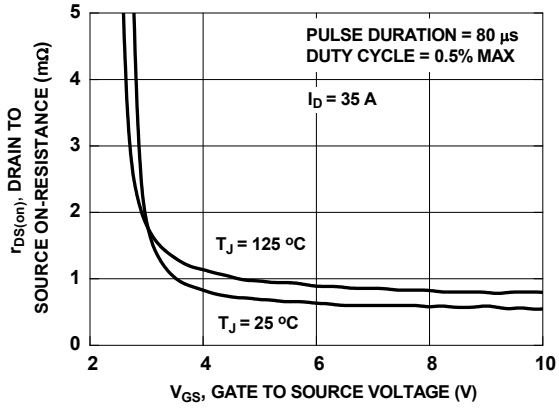


Figure 17. On-Resistance vs. Gate to Source Voltage

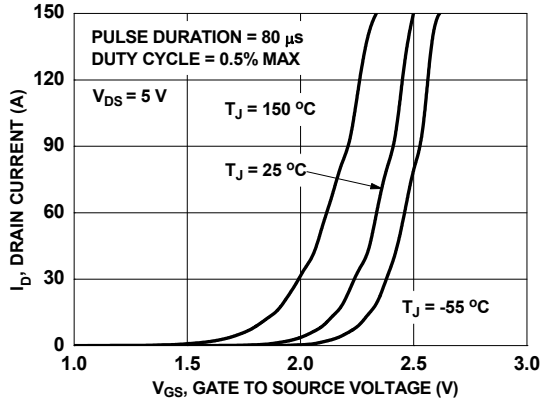


Figure 18. Transfer Characteristics

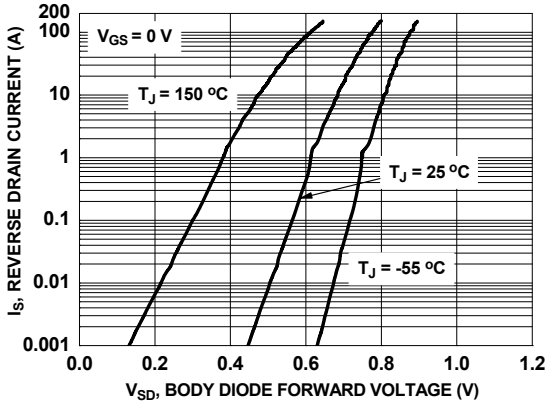


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted.

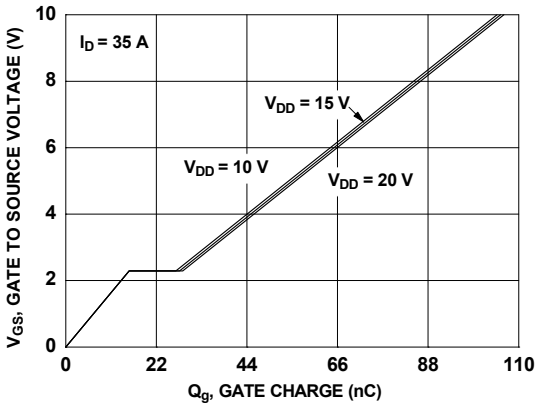


Figure 20. Gate Charge Characteristics

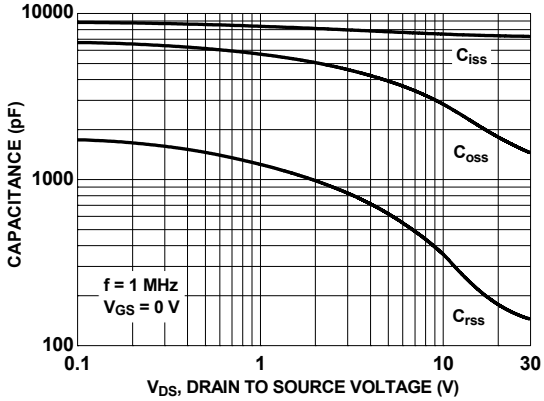


Figure 21. Capacitance vs. Drain to Source Voltage

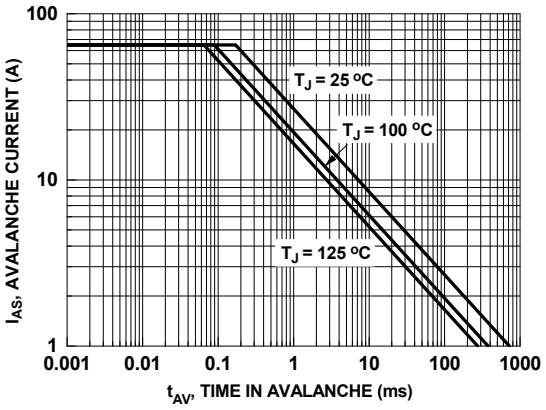


Figure 22. Unclamped Inductive Switching Capability

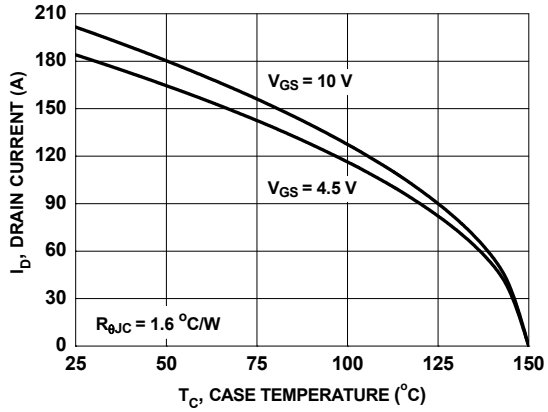


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

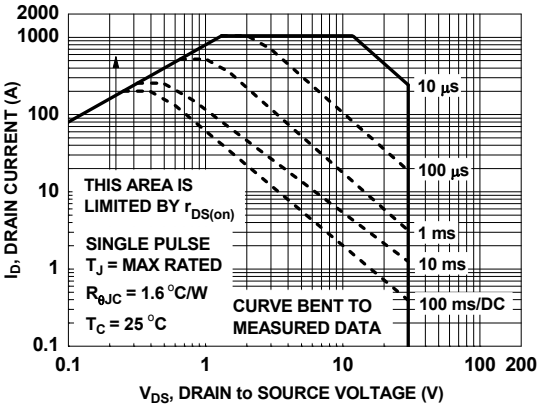


Figure 24. Forward Bias Safe Operating Area

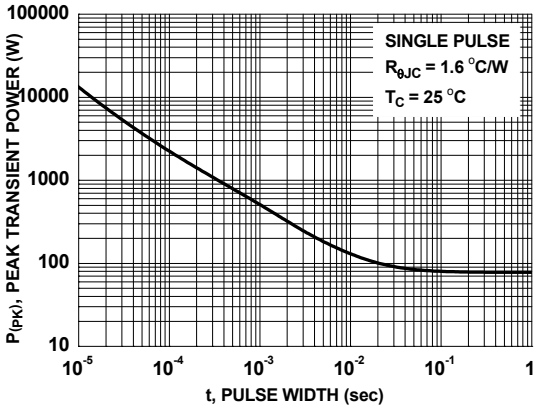


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

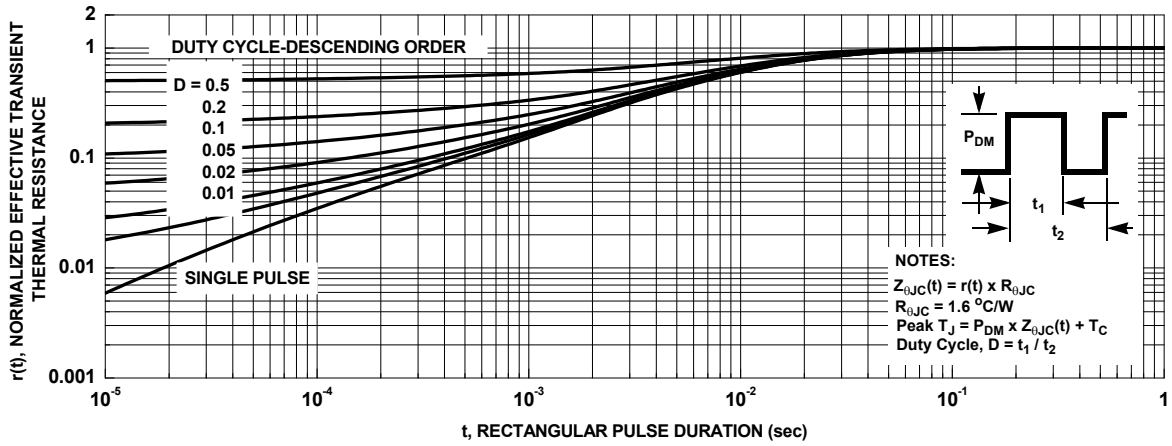
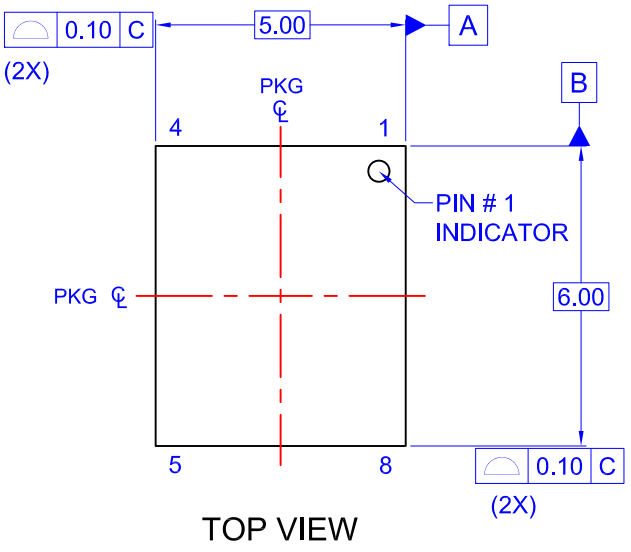
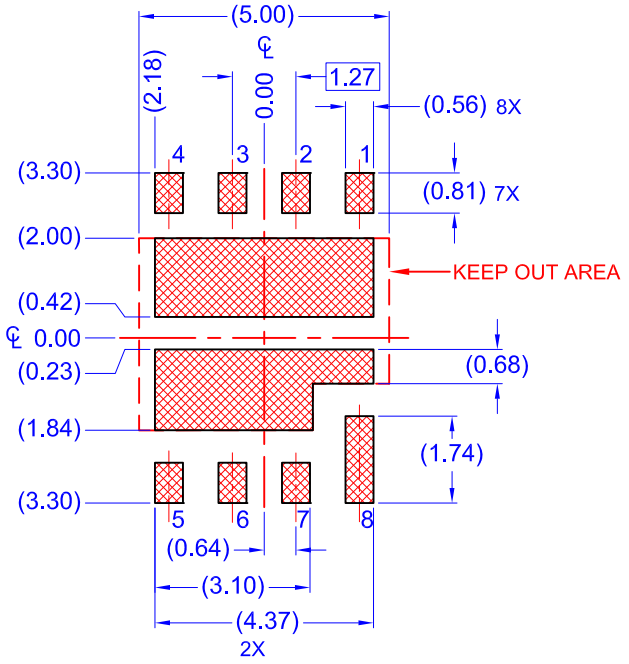


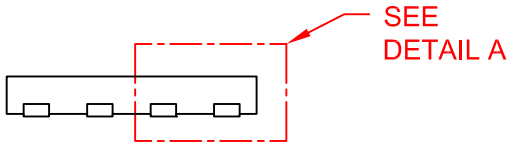
Figure 26. Junction-to-Case Transient Thermal Response Curve



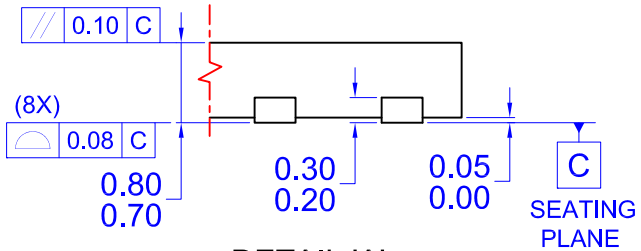
TOP VIEW



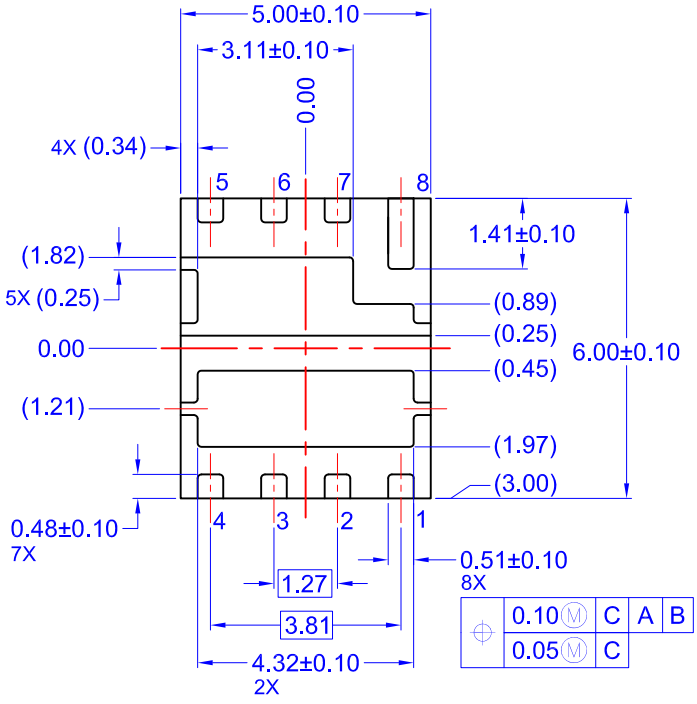
RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL 'A'
(SCALE: 2X)



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: MKT-PQFN08QREV2

FAIRCHILD™

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative