EN63A0QI 12A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN63A0QI is an Intel® Enpirion® Power System on a Chip (PowerSoC) DC-DC converter. It integrates the inductor, MOSFET switches, small-signal circuits and compensation in an advanced 10mm x 11mm x 3mm 76-pin QFN package. It offers high efficiency, excellent line and load regulation over temperature and up to the full 12A load range.

The EN63A0QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architectures. The device's advanced circuit techniques, ultra-high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra-compact, non-isolated DC-DC conversion.

Intel Enpirion Power Solutions significantly help in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

FEATURES

- High Efficiency (Up to 96%)
- Excellent Ripple and EMI Performance
- Up to 12A Continuous Operating Current
- Input Voltage Range (2.5V to 6.6V)
- Frequency Synchronization (Clock or Primary)
- 1.5% V_{OUT} Accuracy (Over Load and Temperature)
- Optimized Total Solution Size (225mm²)
- Precision Enable Threshold for Sequencing
- Programmable Soft-Start
- Master/Slave Configuration for Parallel Operation
- Thermal Shutdown, Over-Current, Short Circuit, and Under-Voltage Protection
- RoHS Compliant, MSL Level 3, 260°C Reflow

APPLICATIONS

- Point of Load Regulation for Low-Power, ASICs Multi-Core and Communication Processors, DSPs, FPGAs and Distributed Power Architectures
- Blade Servers, RAID Storage and LAN/SAN Adapter Cards, Wireless Base Stations, Industrial Automation, Test and Measurement, Embedded Computing, and Printers
- Beat Frequency/Noise Sensitive Applications

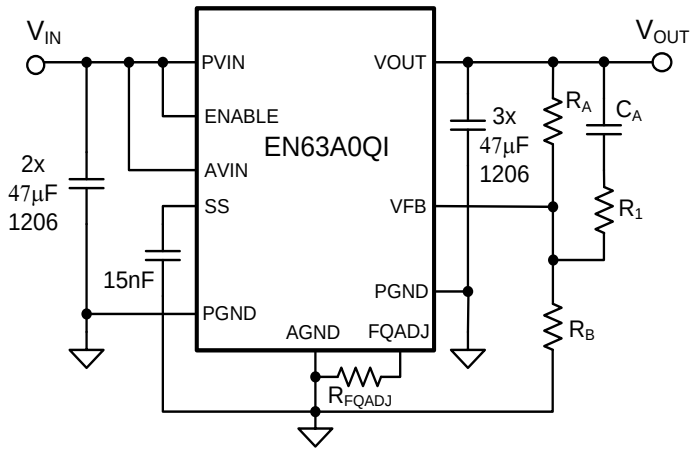


Figure 1: Simplified Applications Circuit

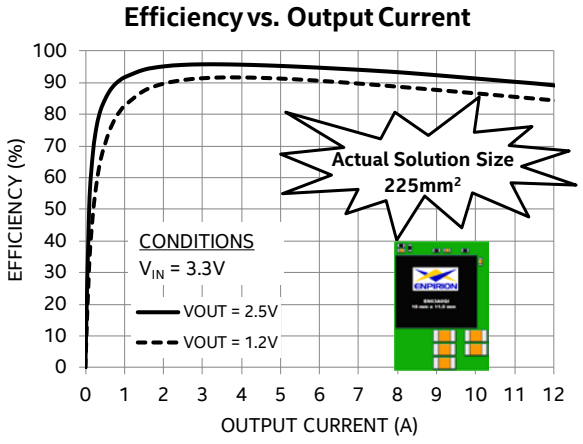


Figure 2: Highest Efficiency in Smallest Solution Size

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN63A0QI	EN63A0QI	-40°C to +125°C	76-pin (10mm x 11mm x 3mm) QFN T&R
EVB-EN63A0QI	EN63A0QI	QFN Evaluation Board	

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

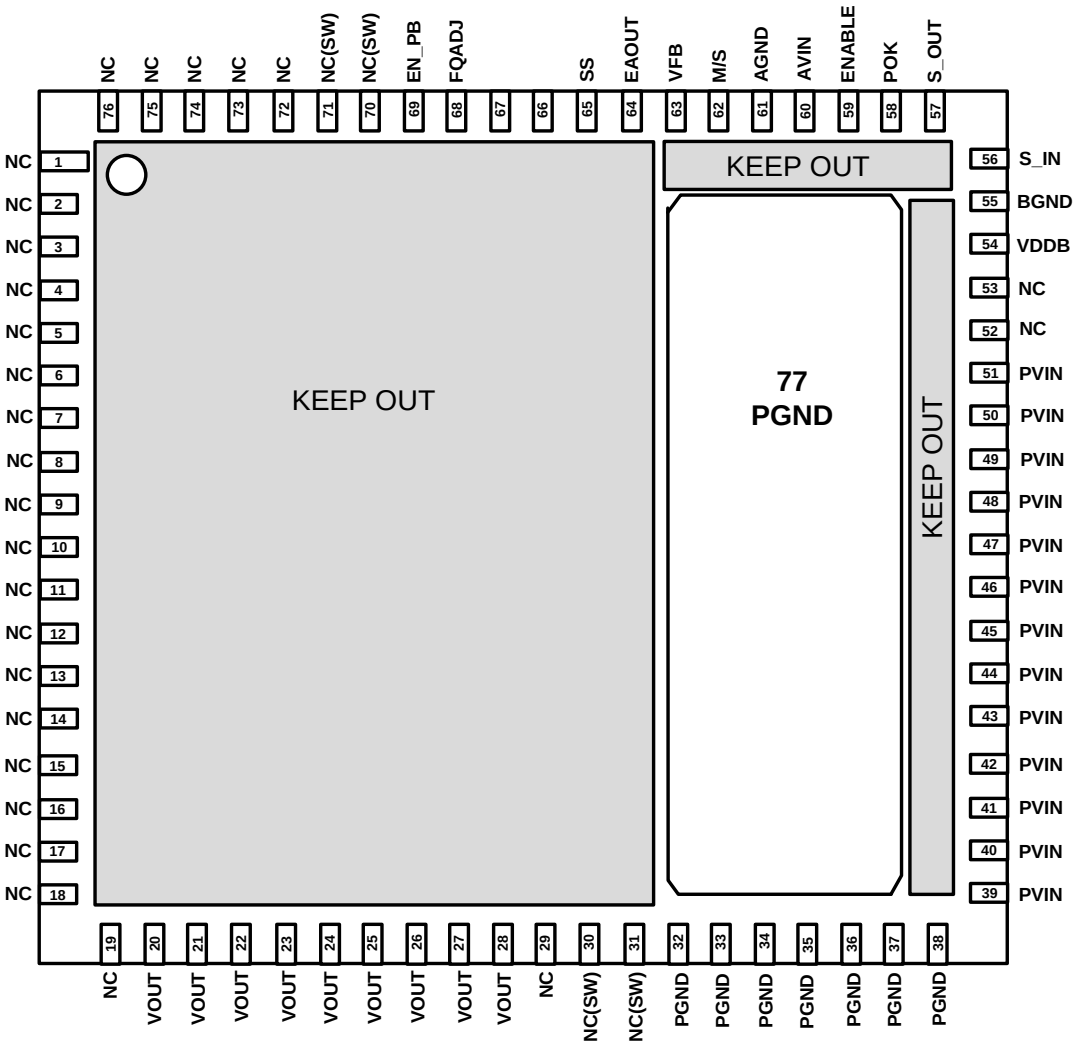


Figure 3: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

NOTE C: Keep-Out are No Connect pads that should not to be electrically connected to each other or to any external signal, ground or voltage. They do not need to be soldered to the PCB.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1-19, 29, 52-53, 67, 72-76	NC	-	No Connect. These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
20-28	VOUT	Power	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins. Refer to the Layout Recommendation section.
30-31, 70-71	NC(SW)	-	No Connect. These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
32-38	PGND	Ground	Input/Output power ground. Connect to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
39-51	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pin. Refer to the Layout Recommendation section.
54	VDDB	Power	Internal regulated voltage used for the internal control circuitry. Decouple with an optional 0.1µF capacitor to BGND for improved efficiency. This pin may be left floating if board space is limited.
55	BGND	Power	Ground for VDDB. Refer to pin 54 description.
56	S_IN	Analog	Digital input. A high level on the M/S pin will make this EN63A0QI a Slave and the S_IN will accept the S_OUT signal from another EN63A0QI for parallel operation. A low level on the M/S pin will make this device a Master and the switching frequency will be phase locked to an external clock. Leave this pin floating if it is not used.
57	S_OUT	Analog	Digital output. A low level on the M/S pin will make this EN63A0QI a Master and the internal switching PWM signal is output on this pin. This output signal is connected to the S_IN pin of another EN63A0QI device for parallel operation. Leave this pin floating if it is not used.
58	POK	Digital	POK is a logic level high when VOUT is within -10% to +20% of the programmed output voltage ($0.9V_{OUT\_NOM} \le V_{OUT} \le 1.2V_{OUT\_NOM}$). This pin has an internal pull-up resistor to AVIN with a nominal value of 94kΩ.
59	ENABLE	Analog	Device enable pin. A high level or floating this pin enables the device while a low level disables the device. A voltage ramp from another power converter may be applied for precision enable. Refer to Power Up Sequencing.
60	AVIN	Power	Analog input voltage for the control circuits. Connect this pin to the input power supply (PVIN) at a quiet point. Can also be connected to an auxiliary supply within a voltage range that is sequencing.

PIN	NAME	TYPE	FUNCTION
61	AGND	Power	The quiet ground for the control circuits. Connect to the ground plane with a via right next to the pin.
62	M/S	Analog	Ternary (three states) input pin. Floating this pin disables parallel operation. A low level configures the device as Master and a high level configures the device as a Slave. A R_{EXT} resistor is recommended to pulling M/S high. Refer to Ternary Pin description in the Functional Description section for R_{EXT} values. Also see S_IN and S_OUT pin descriptions.
63	VFB	Analog	This is the external feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor (C_A) and resistor (R1) are required parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage equal to 0.600V. For Slave devices, leave VFB floating.
64	EAOUT	Analog	Error amplifier output. Allows for customization of the control loop. May be left floating.
65	SS	Analog	A soft-start capacitor is connected between this pin and AGND. The value of the capacitor controls the soft-start interval. Refer to Soft-Start in the Functional Description for more details.
66	VSENSE	Analog	This pin senses output voltage when the device is in pre-bias (or back-feed) mode. Connect VSENSE to VOUT when EN_PB is high or floating. Leave floating when EN_PB is low.
68	FQADJ	Analog	Frequency adjust pin. This pin must have a resistor to AGND which sets the free running frequency of the internal oscillator.
69	EN_PB	Analog	Enable pre-bias input. When this pin is pulled high, the device will support monotonic start-up under a pre-biased load. VSENSE must be tied to VOUT for EN_PB to function. This pin is pulled high internally. Enable pre-bias feature is not available for parallel operations.
77	PGND	Power	Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes. Refer to Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VOUT		-0.3	7.0	V
ENABLE, POK, M/S		-0.3	V_{IN}+0.3	V
VFB, EXTREF, EAOUT, SS, S_IN, S_OUT, FQADJ		-0.3	2.5	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.5	6.6	V
Output Voltage Range	V_{OUT}	0.6	$V_{IN} - V_{DO}$ (1)	V
Output Current Range	I_{OUT}		12	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	20	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	14	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1.0	°C/W

(1) V_{DO} (dropout voltage) is defined as (I_{LOAD} x Droput Resistance). Please refer to Electrical Characteristics Table.

(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: V_{IN} = PVIN = AVIN = 6.6V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	PVIN = AVIN	2.5		6.6	V
VFB Pin Voltage	V_{VFB}	Internal Voltage Reference at: V_{IN} = 5V, ILOAD = 0, T_A = 25°C	0.594	0.600	0.606	V
VFB Pin Voltage (Load and Temperature)	V_{VFB}	0A ≤ I_{LOAD} ≤ 12A Starting Date Code: X501 or greater	0.591	0.600	.609	V
VFB Pin Voltage (Line, Load and Temperature)	V_{VFB}	2.5V ≤ V_{IN} ≤ 6.6V 0A ≤ I_{LOAD} ≤ 12A	0.588	0.600	0.612	V
VFB Pin Input Leakage Current (3)	I_{VFB}	VFB Pin Input Leakage Current	-10		10	nA
Shut-Down Supply Current	I_S	Power Supply Current with ENABLE=0		1.5		mA
Under Voltage Lock-out – V_{IN} Rising	V_{UVLOR}	Voltage Above Which UVLO is Not Asserted		2.2		V
Under Voltage Lock-out – V_{IN} Falling	V_{UVLOF}	Voltage Below Which UVLO is Asserted		2.1		V
Dropout Voltage	V_{DO}	V_{INMIN} – V_{OUT} at Full Load		600	1200	mV
Dropout Resistance (3)	R_{DO}	Input to Output Resistance		50	100	mΩ
Continuous Output Current	I_{OUT_SRC}	Refer to Table 2 for conditions.	0		12	A
Over Current Trip Level	I_{OCP}	Sourcing Current		18.5		A
Switching Frequency	F_{SW}	R_{FADJ} = 4.42 kΩ, V_{IN} = 5V	0.9	1.2	1.5	MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	SYNC Clock Input Frequency Range	0.9*F_{sw}	F_{sw}	1.1*F_{sw}	MHz
S_IN Clock Amplitude – Low	$V_{S\_IN\_LO}$	SYNC Clock Logic Low	0		0.8	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
S_IN Clock Amplitude – High	$V_{S\_IN\_HI}$	SYNC Clock Logic High	1.8		2.5	V
S_IN Clock Duty Cycle (PLL)	DC_{S_INPLL}	M/S Pin Float or Low	20		80	%
S_IN Clock Duty Cycle (PWM)	DC_{S_INPWM}	M/S Pin High	10		90	%
Pre-Bias Level	V_{PB}	Allowable Pre-bias as a Fraction of Programmed Output Voltage for Monotonic start up. Minimum Pre-bias Voltage = 300mV.	20		75	%
Non-Monotonicity	V_{PB_NM}	Allowable Non-monotonicity Under Pre-bias Startup		100		mV
V_{OUT} Range for P_{OK} = High (4)		Range of Output Voltage as a Fraction of Programmed Value When P_{OK} is Asserted	90		120	%
P_{OK} Deglitch Delay		Falling Edge Deglitch Delay After Output Crossing 90% level. F_{SW}=1.2 MHz		213		µs
V_{POK} Logic Low level		With 4mA Current Sink into P_{OK} Pin			0.4	V
V_{POK} Logic high level				V_{IN}		V
POK Internal pull-up resistor				94		kΩ
Current Balance	ΔI_{OUT}	With 2 to 4 Converters in Parallel, the Difference Between Nominal and Actual Current Levels. ΔV_{IN}<50mV; R_{TRACE}< 10 mΩ, I_{load}= # Converter * I_{MAX}		±10		%
V_{OUT} Rise Time Accuracy (5)(6)(7)	ΔT_{RISE}	t_{RISE} [ms] = C_{SS} [nF] x 0.065; 10nF ≤ C_{SS} ≤ 30nF;	-25		+25	%
ENABLE Logic High	V_{ENABLE_HIGH}	2.5V ≤ V_{IN} ≤ 6.6V;	1.2		V_{IN}	V
ENABLE Logic Low	V_{ENABLE_LOW}		0		0.8	V
ENABLE Pin Current	I_{EN}	VIN = 6.6V		50		µA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
M/S Ternary Pin Logic Low	V_{T-LOW}	Tie M/S Pin to GND	0		0.7	V
M/S Ternary Pin Logic Float	$V_{T-FLOAT}$	M/S Pin is Open	1.1		1.4	V
M/S Ternary Pin Logic Hi (8)	V_{T-HIGH}	Pull Up to VIN through an external resistor R_{EXT} . Refer to Figure .	1.8			V
Ternary Pin Input Current	I_{TERN}	2.5V ≤ V_{IN} ≤ 4V, R_{EXT} = 15kΩ 4V < V_{IN} ≤ 6.6V, R_{EXT} = 51kΩ			117 88	µA
Binary Pin Logic Low Threshold	V_{B-LOW}	ENABLE, S_IN			0.8	V
Binary Pin Logic High Threshold	V_{B-HIGH}	ENABLE, S_IN	1.8			V
S_OUT Low Level	$V_{S\_OUT\_LOW}$				0.4	V
S_OUT High Level	$V_{S\_OUT\_HIGH}$		2.0			V

(3) Parameter not production tested but is guaranteed by design.

(4) POK threshold when VOUT is rising is nominally 92%. This threshold is 90% when VOUT is falling. After crossing the 90% level, there is a 256 clock cycle (~213µs at 1.2 MHz) delay before POK is de-asserted. The 90% and 92% levels are nominal values. Expect these thresholds to vary by ±3%.

(5) Parameter not production tested but is guaranteed by design.

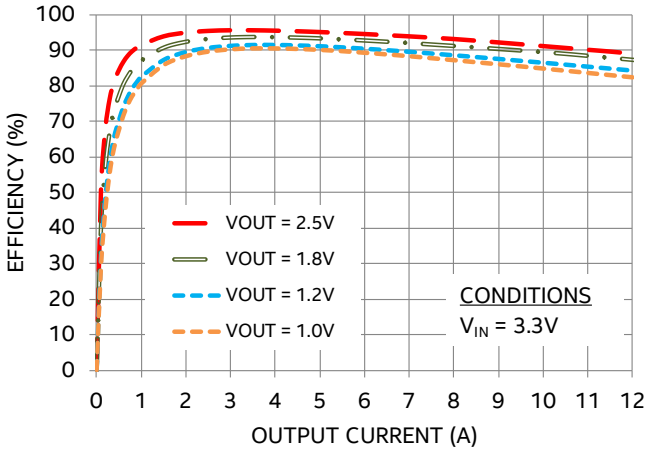
(6) Rise time calculation begins when AVIN > V_{UVLO} and ENABLE = HIGH.

(7) V_{OUT} Rise Time Accuracy does not include soft-start capacitor tolerance.

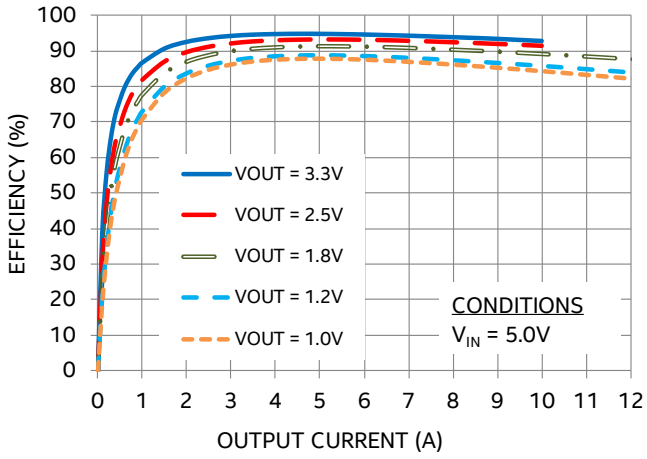
(8) M/S pin is ternary. Ternary pins have three logic levels: high, float, and low. This pin is meant to be strapped to VIN through an external resistor, strapped to GND, or left floating. The state cannot be changed while the device is on.

TYPICAL PERFORMANCE CURVES

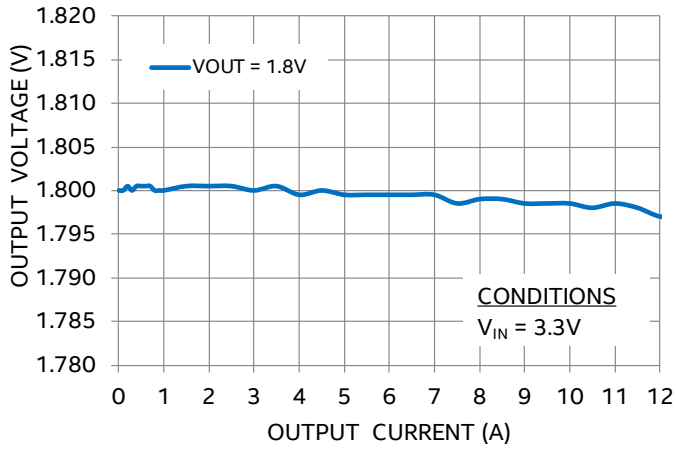
Efficiency vs. Output Current



Efficiency vs. Output Current



Output Voltage vs. Output Current



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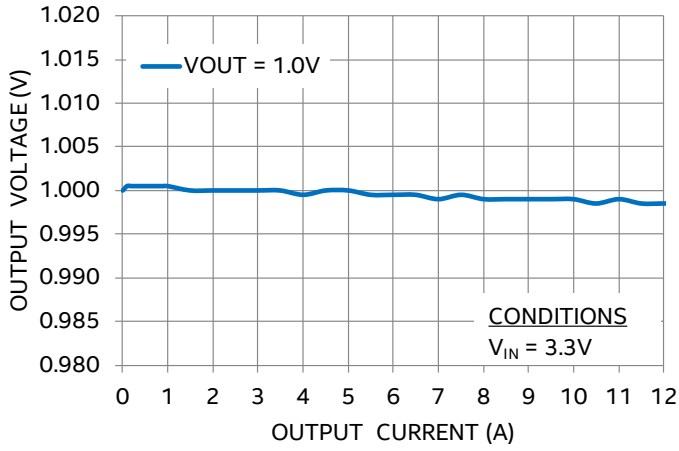

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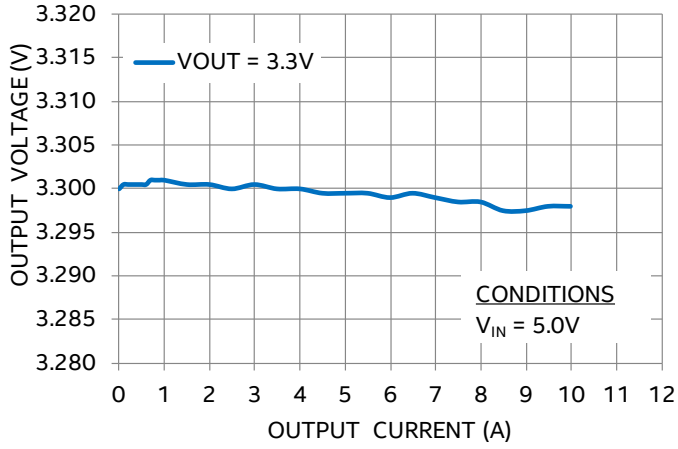

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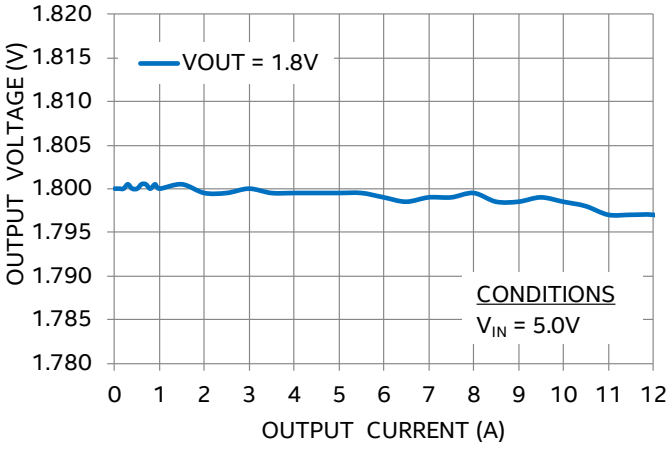
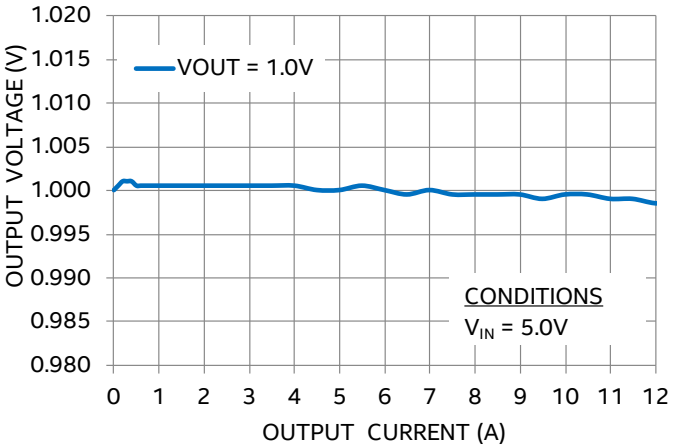
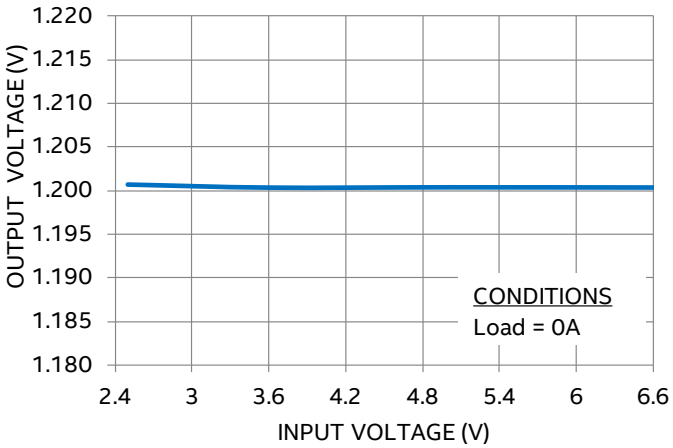


TYPICAL PERFORMANCE CURVES (CONTINUED)

Output Voltage vs. Output Current



Output Voltage vs. Input Voltage



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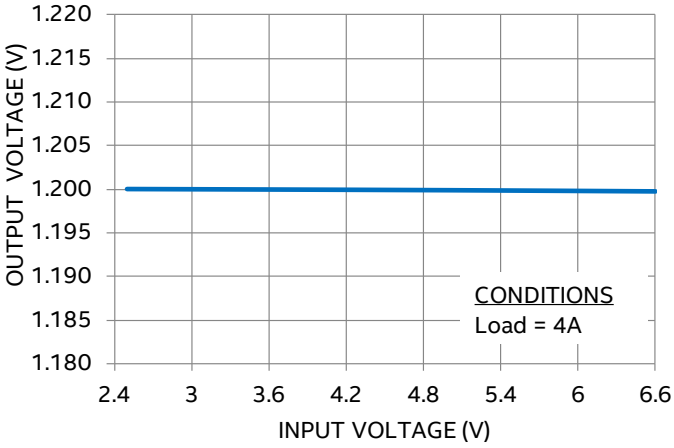
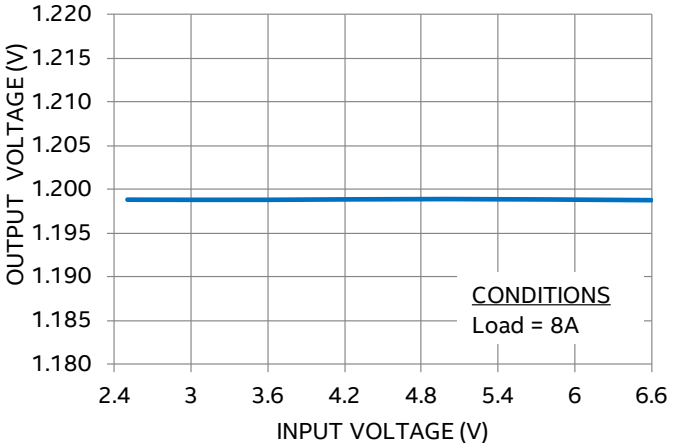
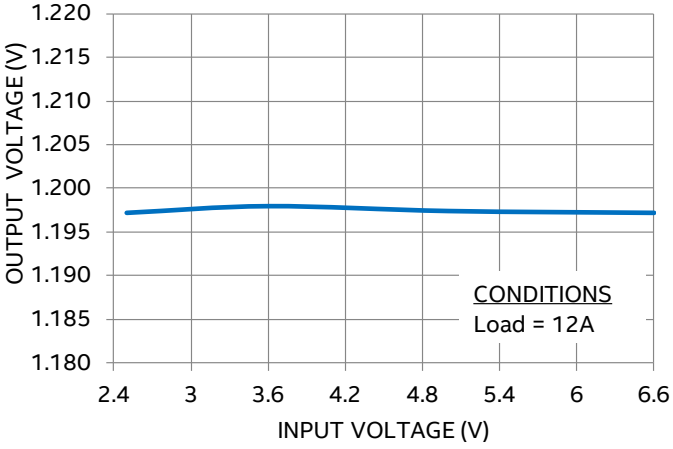


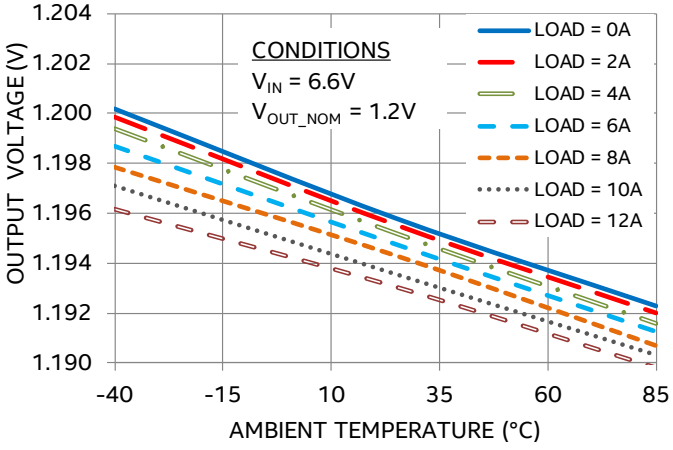
Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage

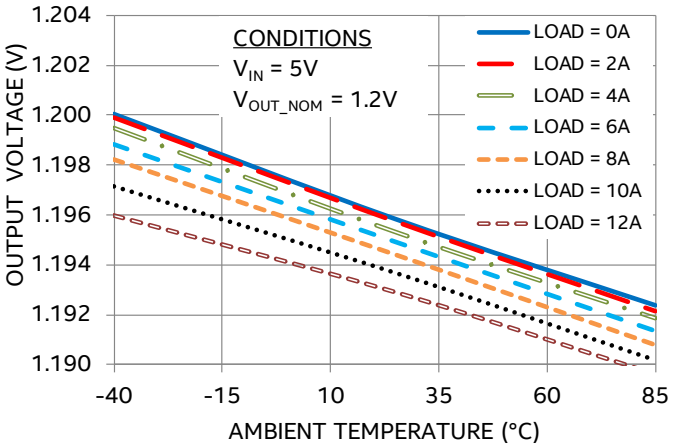


Output Voltage vs. Temperature

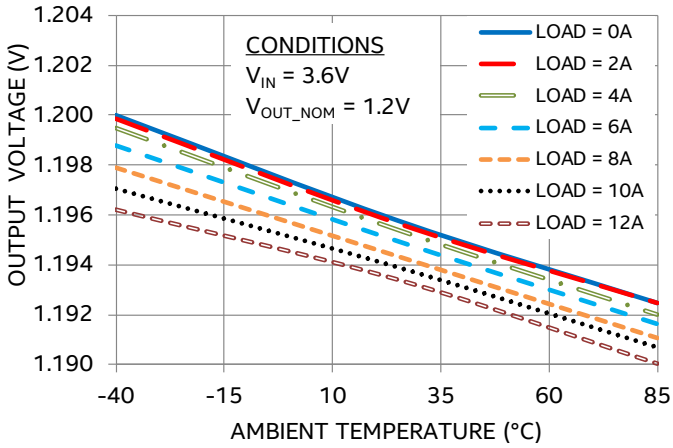


TYPICAL PERFORMANCE CURVES (CONTINUED)

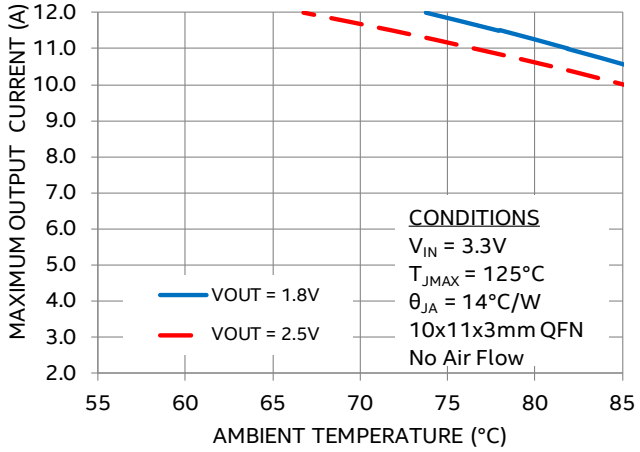
Output Voltage vs. Temperature



Output Voltage vs. Temperature



Output Current De-rating



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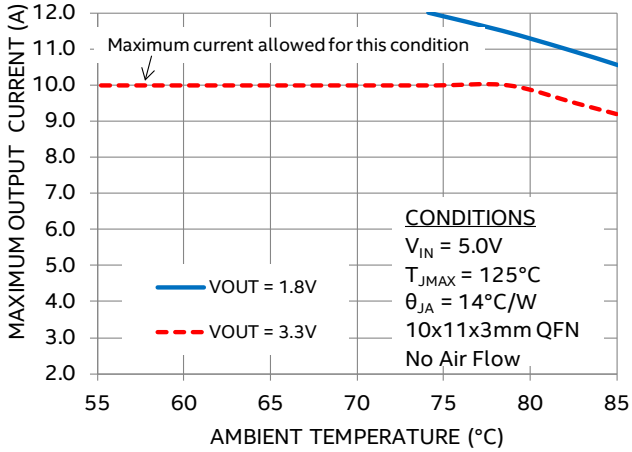
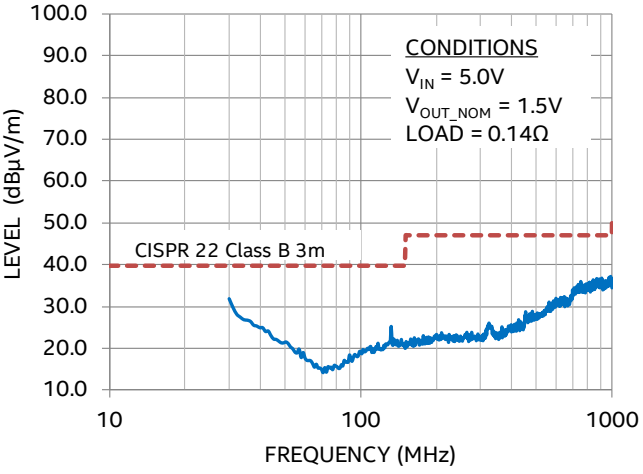
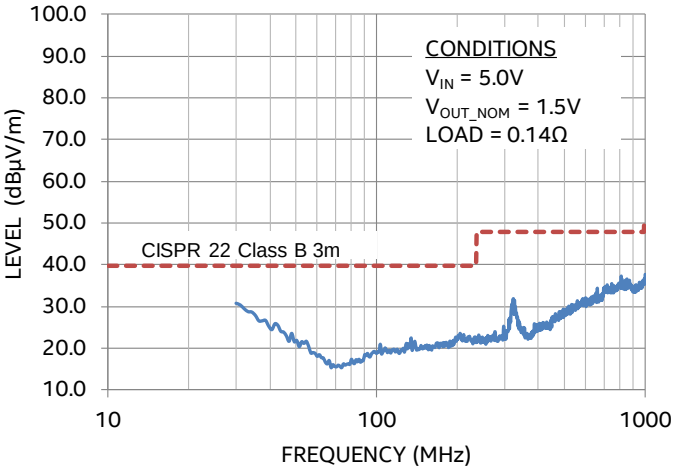


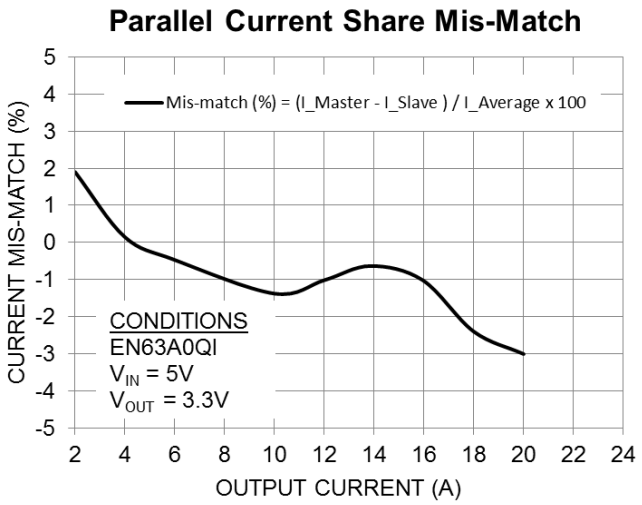
EMI Performance (Horizontal Scan)

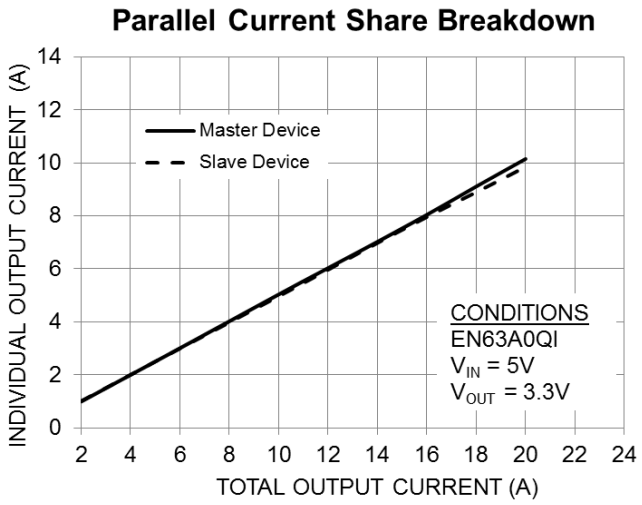


EMI Performance (Vertical Scan)



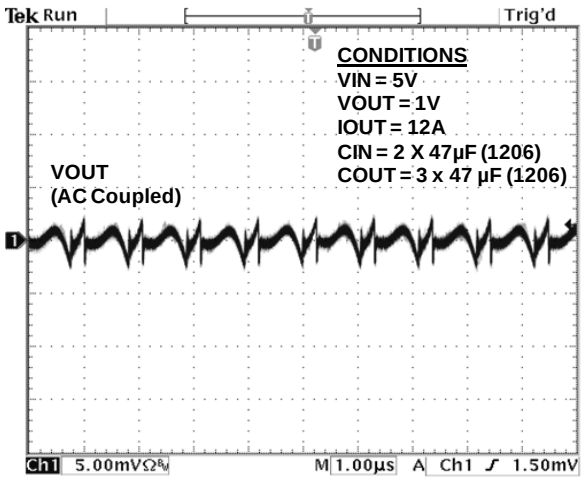
TYPICAL PARALLEL PERFORMANCE CURVES (CONTINUED)



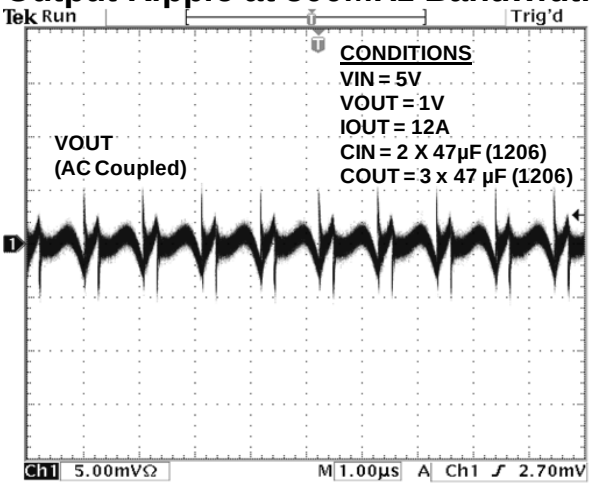


TYPICAL PERFORMANCE CHARACTERISTICS

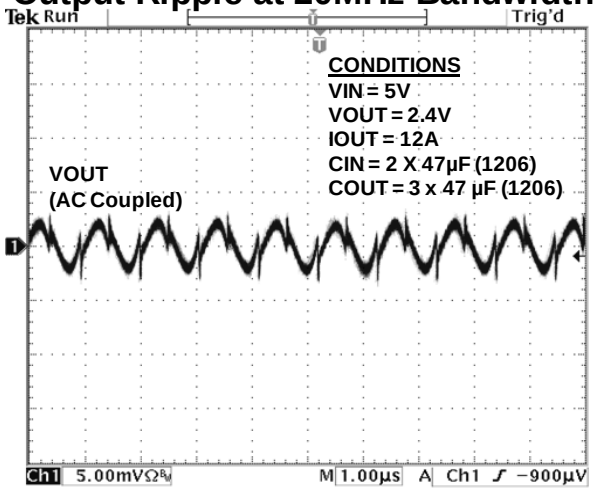
Output Ripple at 20MHz Bandwidth



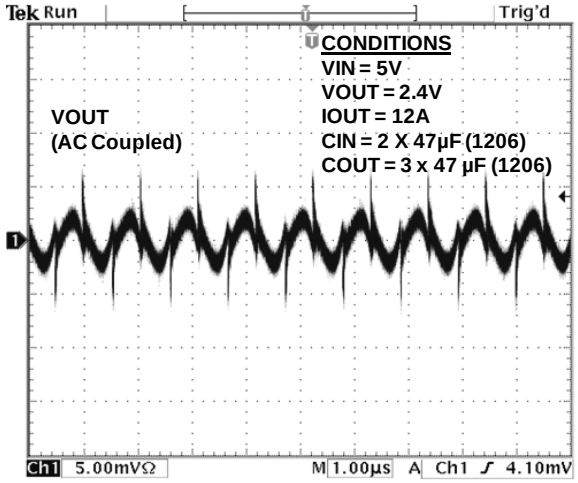
Output Ripple at 500MHz Bandwidth



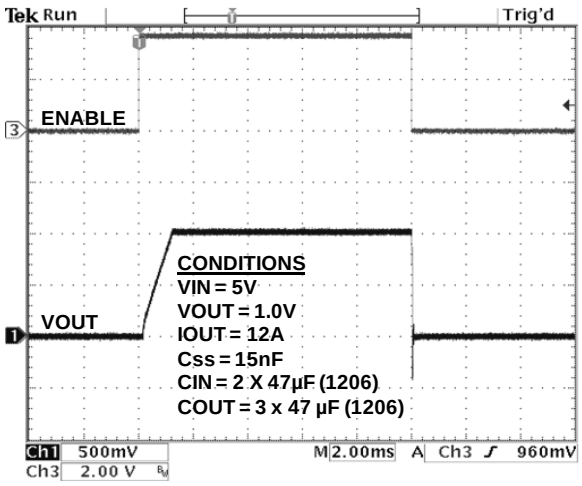
Output Ripple at 20MHz Bandwidth



Output Ripple at 500MHz Bandwidth



Enable Power Up/Down



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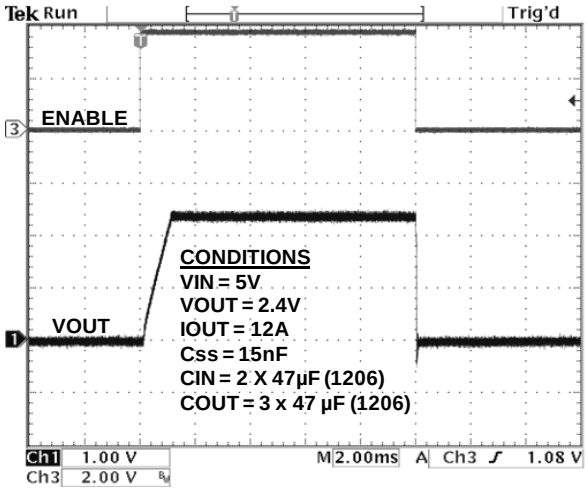
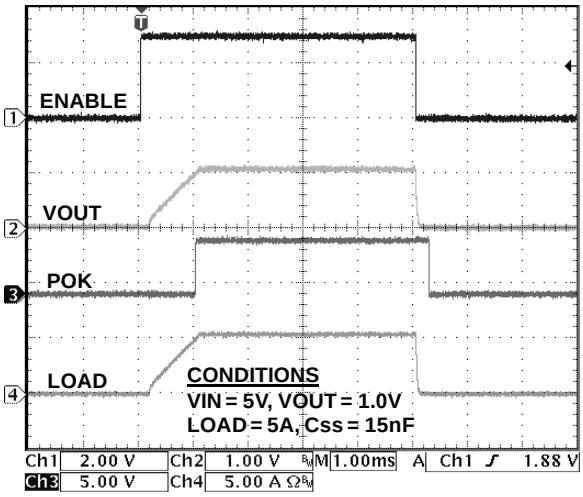
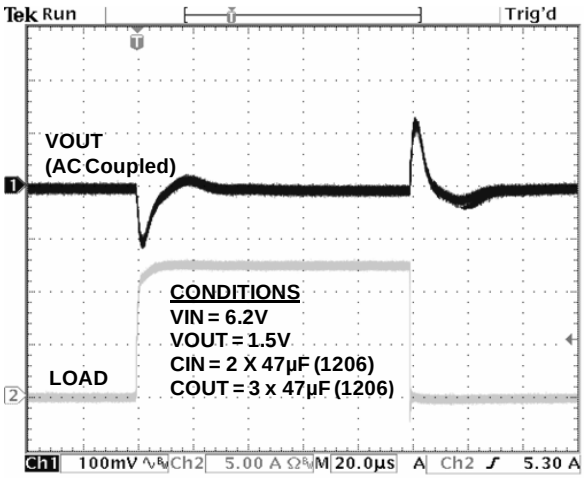


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

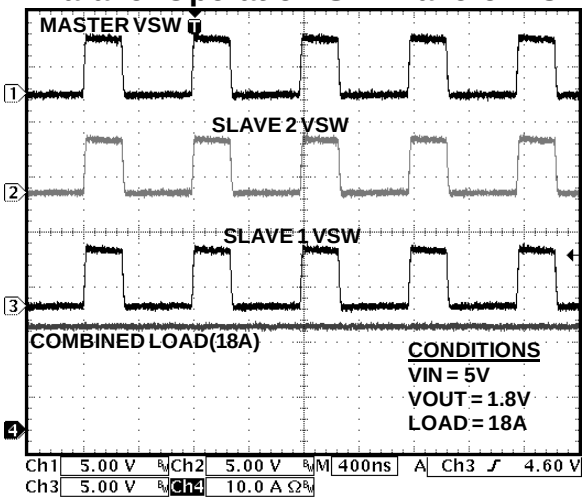
Enable/Disable with POK



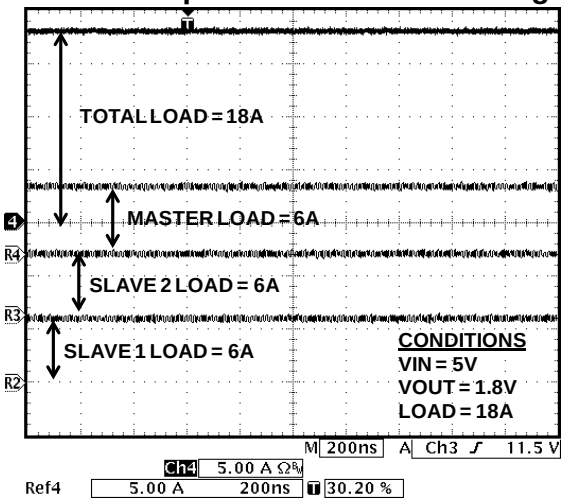
Load Transient from 0 to 12A



Parallel Operation SW Waveforms



Parallel Operation Current Sharing



FUNCTIONAL BLOCK DIAGRAM

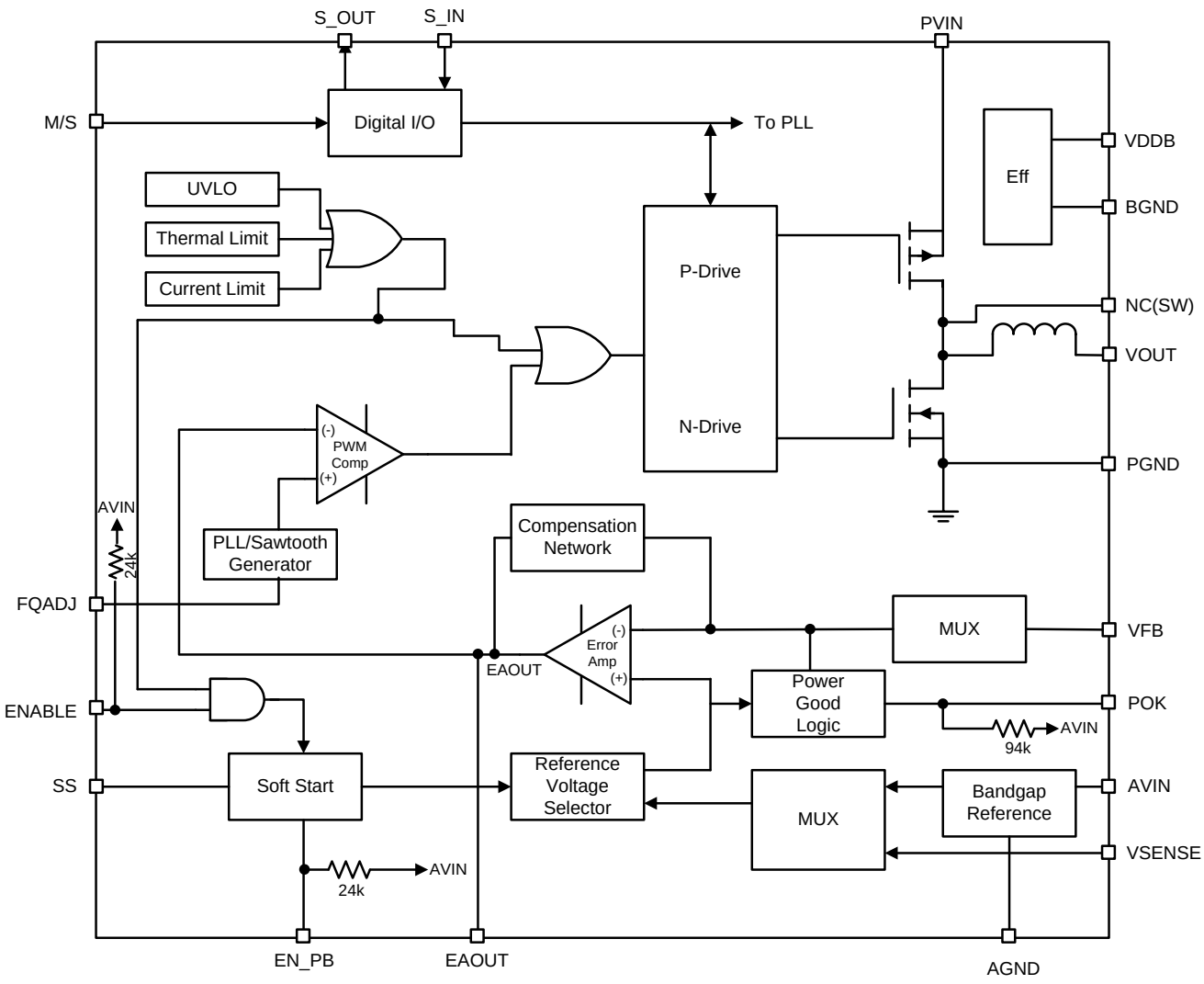


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN63A0QI is a synchronous, programmable buck power supply with integrated power MOSFET switches and integrated inductor. The switching supply uses voltage mode control and a low noise PWM topology. This provides superior impedance matching to ICs processed in sub 90nm process technologies. The nominal input voltage range is 2.5 - 6.6 volts. The output voltage is programmed using an external resistor divider network. The feedback control loop incorporates a type IV voltage mode control design. Type IV voltage mode control maximizes control loop bandwidth and maintains excellent phase margin to improve transient performance. The EN63A0QI is designed to support up to 12A continuous output current operation. The operating switching frequency is between 0.9MHz and 1.5MHz and enables the use of small-size input and output capacitors.

The power supply has the following features:

- Precision Enable Threshold
- Soft-Start
- Pre-bias Start-Up
- Resistor Programmable Switching Frequency
- Phase-Lock Frequency Synchronization
- Parallel Operation
- Power OK
- Over-Current/Short Circuit Protection
- Thermal Shutdown with Hysteresis
- Under-Voltage Lockout

Precision Enable

The ENABLE threshold is a precision analog voltage rather than a digital logic threshold. A precision voltage reference and a comparator circuit are kept powered up even when ENABLE is de-asserted. The narrow voltage gap between ENABLE Logic Low and ENABLE Logic High allows the device to turn on at a precise enable voltage level. With the enable threshold pinpointed, a proper choice of soft-start capacitor helps to accurately sequence multiple power supplies in a system as desired. There is an ENABLE lockout time of 2ms that prevents the device from re-enabling immediately after it is disabled.

Soft-Start Operation

The SS pin in conjunction with a small external capacitor between this pin and AGND provides a soft-start function to limit in-rush current during device power-up. When the part is initially powered up, the output voltage is gradually ramped to its final value. The gradual output ramp is achieved by increasing the reference voltage to the error amplifier. A constant current flowing into the soft-start capacitor provides the reference voltage ramp. When the voltage on the soft-start capacitor reaches 0.60V, the output has reached its programmed voltage. Once the output voltage has reached nominal voltage the soft-start capacitor will continue to charge to 1.5V (Typical). The output rise time can be controlled by the choice of soft-start capacitor value.

The rise time is defined as the time from when the ENABLE signal crosses the threshold and the input voltage crosses the upper UVLO threshold to the time when the output voltage reaches 95% of the programmed value. The rise time (t_{RISE}) is given by the following equation:

$$t_{RISE}\ [ms] = C_{ss}\ [nF] \times 0.065$$

The rise time (t_{RISE}) is in milliseconds and the soft-start capacitor (C_{SS}) is in nano-Farads. The soft-start capacitor should be between 10nF and 100nF.

Pre-Bias Start-up

The EN63A0QI supports startup into a pre-biased load. A proprietary circuit ensures the output voltage rises up from the pre-bias value to the programmed output voltage. Start-up is guaranteed to be monotonic for pre-bias voltages in the range of 20% to 75% of the programmed output voltage with a minimum pre-bias voltage of 300mV. Outside of the 20% to 75% range, the output voltage rise will not be monotonic. The Pre-Bias feature is automatically engaged with an internal pull-up resistor. For this feature to work properly, V_{IN} must be ramped up prior to ENABLE turning on the device. Tie VSENSE to VOUT if Pre-Bias is used. Tie EN_PB

to ground and leave VSENSE floating to disable the Pre-Bias feature. Pre-Bias is supported for external clock synchronization, but not supported for parallel operations.

Resistor Programmable Frequency

The operation of the EN63A0QI can be optimized by a proper choice of the R_{FQADJ} resistor. The frequency can be tuned to optimize dynamic performance and efficiency. Refer to Table 1 and Table 2 for recommended RFQADJ values based on maximum output current operations.

Table 1: Recommended R_{FQADJ} (kΩ) at 10A

V_{IN} \ V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
3.3V ±10%	3.57	3.57	4.42	4.42	3.57	--
5.0V ±10%	3.57	3.57	3.57	4.42	4.42	3.57
6.0V ±10%	3.57	3.57	3.57	4.42	4.42	3.57

Table 2: Recommended R_{FQADJ} (kΩ) at 12A

V_{IN} \ V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
3.3V ±10%	3.57	3.57	4.42	4.42	3.57	--
5.0V ±10%	3.57	12.1	12.1	20.0	NR	NR
6.0V ±10%	20.0	20.0	20.0	NR	NR	NR

Note: NR = Device not rated for this operation condition

Phase-Lock Operation:

The EN63A0QI can be phase-locked to an external clock signal to synchronize its switching frequency. The M/S pin can be left floating or pulled to ground to allow the device to synchronize with an external clock signal using the S_IN pin. When a clock signal is present at S_IN, an activity detector recognizes the presence of the clock signal and the internal oscillator phase locks to the external clock. The external clock could be the system clock or the output of another EN63A0QI. The phase locked clock is then output at S_OUT.

Master / Slave (Parallel) Operation and Frequency Synchronization

Multiple EN63A0QI devices may be connected in a Master/Slave configuration to handle larger load currents. The device is placed in Master mode by pulling the M/S pin low or in Slave mode by pulling M/S pin high. **When the M/S pin is in float state, parallel operation is not possible.** In Master mode, a version of the internal switching PWM signal is output on the S_OUT pin. This PWM signal from the Master is fed to the Slave device at its S_IN pin. The Slave device acts like an extension of the power FETs in the Master and inherits the PWM frequency and duty cycle. The inductor in the Slave prevents crow-bar currents from Master to Slave due to timing delays. The Master device's switching clock may be phase-locked to an external clock source or another EN63A0QI to move the entire parallel operation frequency away from sensitive frequencies. The feedback network for the Slave device may be left open. Additional Slave devices may be paralleled together with the Master by connecting the S_OUT of the Master to the S_IN of all other Slave devices. Refer to Figure for details.

Careful attention is needed in the layout for parallel operation. The VIN, VOUT and GND of the paralleled devices should have low impedance connections between each other. Maximize the amount of copper used to connect these pins and use as many vias as possible when using multiple layers. Place the Master device between all other Slaves and closest to the point of load.

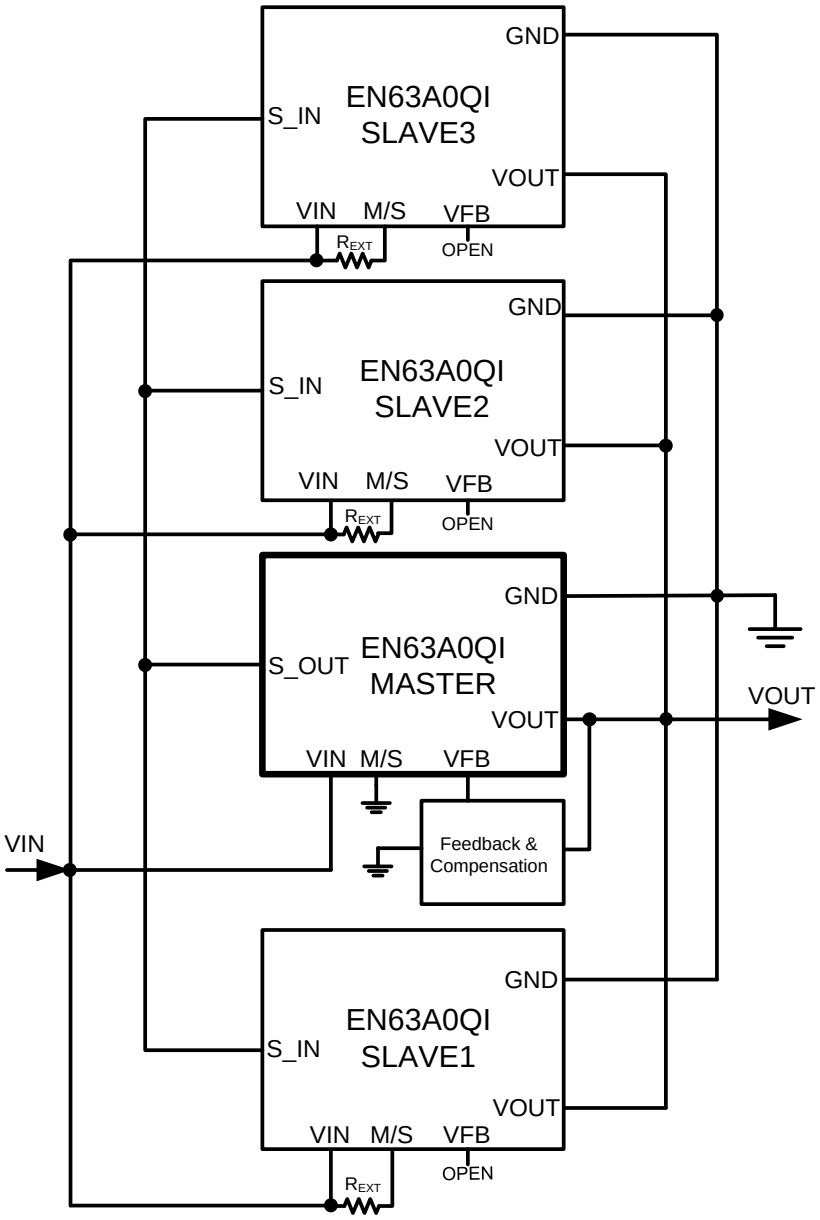


Figure 5. Master/Slave Parallel Operation Diagram

POK Operation

The POK signals that the output voltage is within the specified range. The POK signal is asserted high when the rising output voltage crosses 92% (nominal) of the programmed output voltage. If the output voltage falls outside the range of 90% to 120%, POK remains asserted for the de-glitch time (213µs at 1.2MHz). After the de-glitch time, POK is de-asserted. POK is also de-asserted if the output voltage exceeds 120% of the programmed output voltage.

Over-Current Protection (OCP)

The current limit function is achieved by sensing the current flowing through a sense P-FET. When the sensed current exceeds the current limit, both power FETs are turned off for the rest of the switching cycle. If the over-current condition is removed, the over-current protection circuit will re-enable PWM operation. If the over-current condition persists, the circuit will continue to protect the load. The OCP trip point is nominally set as specified in the Electrical Charactrestics Table. In the event the OCP circuit trips consistently in normal operation, the device enters a hiccup mode. The device is disabled for 27ms and restarted with a normal soft-start. This cycle can continue indefinitely as long as the over current condition persists.

Thermal Protection

Temperature sensing circuits in the controller will disable operation when the junction temperature exceeds the thermal shutdown temperature. Once the junction temperature drops to a safe operating level, the converter will re-start with a normal soft-start. The thermal shutdown temperature and hysteresis values can be found in the Thermal Charactrestic Table.

Input Under-Voltage Lock-Out

When the input voltage is below a required voltage level (V_{UVLOR}) for normal operation, the converter switching is inhibited. The lock-out threshold has hysteresis to prevent chatter. Thus when the device is operating normally, the input voltage has to fall below the lower threshold (V_{UVLOF}) for the device to stop switching.

APPLICATION INFORMATION

Output Voltage Programming and loop Compensation

The EN63A0QI output voltage is programmed using a simple resistor divider network. A phase lead capacitor plus a resistor are required for stabilizing the loop. Figure 6 shows the required components and the equations to calculate their values.

The EN63A0QI output voltage is determined by the voltage presented at the VFB pin. This voltage is set by way of a resistor divider between VOUT and AGND with the midpoint going to VFB.

The EN63A0QI uses a type IV compensation network. Most of this network is integrated. However, a phase lead capacitor and a resistor are required in parallel with upper resistor of the external feedback network (Refer to Figure 1, Figure 6). Total compensation is optimized for use with three 47µF output capacitance and will result in a wide loop bandwidth and excellent load transient performance for most applications. Additional capacitance may be placed beyond the voltage sensing point outside the control loop. Voltage mode operation provides high noise immunity at light load. Furthermore, voltage mode control provides superior impedance matching to ICs processed in sub 90nm technologies.

In some cases modifications to the compensation or output capacitance may be required to optimize device performance such as transient response, ripple, or hold-up time. The EN63A0QI provides the capability to modify the control loop response to allow for customization for such applications. For more information, visit https://www.altera.com/support.html.

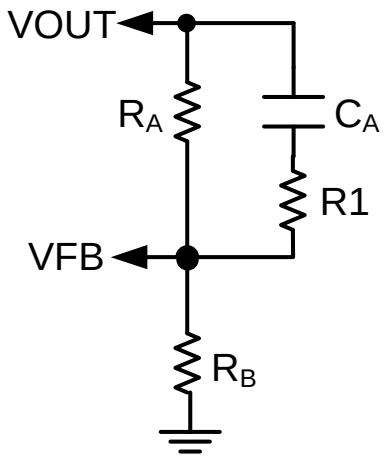


Figure 6: External Feedback/Compensation Network

The feedback and compensation network values depend on the input voltage and output voltage. Calculate the external feedback and compensation network values with the equations below.

R_A [Ω] = 48,400 x V_{IN} [V]

R_B[Ω] = (V_{FB} x R_A) / (V_{OUT} – V_{FB}) [V]

V_{FB} = 0.6V nominal

*Round R_A & R_B up to closest standard value

C_A [F] = 4.6 x 10^{-6} / R_A [Ω]

*Round C_A down to closest standard value

R1 = 12kΩ

The feedback resistor network should be sensed at the last output capacitor close to the device. Keep the trace to VFB pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Input Capacitor Selection

The EN63A0QI has been optimized for use with two 1206 47µF input capacitors. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

In some applications, lower value ceramic capacitors may be needed in parallel with the larger capacitors in order to provide high frequency decoupling. The capacitors shown in Table 3 are typical input capacitors. Other capacitors with similar characteristics may also be used.

Table 3: Recommended Input Capacitors

DESCRIPTION	MFG	P/N
47µF, 10V, 20%, X5R, 1206 (2 capacitors needed)	Murata	GRM31CR61A476ME19L
	Taiyo Yuden	LMK316BJ476ML-T

Output Capacitor Selection

The EN63A0QI has been optimized for use with three 1206 47µF output capacitors. Low ESR, X5R or X7R ceramic capacitors are recommended as the primary choice. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage. The capacitors shown in Table 4 are typical output capacitors. Other capacitors with similar characteristics may also be used. Additional bulk capacitance from 100µF to 1000µF may be placed beyond the voltage sensing point outside the control loop. This additional capacitance should have a minimum ESR of 6mΩ to ensure stable operation. Most tantalum capacitors will have more than 6mΩ of ESR and may be used without special care. Adding distance in layout may help increase the ESR between the feedback sense point and the bulk capacitors.

Table 4: Recommended Output Capacitors

DESCRIPTION	MFG	P/N
47µF, 10V, 20%, X5R, 1206 (3 capacitors needed)	Taiyo Yuden	LMK316BJ476ML-T
47µF, 6.3V, 20%, X5R, 1206 (3 capacitors needed)	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK316BJ476ML-T
10µF, 6.3V, 10%, X7R, 0805 (Optional 1 capacitor in parallel with 3x47µF)	Murata	GRM21BR70J106KE76L
	Taiyo Yuden	JMK212B7106KG-T

Output ripple voltage is primarily determined by the aggregate output capacitor impedance. Placing multiple capacitors in parallel reduces the impedance and hence will result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Table 5. Typical Ripple Voltages

Output Capacitor Configuration	Typical Output Ripple (mVp-p)
3 x 47 µF	<5mV

† 20 MHz bandwidth limit measured on Evaluation Board

M/S - Ternary Pin

M/S is a ternary pin. This pin can assume 3 states – A low state (0V to 0.7V), a high state (1.8V to VIN) and a float state (1.1V to 1.4V). Device operation is controlled by the state of the pin. The pins may be pulled to ground or left floating without any special care. When pulling high to VIN, a series resistor is recommended. The resistor value may be optimized to reduce the current drawn by the pin. The resistance should not be too high as in that case the pin may not recognize the high state. The recommend resistance (R_{EXT}) value is given in Table 6.

Table 6. Recommended R_{EXT} Resistor

V_{IN} (V)	I_{MAX} (µA)	R_{EXT} (kΩ)
2.5 – 4.0	117	15
4.0 – 6.6	88	51

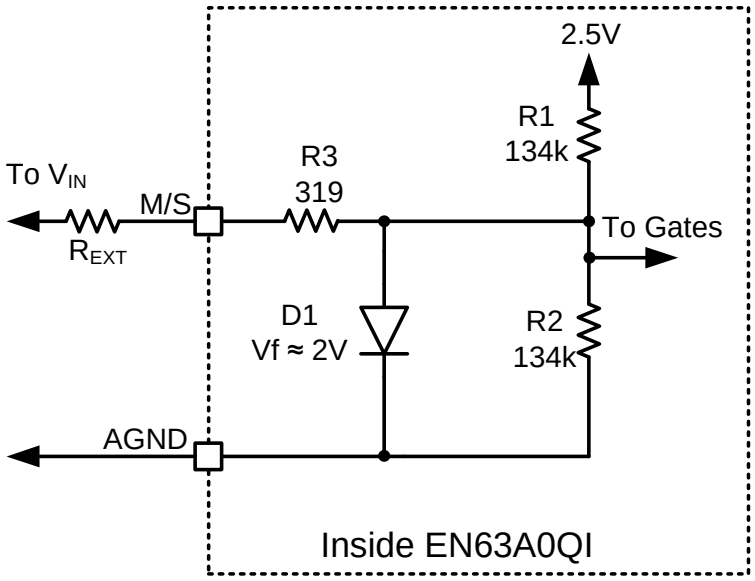


Figure 7. Selection of R_{EXT} to Connect M/S pin to V_{IN}

Table 7. M/S (Master/Slave) Pin States

M/S Pin	Function
Low (0V to 0.7V)	M/S pin is pulled to ground directly. This is the Master mode. Switching PWM phase will lock onto S_IN external clock if a signal is available. S_OUT outputs a version of the internal switching PWM signal.
Float (1.1V to 1.4V)	M/S pin is left floating. Parallel operation is not feasible. Switching PWM phase will lock onto S_IN external clock if a signal is available. S_OUT outputs a version of the internal switching PWM signal.
High (>1.8V)	M/S pin is pulled to VIN with R_{EXT}. This is the Slave mode. The S_IN signal of the Slave should connect to the S_OUT of the Master device. This signal synchronizes the switching frequency and duty cycle of the Master to the Slave device.

Power-Up Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. Tying all three pins together meets these requirements.

THERMAL CONSIDERATIONS

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Altera Enpirion PowerSoC helps alleviate some of those concerns.

The Altera Enpirion EN63A0QI DC-DC converter is packaged in an 10x11x3mm 76-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The following example and calculations illustrate the thermal performance of the EN63A0QI.

Example:

V_{IN} = 5V

V_{OUT} = 1.8V

I_{OUT} = 12A

First calculate the output power.

P_{OUT} = 1.8V x 12A = 21.6W

Next, determine the input power based on the efficiency (η) shown in Figure 8.

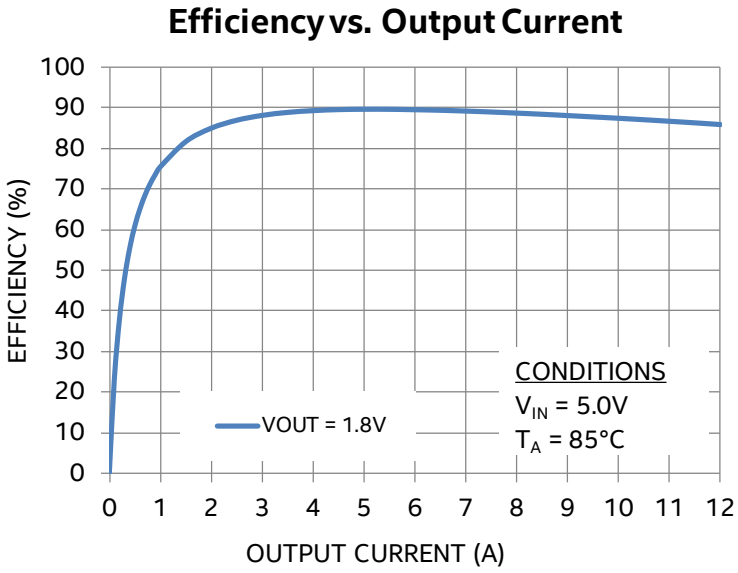


Figure 8: Efficiency vs. Output Current

η = P_{OUT} / P_{IN} = 85% = 0.85

P_{IN} = P_{OUT} / η

P_{IN} ≈ 21.6W / 0.85 ≈ 25.41W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 25.41W – 21.6 ≈ 3.81W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN63A0QI has a θ_{JA} value of 14 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

$\Delta T = P_D \times \theta_{JA}$

$\Delta T \approx 3.81W \times 14°C/W = 53.36°C \approx 53°C$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J = T_A + \Delta T$

$T_J \approx 25°C + 53°C \approx 78°C$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} - P_D \times \theta_{JA}$

$\approx 125°C - 53°C \approx 72°C$

The maximum ambient temperature the device can reach is 72°C given the input and output conditions. Note that the efficiency used in this example is at 85°C ambient temperature and is a worst case condition. Refer to the de-rating curves in the Typical Performance Curves section.

ENGINEERING SCHEMATIC

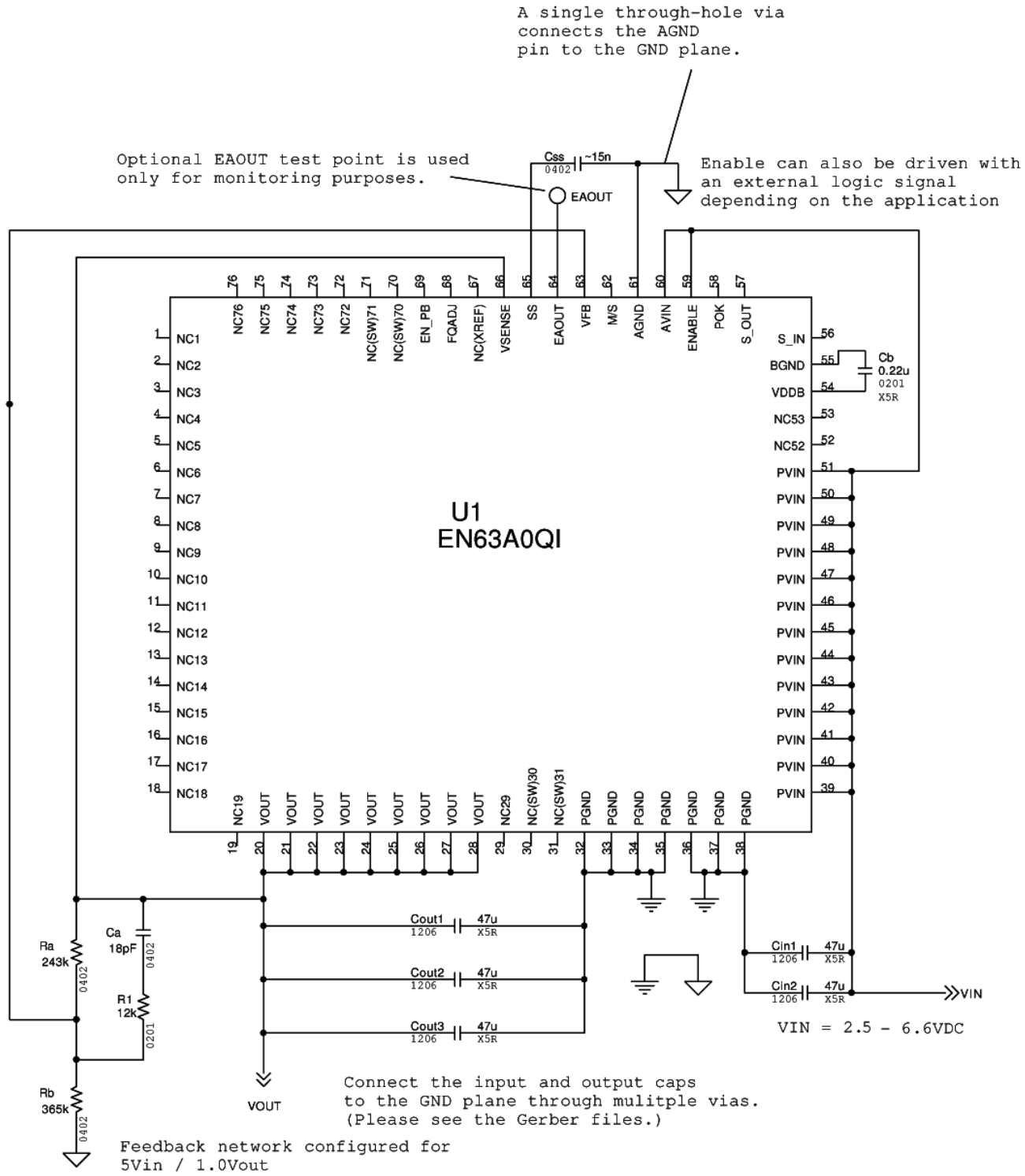


Figure 9. Engineering Schematic with Engineering Notes

LAYOUT RECOMMENDATIONS

Figure 10 shows the critical components and top layer traces for minimum footprint in single-supply mode with ENABLE tied to AVIN. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at www.altera.com/powersoc for details on all layers.

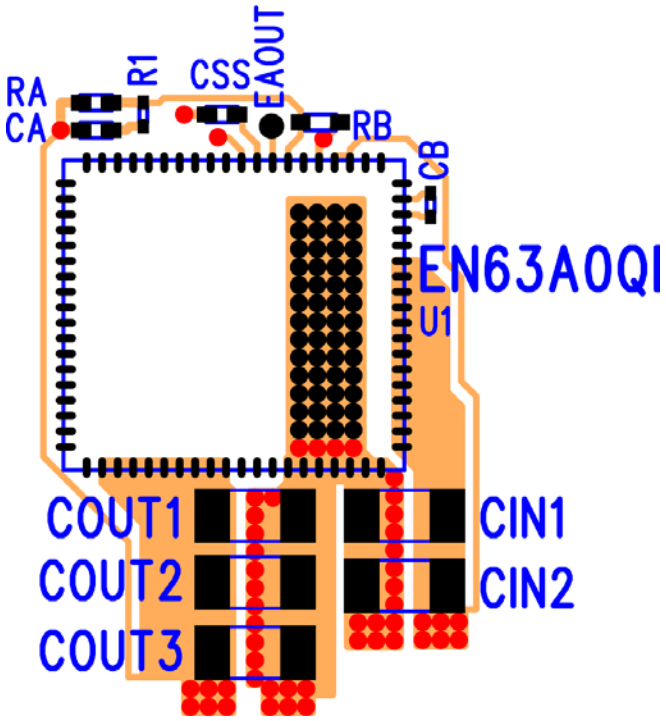


Figure 10. Top Layout with Critical Components Only (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN63A0QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN63A0QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 6: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure this connection is made at the input capacitor.
Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure . Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.
Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.
Recommendation 9: Keep R_A, C_A, R_B, and R_1 close to the VFB pin (Refer to Figure). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Recommendation 10: Follow all the layout recommendations as close as possible to optimize performance. Not following layout recommendations can complicate designs and create anomalies different than the expected operation of the product.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 11.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN63A0QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 11 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the General QFN Package Soldering Guidelines for more details and recommendations.

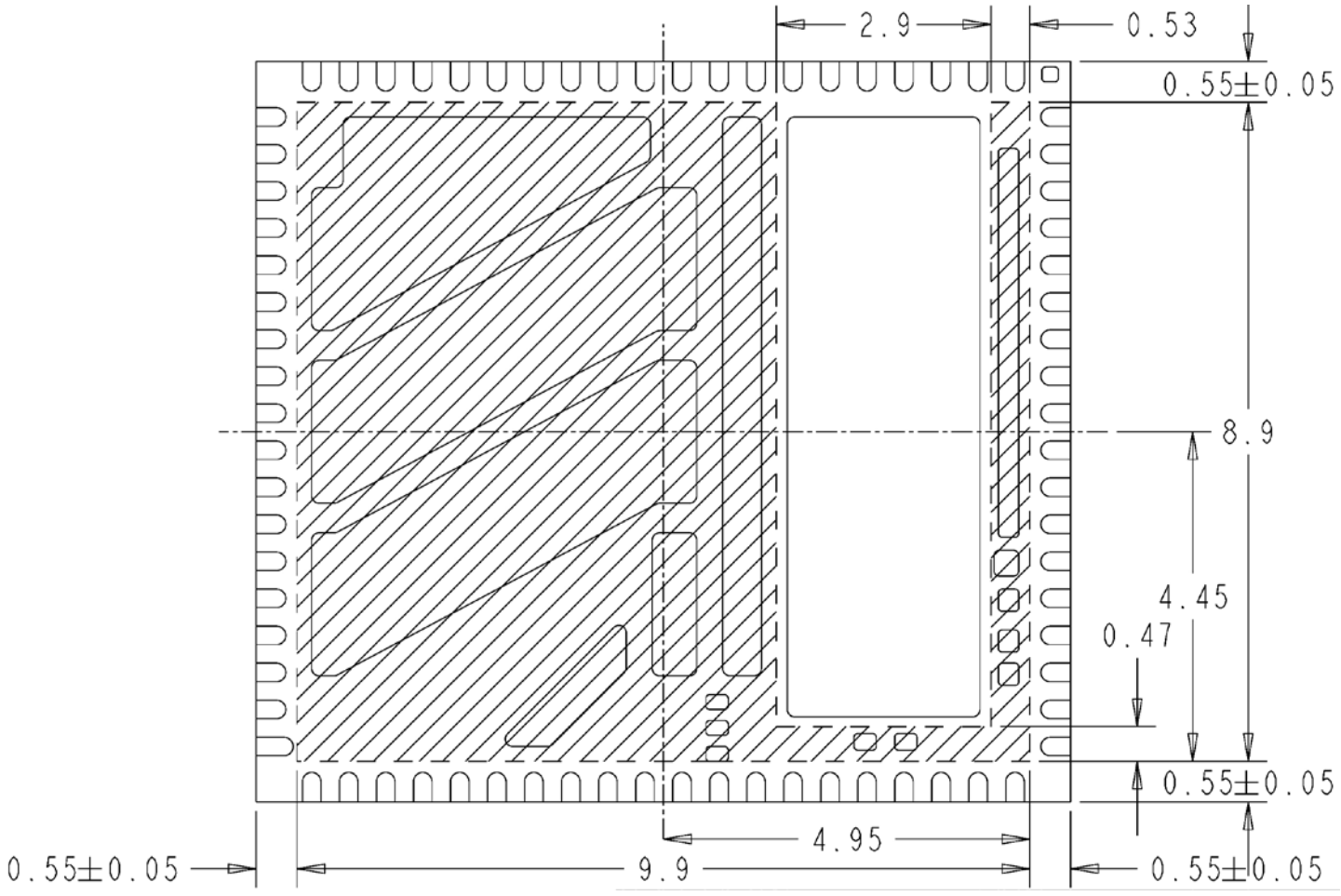


Figure 11: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

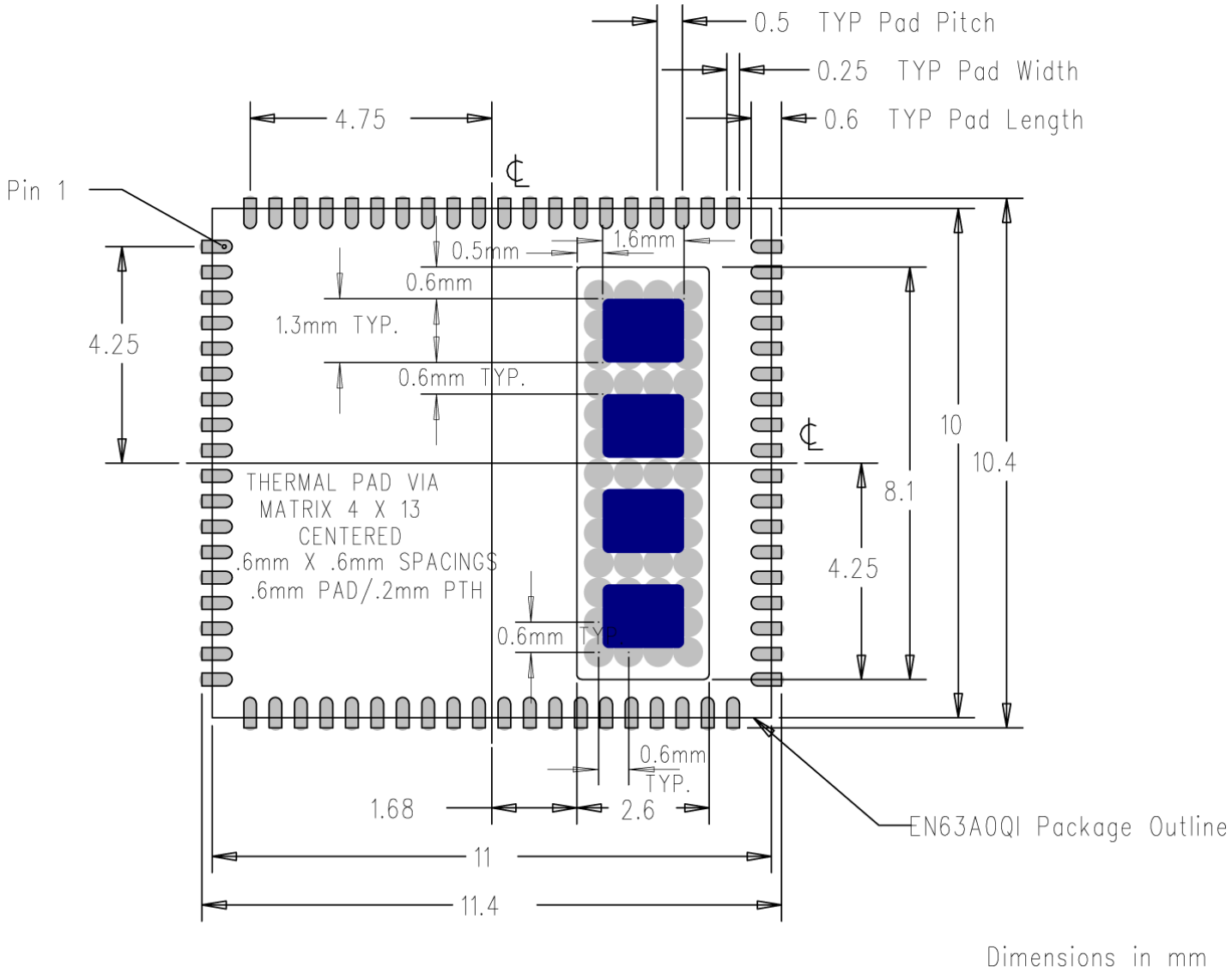


Figure 12: Landing Pattern with Solder Stencil (Top View)

The solder stencil aperture for the thermal PGND pad is shown in Figure 12 and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

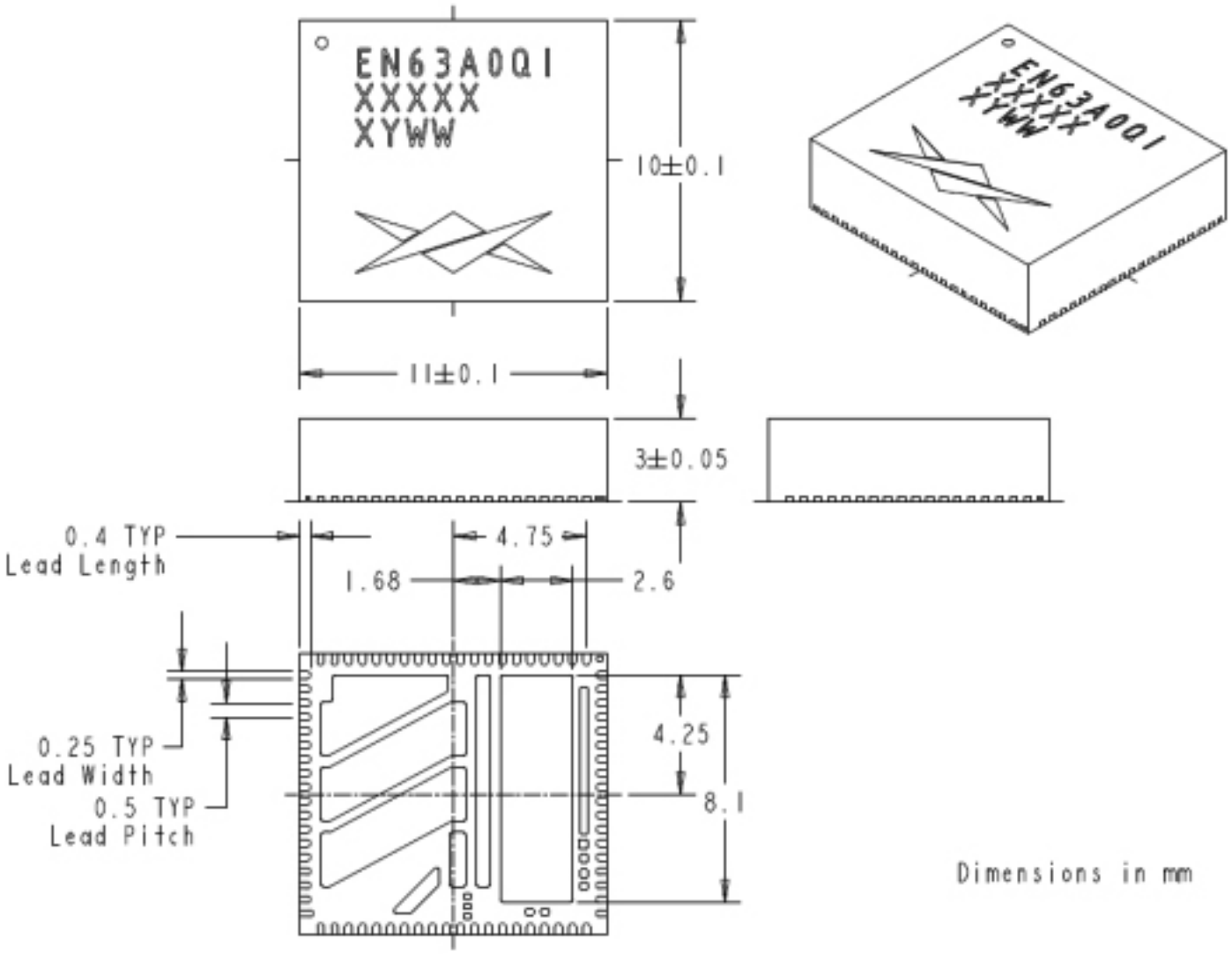


Figure 13: EN63A0QI Package Dimensions

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
B	May 2012	• Introductory production datasheet
C	May 2012	• Overall document reformatted and rewritten for better clarity • Added simplified application schematic • Added Keep Out area in pinout diagram • Added thermal operating range • Added maximum dropout voltage and resistance values • Added various performance characteristic curves and waveforms • Removed soft-shutdown from soft-start description • Added block diagram on parallel operation • Modified recommended input and output capacitor values • Added sections on engineering schematic and thermal calculations • Added stencil aperture description
D	Oct 2013	• Formatting changes
E	May 2014	• Changed a typo in EN_PB pull up section so that the resistance is 94k instead of 120k
F	Dec 2014	• Added a row into the EC table where the line voltage was removed in the VFB accuracy spec • Removed contact Altera applications support statements
G	March 2015	• Added 1.5% Load Regulation over temperature onto the front page • Changed the VFB leakage current spec to ±10nA • Updated the Block Diagram PMOS so that substrate is connected to source
H	April 2016	• Modified pin 55 description (changed refer to pin from 46 to 54) • Changed Vout vs Iout (5Vin, 3V3out) curve (limited to Iout of 10A) • Modified CISPR EMI performance horizontal and vertical scan curves • Changed parallel current share mis-match and breakdown curves (limited to 20A) • Modified thermal overload protection section • Corrected typo in thermal considerations section (efficiency calculation – 87% to 85% in equations) • Modified Engineering schematic (added Rfqadj) • Formatting changes
I	May 2018	• Changed into Intel format • Corrected R_{FADJ} in Table 2 for 5.0VIN & 6.0VIN

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.altera.com/enpirion