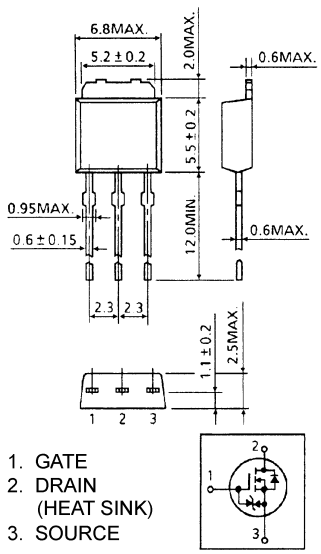
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSV)

2SK3472

Switching Regulator Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 4.0 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 0.8 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (max) (V_{DS} = 450 V)
- Enhancement-model: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	SC-64
TOSHIBA	2-7B1B

Weight: 0.36 g (typ.)

Maximum Ratings (Tc = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	450	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	450	V
Gate-source voltage		V_{GSS}	±30	V
Drain current	DC (Note 1)	I_D	1	A
	Pulse (Note 1)	I_{DP}	2	A
Drain power dissipation		P_D	20	W
Single pulse avalanche energy (Note 2)		E_{AS}	122	mJ
Avalanche current		I_{AR}	1	A
Repetitive avalanche energy (Note 3)		E_{AR}	2	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	6.25	°C/W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	125	°C/W

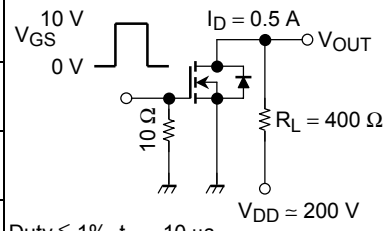
Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 203 mH, R_G = 25 Ω, I_{AR} = 1 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.

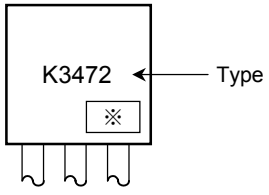
Electrical Characteristics (Tc = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±25 V, V_{DS} = 0 V	—	—	±10	μA
Drain-source breakdown voltage		$V_{(BR)\ GSS}$	I_G = ±10 μA, V_{DS} = 0 V	±30	—	—	V
Drain cut-OFF current		I_{DSS}	V_{DS} = 450 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	450	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 0.5 A	—	4.0	4.6	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 0.5 A	0.3	0.8	—	S
Input capacitance		C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	180	—	pF
Reverse transfer capacitance		C_{rss}		—	2	—	
Output capacitance		C_{oss}		—	20	—	
Switching time	Rise time	t_r		—	7	—	ns
	Turn-ON time	t_{on}		—	15	—	
	Fall time	t_f		—	30	—	
	Turn-OFF time	t_{off}		—	70	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 360 V, V_{GS} = 10 V, I_D = 1 A	—	5	—	nC
Gate-source charge		Q_{gs}		—	3	—	
Gate-drain (“miller”) charge		Q_{gd}		—	2	—	

Source-Drain Ratings and Characteristics (Tc = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	1	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	2	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 1 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 1 A, V_{GS} = 0 V, dI_{DR}/dt = 100 A/μs	—	350	—	μs
Reverse recovery charge	Q_{rr}		—	1.3	—	μC

Marking

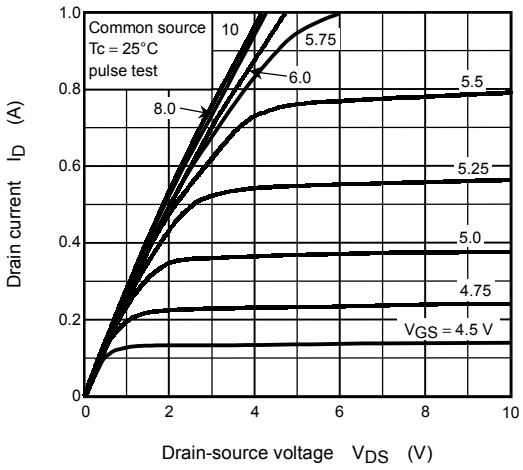


※ Lot Number

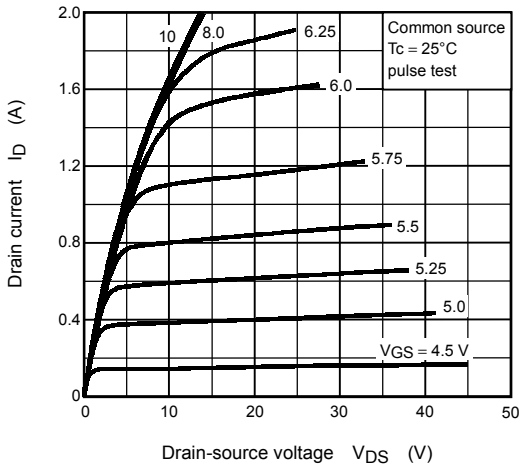
Month (starting from alphabet A)

Year (last number of the christian era)

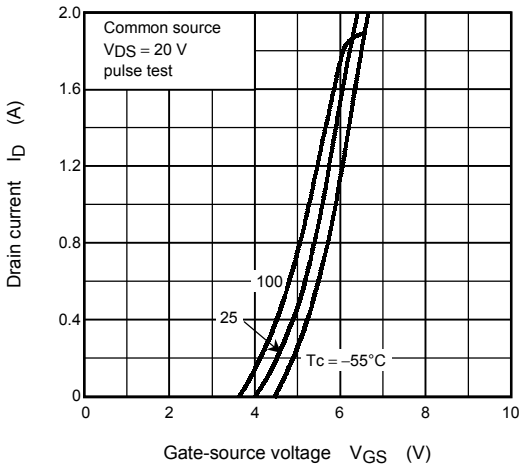
$I_D - V_{DS}$



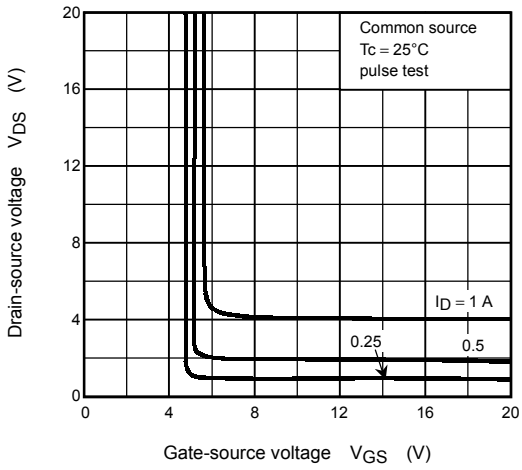
$I_D - V_{DS}$



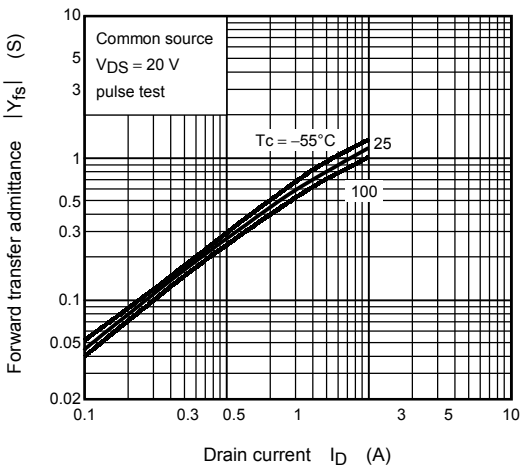
$I_D - V_{GS}$



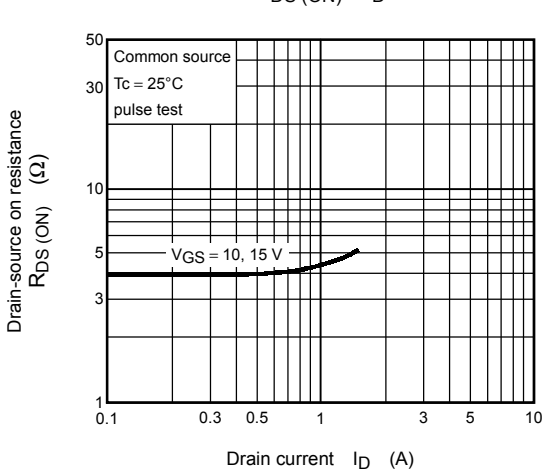
$V_{DS} - V_{GS}$



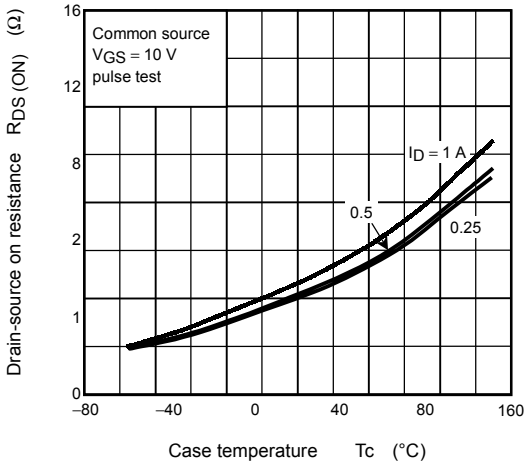
$|Y_{fs}| - I_D$



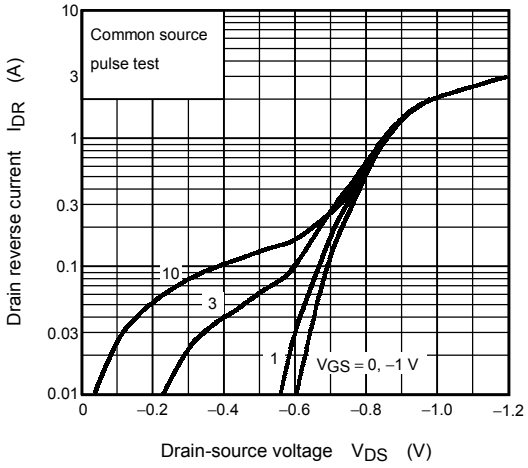
$R_{DS\ (ON)} - I_D$



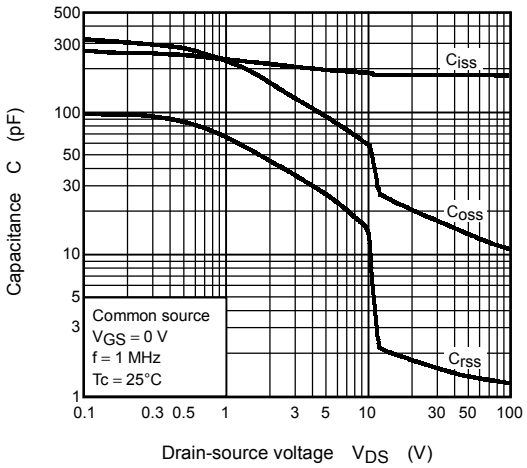
$R_{DS\ (ON)}$ – Tc



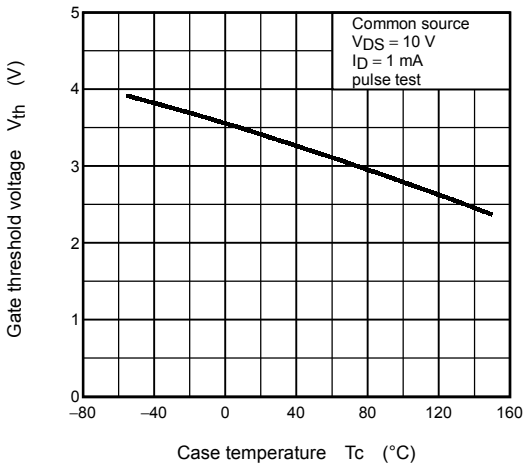
I_{DR} – V_{DS}



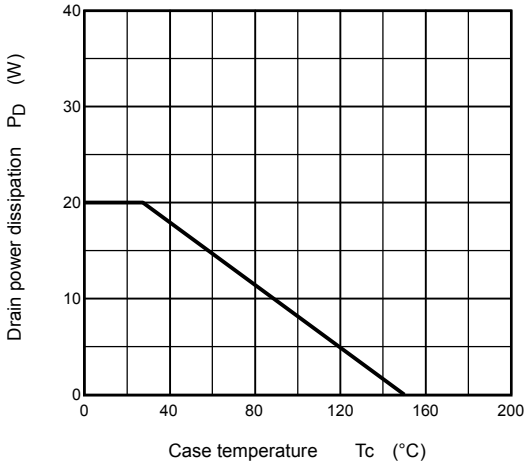
Capacitance – V_{DS}



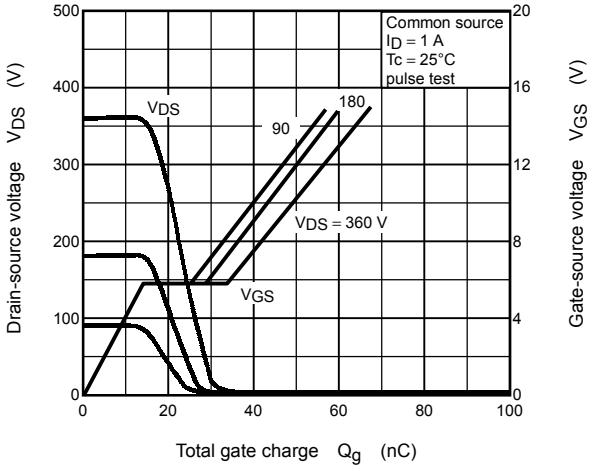
V_{th} – Tc



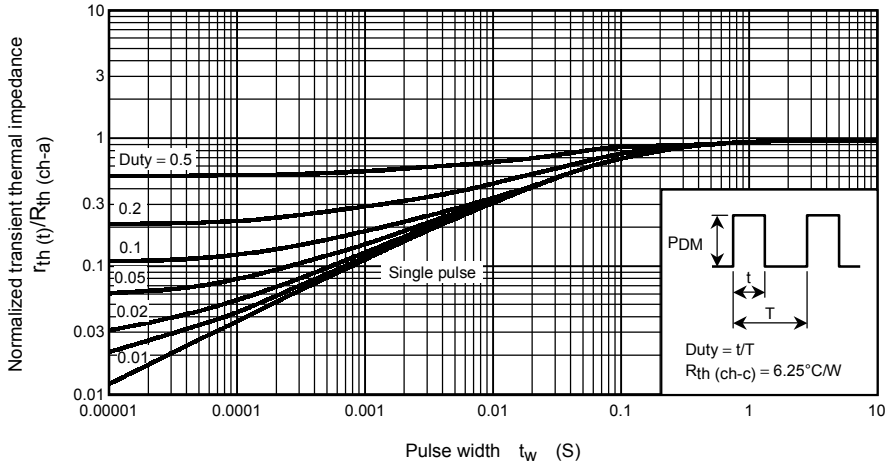
P_D – Tc



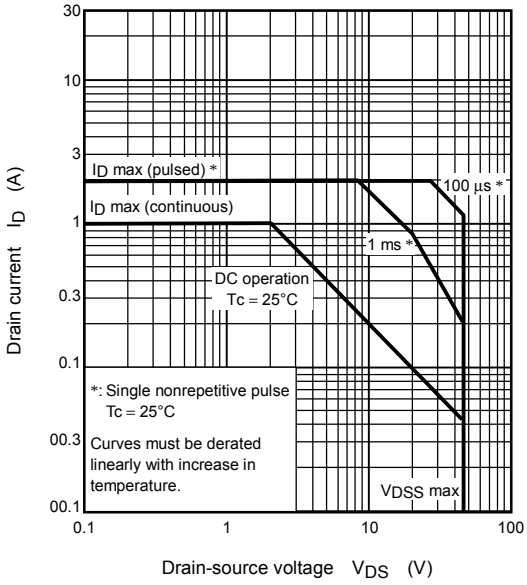
Dynamic input/output characteristics



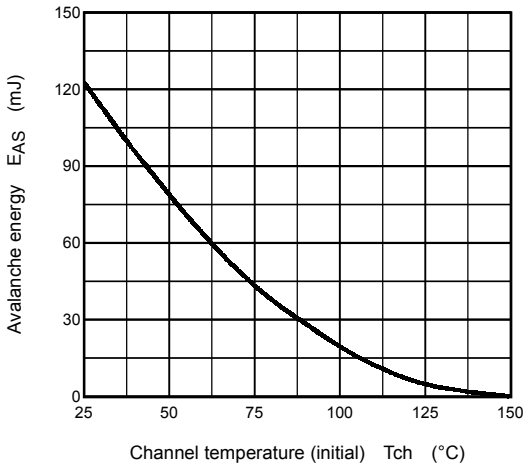
$r_{th} - t_w$

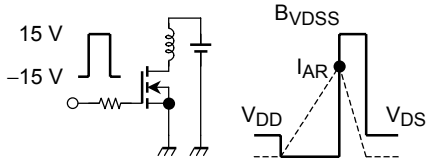


Safe operating area



$E_{AS} - T_{ch}$





Test circuit Wave form

$R_G = 25\ \Omega$
$V_{DD} = 90$ V, L = 203 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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