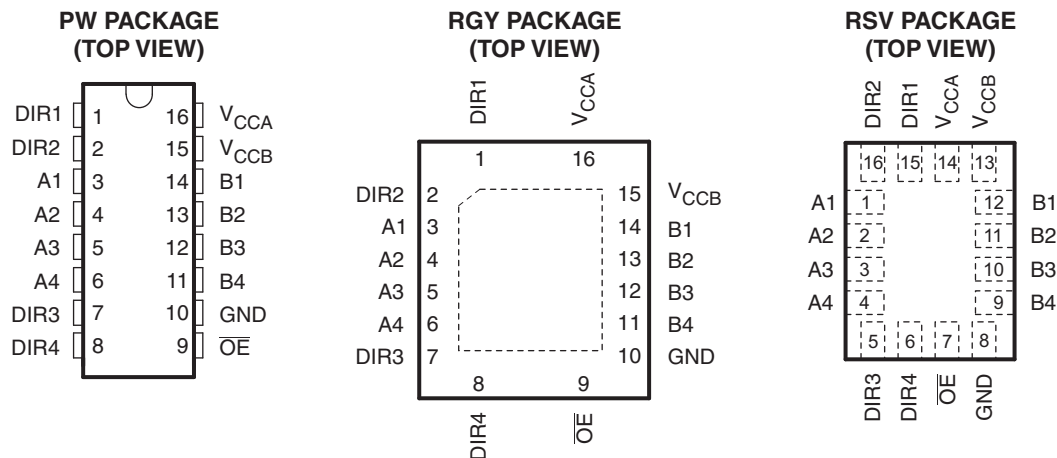


4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

FEATURES

- Each Channel Has an Independent DIR Control Input
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- I_{off} Supports Partial Power-Down-Mode Operation
- Typical Data Rates
 - 380 Mbps (1.8-V to 3.3-V Translation)
 - 200 Mbps (<1.8-V to 3.3-V Translation)
 - 200 Mbps (Translate to 2.5 V or 1.8 V)
 - 150 Mbps (Translate to 1.5 V)
 - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds the Following Levels (tested per JESD 22)
 - 8000-V Human-Body Model (A114-A)
 - 250-V Machine Model (A115-A)
 - 1500-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The SN74AVC4T774 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74AVC4T774 is designed for asynchronous communication between data buses. The logic levels of the direction-control (DIR) input and the output-enable (\overline{OE}) input activate either the B-port outputs or the A-port outputs or place both output ports in the high-impedance mode. The device transmits data from the A bus to the B bus when the B outputs are activated, and from the B bus to the A bus when the A outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

The SN74AVC4T774 is designed so that the control pins (DIR1, DIR2, DIR3, DIR4, and \overline{OE}) are supplied by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Since this device has CMOS inputs, it is very important to not allow them to float. If the inputs are not driven to either a high V_{CC} state, or a low GND state, an undesirable larger than expected I_{CC} current may result. Since the input voltage settlement is governed by many factors (e.g. capacitance, board-layout, package inductance, surrounding conditions, etc.), ensuring that they these inputs are kept out of erroneous switching states and tying them to either a high or a low level minimizes the leakage-current.

ORDERING INFORMATION

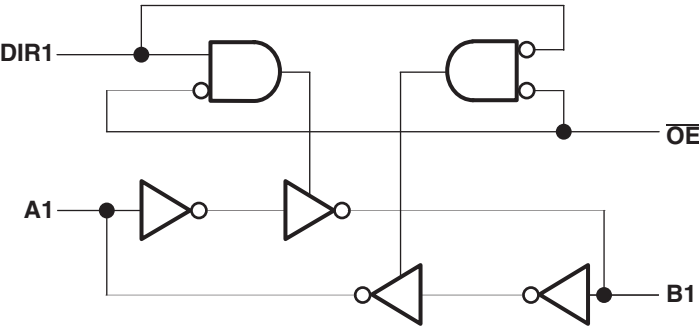
T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AVC4T774RGYR	WT774
	QFN – RSV	Tape and reel	SN74AVC4T774RSVR	ZVK
	TSSOP – PW	Tube	SN74AVC4T774PW	WT774
		Tape and reel	SN74AVC4T774PWR	

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE
(Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
\overline{OE}	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)⁽¹⁾



(1) Shown for a single channel

TYPICAL APPLICATION

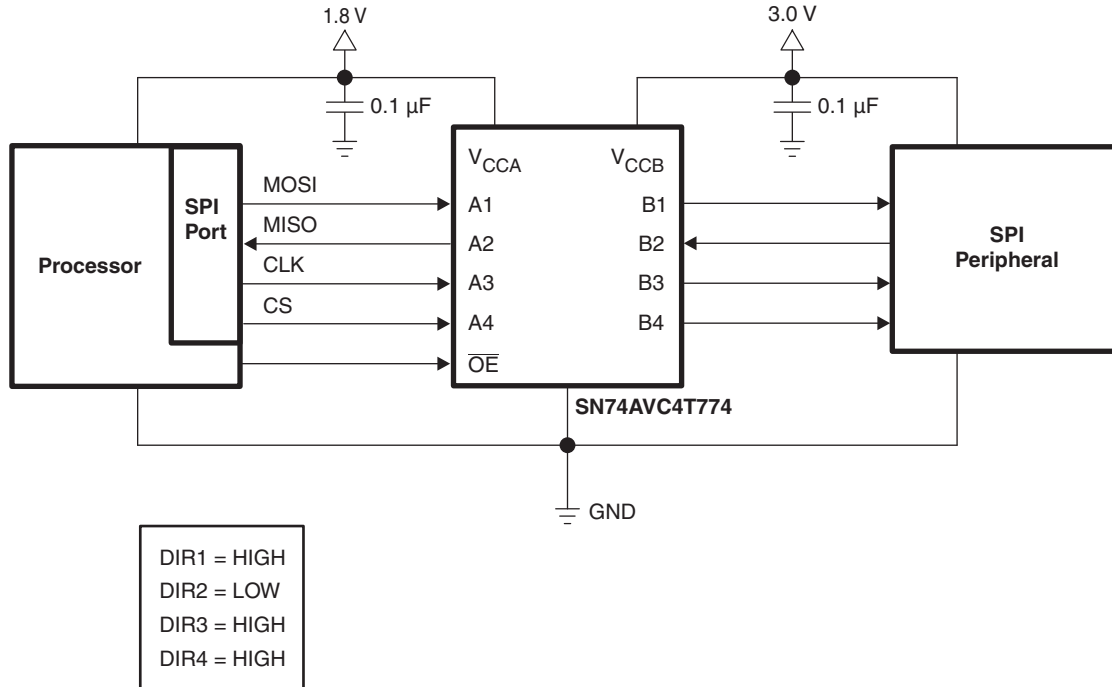


Figure 1. Typical Application of the SN74AVC4T774

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CCA} V _{CCB}	Supply voltage range	−0.5	4.6	V
V _I	Input voltage range ⁽²⁾	I/O ports (A port)	−0.5	4.6
		I/O ports (B port)	−0.5	4.6
		Control inputs	−0.5	4.6
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	A port	−0.5	4.6
		B port	−0.5	4.6
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	A port	−0.5	V _{CCA} + 0.5
		B port	−0.5	V _{CCB} + 0.5
I _{IK}	Input clamp current	V _I < 0	−50	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CCA} , V _{CCB} , or GND		±100	mA
T _{stg}	Storage temperature range.	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

PACKAGE THERMAL IMPEDANCE

			UNIT	
θ_{JA}	Package thermal impedance	PW package ⁽¹⁾	108	°C/W
		RGY package ⁽²⁾	39	
		RSV package ⁽¹⁾	184	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

(2) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾⁽²⁾⁽³⁾

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
V _{CCB}	Supply voltage				1.2	3.6	V
V _{IH}	High-level input voltage	Data inputs ⁽⁴⁾	1.2 V to 1.95 V		V _{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.2 V to 1.95 V		V _{CCI} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _{IH}	High-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾ (DIRx, \overline{OE})	1.2 V to 1.95 V		V _{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾ (DIRx, \overline{OE})	1.2 V to 1.95 V		V _{CCA} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _I	Input voltage				0	3.6	V
V _O	Output voltage	Active state			0	V _{CCO}	V
		3-state			0	3.6	
I _{OH}	High-level output current			1.1 V to 1.2 V		−3	mA
				1.4 V to 1.6 V		−6	
				1.65 V to 1.95 V		−8	
				2.3 V to 2.7 V		−9	
				3 V to 3.6 V		−12	
I _{OL}	Low-level output current			1.1 V to 1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T _A	Operating free-air temperature				−40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V

(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7$ V, V_{IL} max = $V_{CCA} \times 0.3$ V

ELECTRICAL CHARACTERISTICS⁽¹⁾⁽²⁾⁽³⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				$V_{CCO} - 0.2$		V
	$I_{OH} = -3\ \text{mA}$		1.2 V	1.2 V		0.95				
	$I_{OH} = -6\ \text{mA}$		1.4 V	1.4 V				1.05		
	$I_{OH} = -8\ \text{mA}$		1.65 V	1.65 V				1.2		
	$I_{OH} = -9\ \text{mA}$		2.3 V	2.3 V				1.75		
	$I_{OH} = -12\ \text{mA}$		3 V	3 V				2.3		
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
	$I_{OL} = 3\ \text{mA}$		1.2 V	1.2 V		0.25				
	$I_{OL} = 6\ \text{mA}$		1.4 V	1.4 V					0.35	
	$I_{OL} = 8\ \text{mA}$		1.65 V	1.65 V					0.45	
	$I_{OL} = 9\ \text{mA}$		2.3 V	2.3 V					0.55	
	$I_{OL} = 12\ \text{mA}$		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	1.2 V to 3.6 V	1.2 V to 3.6 V		± 0.025	± 0.25		± 1	μA
I_{off}	A or B port	V_I or $V_O = 0$ to 3.6 V	0 V	0 V to 3.6 V		± 0.1	± 1		± 5	μA
			0 V to 3.6 V	0 V		± 0.1	± 1		± 5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$	3.6 V	3.6 V		± 0.5	± 2.5		± 5	μA
I_{CCA}		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
			0 V	0 V to 3.6 V					-2	
			0 V to 3.6 V	0 V					8	
I_{CCB}		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
			0 V	0 V to 3.6 V					8	
			0 V to 3.6 V	0 V					-2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V					16	μA
C_i	Control inputs	$V_I = 3.3\ \text{V}$ or GND	3.3 V	3.3 V		2.5			3	pF
C_{io}	A or B port	$V_O = 3.3\ \text{V}$ or GND	3.3 V	3.3 V		5			6	pF

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) V_{CCI} is the V_{CC} associated with the input port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 1.2\text{ V}$ (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.5	2.8	2.7	2.7	3.1	ns
t_{PHL}			3.5	2.8	2.7	2.7	3.1	
t_{PLH}	B	A	3.8	3.4	3.2	3	2.9	ns
t_{PHL}			3.8	3.4	3.2	3	2.9	
t_{PZH}	\overline{OE}	A	6	4.8	4.4	5.3	9.3	ns
t_{PZL}			6	4.8	4.4	5.3	9.3	
t_{PZH}	\overline{OE}	B	6.7	6.7	6.6	6.7	6.6	ns
t_{PZL}			6.7	6.7	6.6	6.7	6.6	
t_{PHZ}	\overline{OE}	A	4.3	3.6	3.7	3.3	4	ns
t_{PLZ}			4.3	3.6	3.7	3.3	4	
t_{PHZ}	\overline{OE}	B	4.4	4.4	4.4	4.4	4.4	ns
t_{PLZ}			4.4	4.4	4.4	4.4	4.4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.1	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	ns
t_{PHL}			3.1	0.3	4.4	0.2	3.9	0.1	3.6	0.1	3.9	
t_{PLH}	B	A	2.9	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	ns
t_{PHL}			2.9	0.6	5.1	0.4	4.9	0.2	4.6	0.1	4.5	
t_{PZH}	\overline{OE}	A	5.3	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	ns
t_{PZL}			5.3	1.1	7.1	0.9	6.2	0.7	5.5	0.1	6.4	
t_{PZH}	\overline{OE}	B	4.4	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	ns
t_{PZL}			4.4	1.1	8.2	1.1	8.2	1.1	8.2	1.1	8.2	
t_{PHZ}	\overline{OE}	A	3.6	1.2	4.8	0.8	5.4	0.4	5.1	1	5.4	ns
t_{PLZ}			3.6	1.2	4.8	0.8	5.4	0.4	5.1	1	5.4	
t_{PHZ}	\overline{OE}	B	3.1	0.3	5.6	0.2	5.7	0.3	5.6	0.3	5.6	ns
t_{PLZ}			3.1	0.3	5.6	0.2	5.7	0.3	5.6	0.3	5.6	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.8	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	ns
t_{PHL}			2.8	0.1	4.1	0.1	3.6	0.1	3.1	0.1	3.3	
t_{PLH}	B	A	2.6	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	ns
t_{PHL}			2.6	0.4	4.3	0.1	4.1	0.1	3.8	0.1	3.7	
t_{PZH}	\overline{OE}	A	5	0.8	6.7	0.6	5.8	0.4	4.8	0.3	4.6	ns
t_{PZL}			5	0.8	6.7	0.6	5.8	0.4	4.8	0.3	4.6	
t_{PZH}	\overline{OE}	B	3.3	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	ns
t_{PZL}			3.3	0.2	6.7	0.2	6.6	0.2	6.7	0.2	6.7	
t_{PHZ}	\overline{OE}	A	3.4	0.7	4.7	0.3	5.1	0.1	4.5	0.8	5	ns
t_{PLZ}			3.4	0.7	4.7	0.3	5.1	0.1	4.5	0.8	5	
t_{PHZ}	\overline{OE}	B	2.9	0.1	5.7	0.1	5.8	0.1	5.8	0.1	5.8	ns
t_{PLZ}			2.9	0.1	5.7	0.1	5.8	0.1	5.8	0.1	5.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	ns
t_{PHL}			2.6	0.1	3.8	0.1	3.2	0.1	2.7	0.1	2.6	
t_{PLH}	B	A	2.5	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	ns
t_{PHL}			2.5	0.5	3.4	0.2	3.1	0.1	2.8	0.1	2.6	
t_{PZH}	\overline{OE}	A	4.7	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	ns
t_{PZL}			4.7	0.7	6.2	0.5	5.2	0.3	4.1	0.3	3.6	
t_{PZH}	\overline{OE}	B	2.3	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns
t_{PZL}			2.3	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	
t_{PHZ}	\overline{OE}	A	3	0.2	4.3	0.1	4.9	0.1	4	0.7	4.3	ns
t_{PLZ}			3	0.2	4.3	0.1	4.9	0.1	4	0.7	4.3	
t_{PHZ}	\overline{OE}	B	1.9	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7	ns
t_{PLZ}			1.9	0.1	4.7	0.1	4.6	0.1	4.7	0.1	4.7	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.5	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	ns
t_{PHL}			2.5	0.1	3.6	0.1	3	0.1	2.6	0.1	2.4	
t_{PLH}	B	A	2.6	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	ns
t_{PHL}			2.6	0.5	3.4	0.2	2.9	0.1	2.5	0.1	2.3	
t_{PZH}	\overline{OE}	A	4.5	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	ns
t_{PZL}			3.8	0.9	5.9	0.5	5	0.3	3.8	0.3	3.3	
t_{PZH}	\overline{OE}	B	1.9	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	ns
t_{PZL}			1.9	0.4	3.6	0.4	3.6	0.4	3.6	0.4	3.6	
t_{PHZ}	\overline{OE}	A	2.7	0.1	4.2	0.1	4.6	0.3	3.8	0.7	3.9	ns
t_{PLZ}			2.7	0.1	4.2	0.1	4.6	0.3	3.8	0.7	3.9	
t_{PHZ}	\overline{OE}	B	2.3	0.1	4.5	0.1	4.5	0.1	4.6	0.1	4.6	ns
t_{PLZ}			2.3	0.1	4.5	0.1	4.5	0.1	4.6	0.1	4.6	

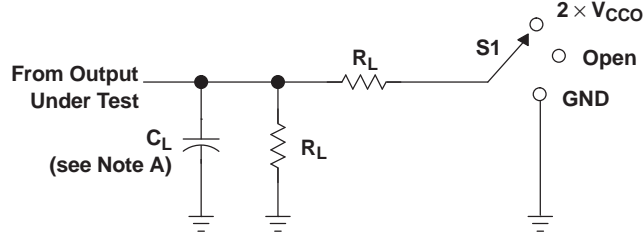
OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.2 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.5 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.8 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5 \text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3 \text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A to B	Outputs enabled	$C_L = 0,$ $f = 10 \text{ MHz},$ $t_r = t_f = 1 \text{ ns}$	3	3	3	3	4	pF
		Outputs disabled		1	1	1	2	2	
	B to A	Outputs enabled		12	13	14	15	17	
		Outputs disabled		2	2	2	2	2	
$C_{pdB}^{(1)}$	A to B	Outputs enabled	$C_L = 0,$ $f = 10 \text{ MHz},$ $t_r = t_f = 1 \text{ ns}$	12	13	14	16	17	pF
		Outputs disabled		2	2	2	2	2	
	B to A	Outputs enabled		3	3	3	3	4	
		Outputs disabled		1	1	1	2	2	

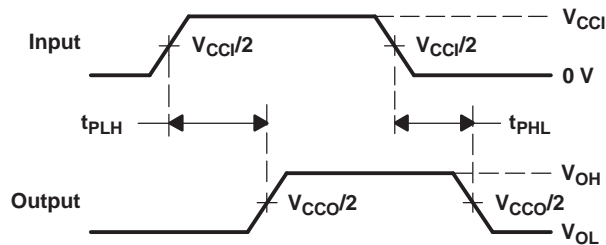
(1) Power dissipation capacitance per transceiver

PARAMETER MEASUREMENT INFORMATION



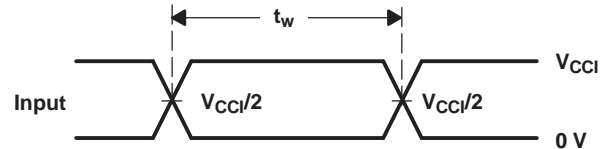
LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V

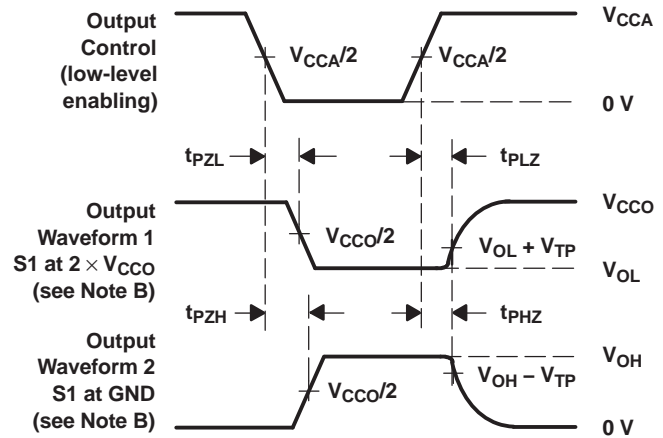


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. V_{CCI} is the V_{CC} associated with the input port.
 - I. V_{CCO} is the V_{CC} associated with the output port.

Figure 2. Load and Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T774RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774	Samples
74AVC4T774RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	Samples
SN74AVC4T774PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774	Samples
SN74AVC4T774RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC4T774PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T774RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T774RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

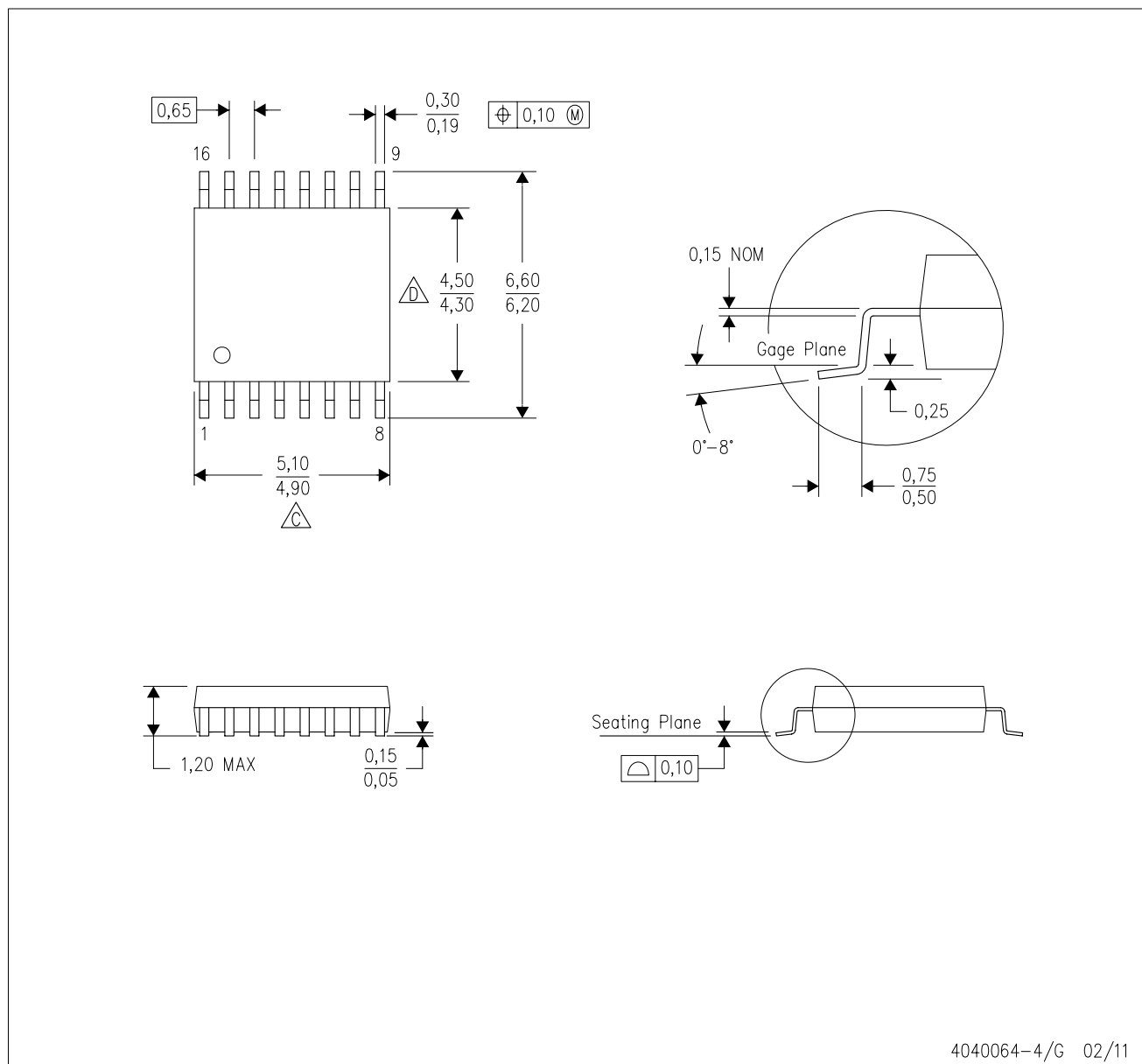


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC4T774PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74AVC4T774RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
SN74AVC4T774RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

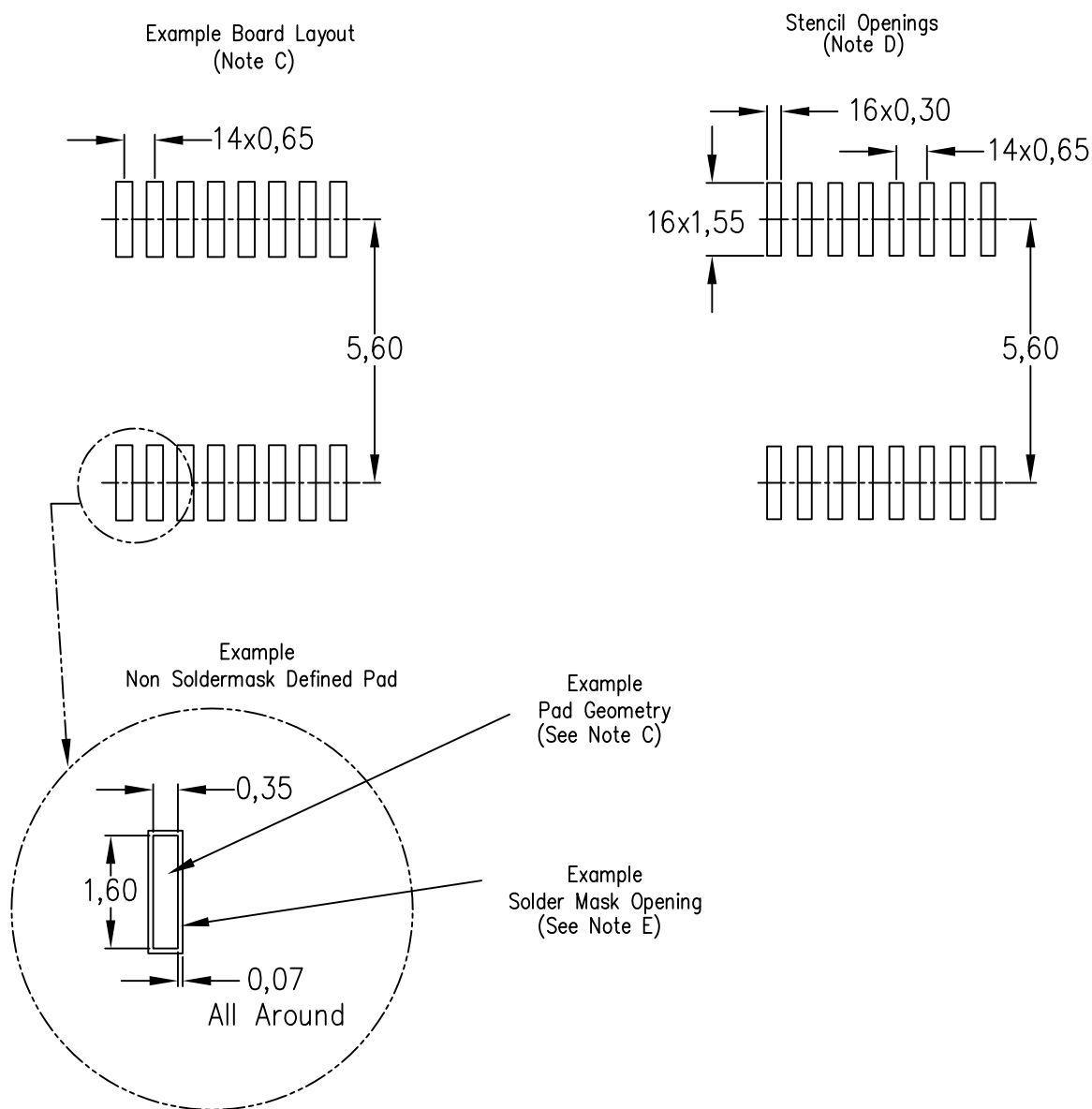


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

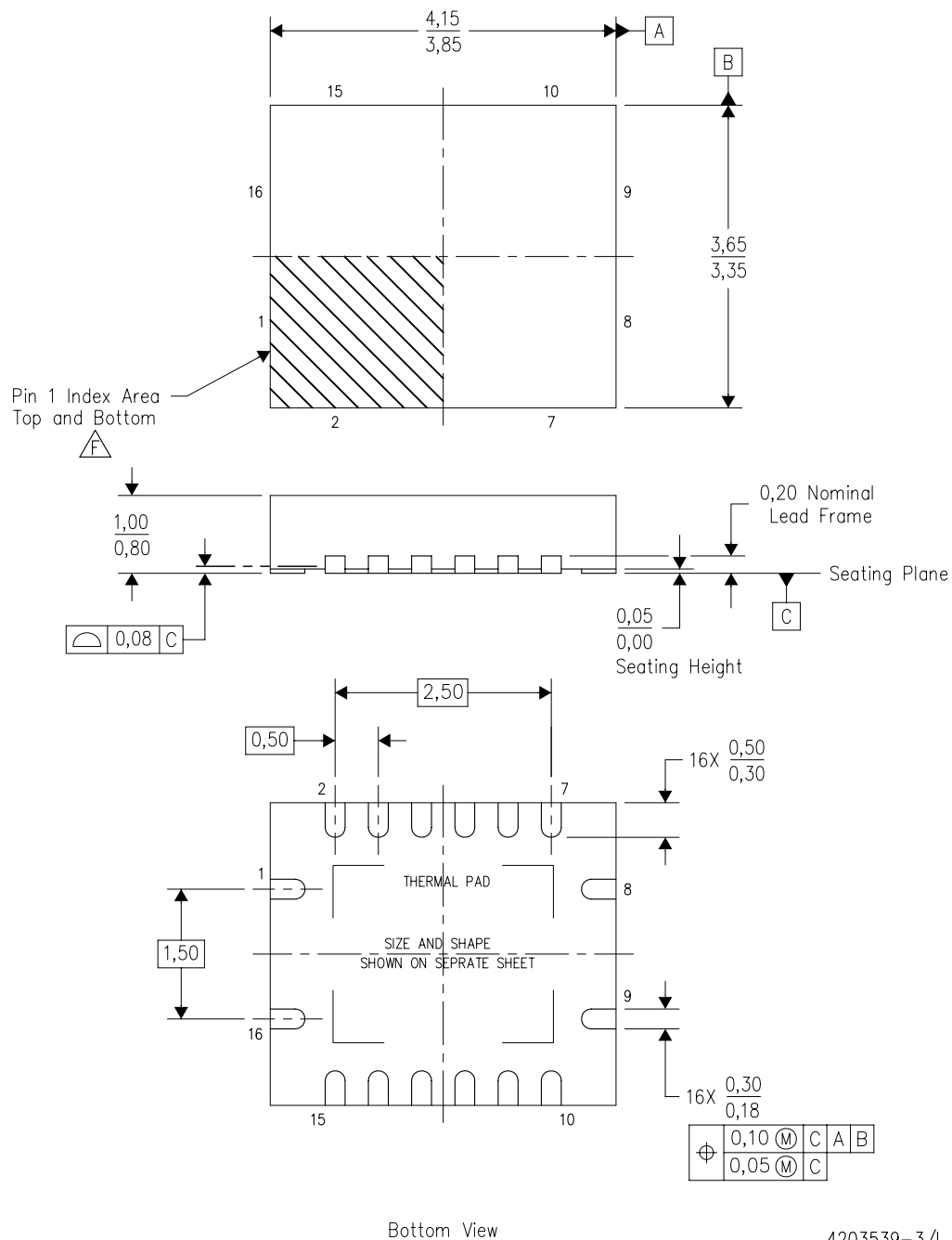


4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

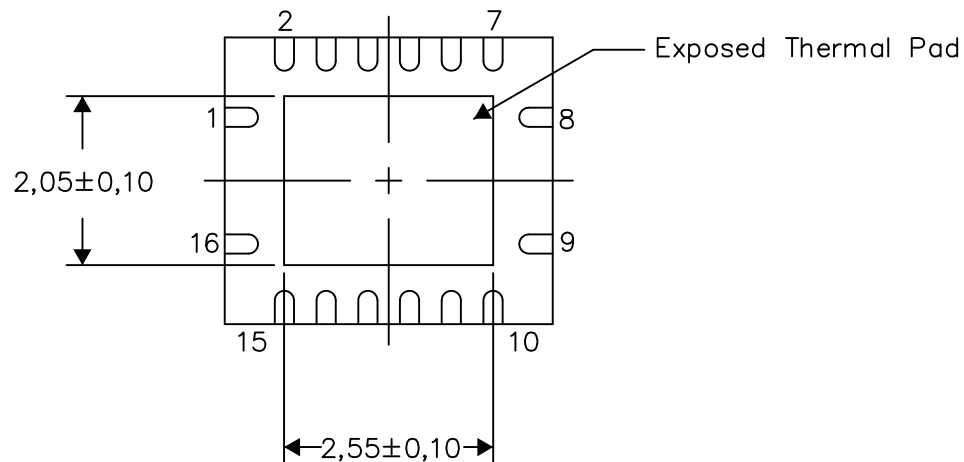
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

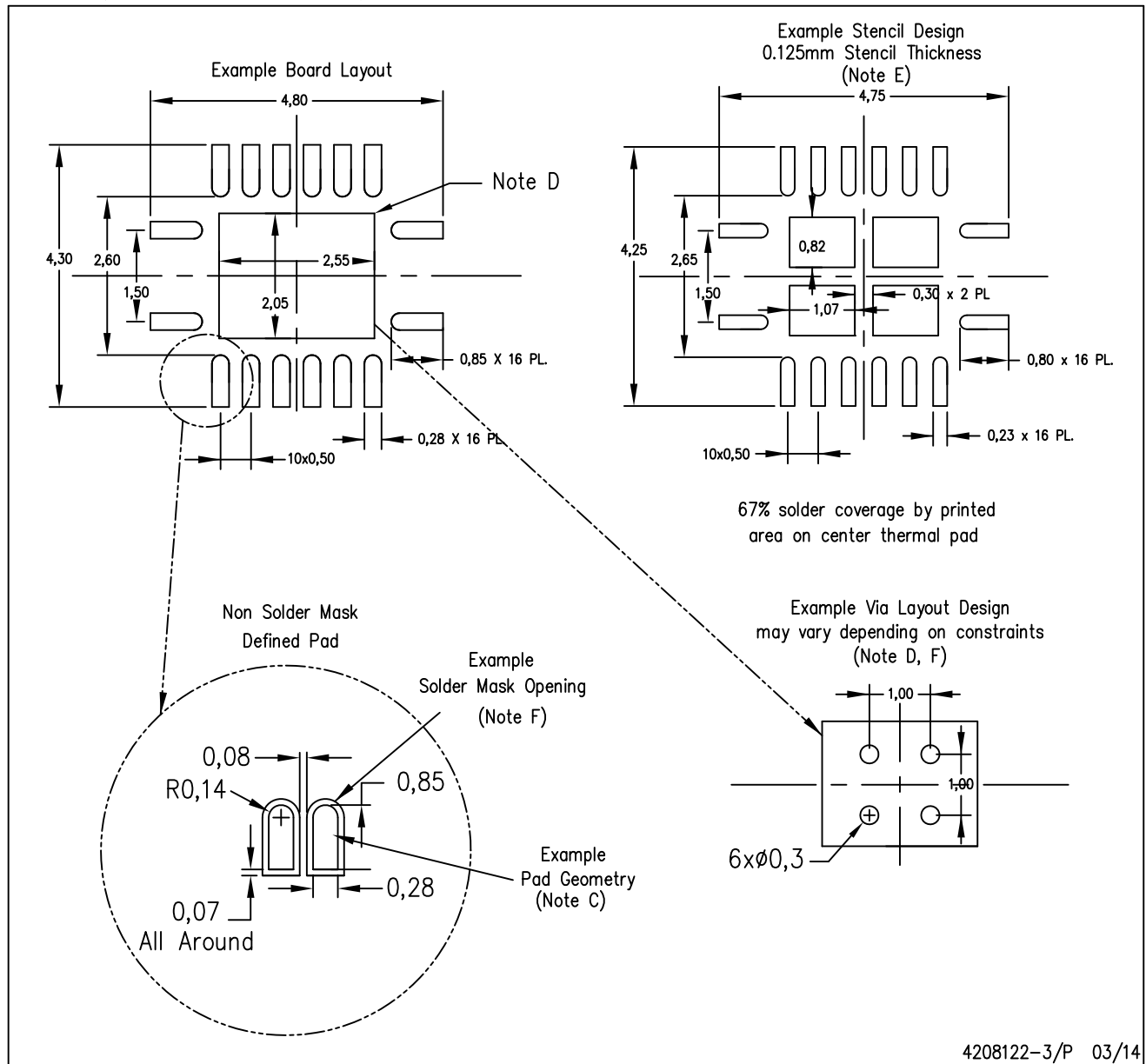
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

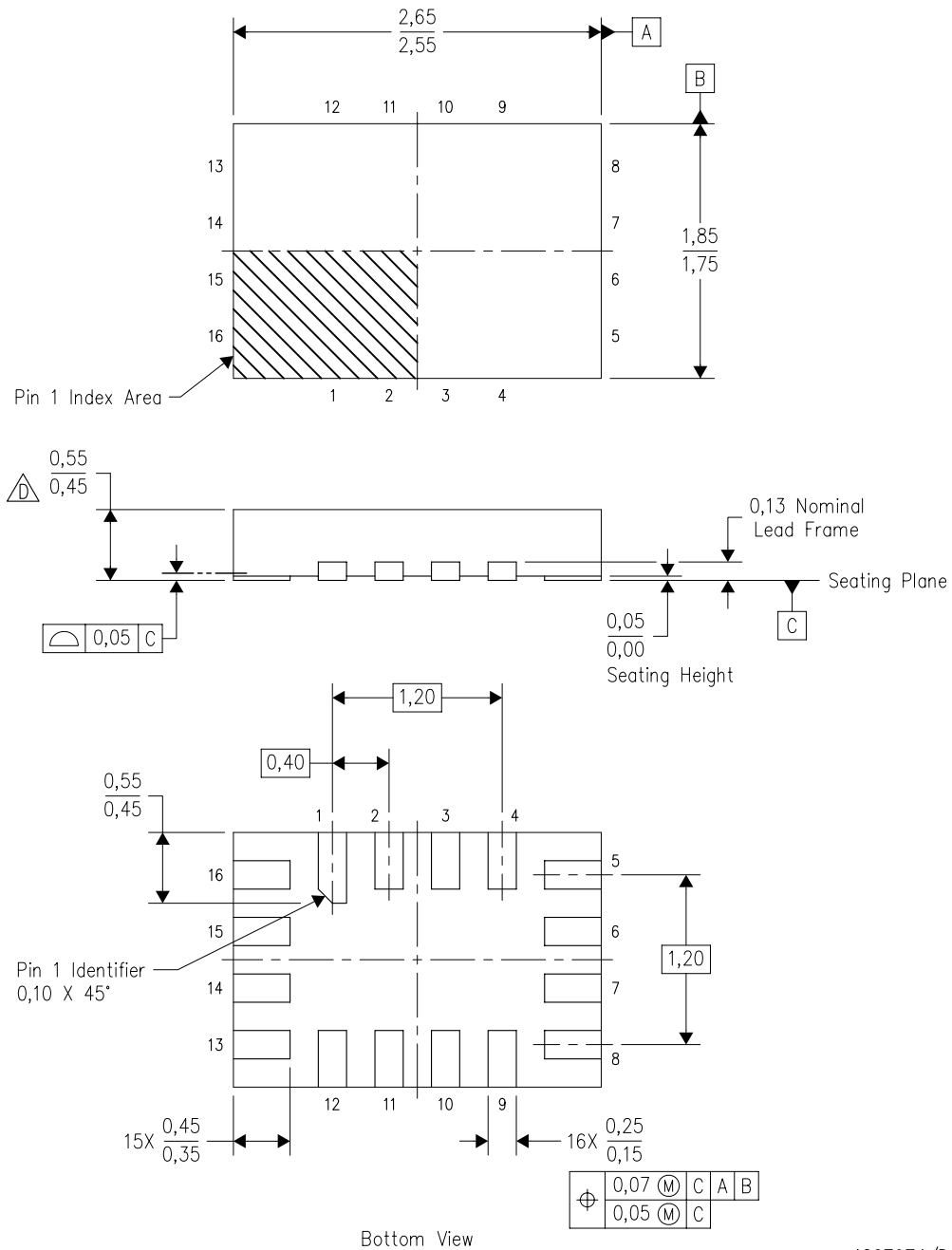
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

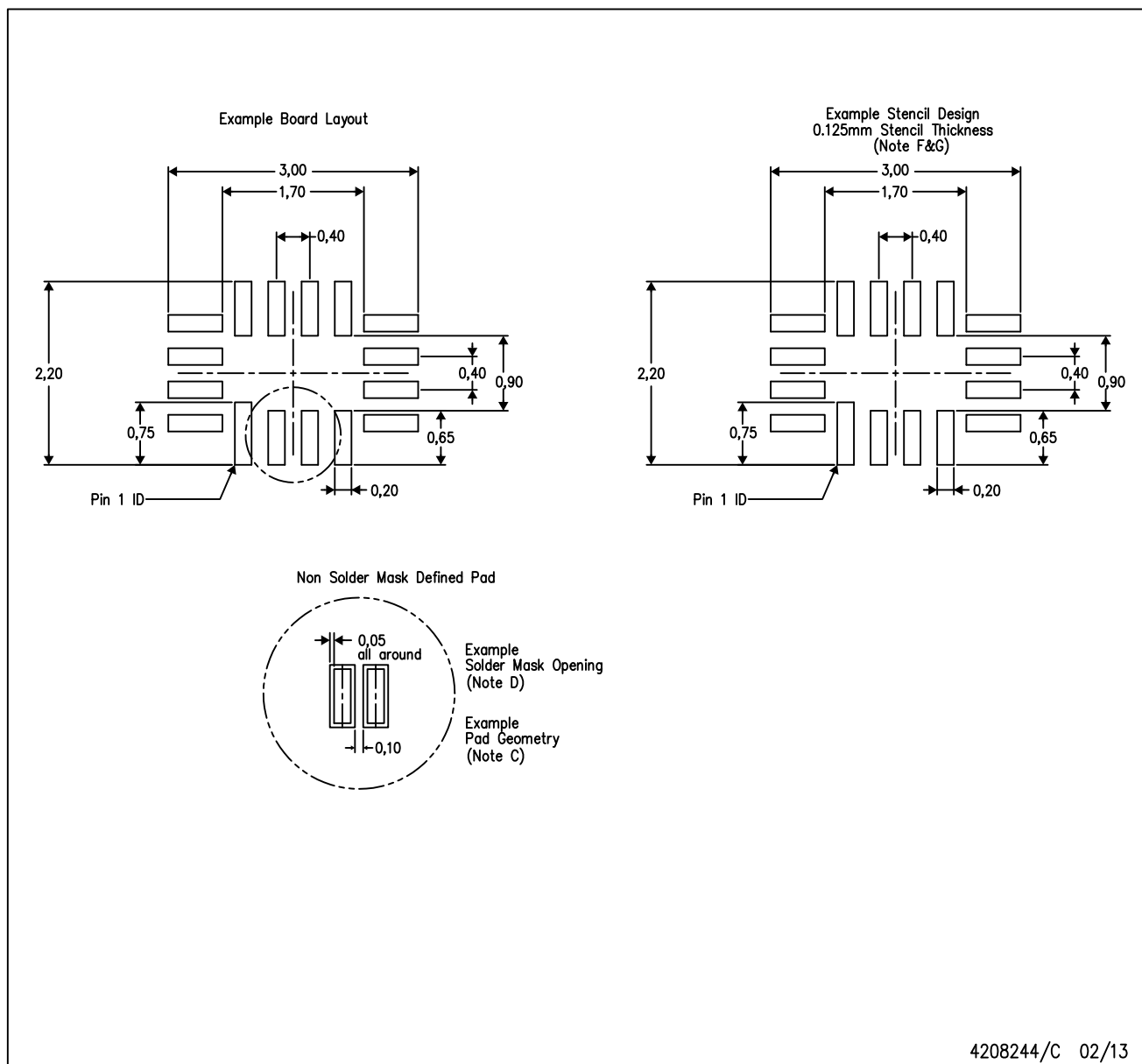


4207974/D 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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