

# 4V Drive Nch+Pch MOSFET

## SP8M8

### ●Structure

Silicon N-channel / P-channel MOSFET

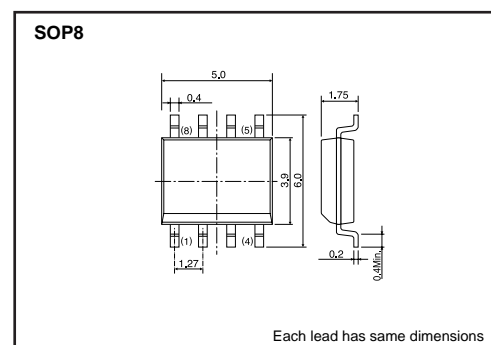
### ●Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

### ●Application

Power switching, DC / DC converter.

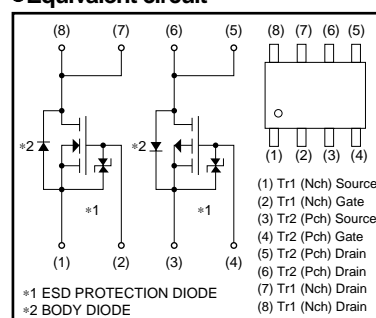
### ●Dimensions (Unit : mm)



### ●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M8		○

### ●Equivalent circuit



\*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Nchannel	Pchannel	
Drain-source voltage	$V_{DS}$	30	-30	V
Gate-source voltage	$V_{GS}$	±20	±20	V
Drain current	Continuous	$I_D$	±6.0	A
	Pulsed	$I_{DP}^{*1}$	±24	A
Source current (Body diode)	Continuous	$I_S$	1.6	A
	Pulsed	$I_{SP}^{*1}$	20	A
Total power dissipation	$P_D^{*2}$	2		W
Channel temperature	$T_{ch}$	150		°C
Storage temperature	$T_{stg}$	-55 to +150		°C

\*1  $P_w \leq 10 \mu s$ , Duty cycle  $\leq 1\%$

\*2 MOUNTED ON A CERAMIC BOARD.

### ●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th (ch-a)}^*$	62.5	°C / W

\*MOUNTED ON A CERAMIC BOARD.

## Transistors

## N-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	—	—	$\pm 10$	$\mu A$	$V_{GS}=\pm 20V$ , $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D=1mA$ , $V_{GS}=0V$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu A$	$V_{DS}=30V$ , $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	—	2.5	V	$V_{DS}=10V$ , $I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	21	30	m $\Omega$	$I_D=6.0A$ , $V_{GS}=10V$
		—	30	42		$I_D=6.0A$ , $V_{GS}=4.5V$
		—	33	47		$I_D=6.0A$ , $V_{GS}=4V$
Forward transfer admittance	$ Y_{fs} $ *	4.0	—	—	S	$I_D=6.0A$ , $V_{DS}=10V$
Input capacitance	$C_{iss}$	—	520	—	pF	$V_{DS}=10V$
Output capacitance	$C_{oss}$	—	150	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	$C_{rss}$	—	95	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	9	—	ns	$I_D=3A$ , $V_{DD}\doteq 15V$
Rise time	$t_r$ *	—	21	—	ns	$V_{GS}=10V$
Turn-off delay time	$t_{d(off)}$ *	—	36	—	ns	$R_L=5.0\Omega$
Fall time	$t_f$ *	—	13	—	ns	$R_G=10\Omega$
Total gate charge	$Q_g$ *	—	7.2	—	nC	$V_{DD}\doteq 15V$
Gate-source charge	$Q_{gs}$ *	—	1.8	—	nC	$V_{GS}=5V$
Gate-drain charge	$Q_{gd}$ *	—	2.8	—	nC	$I_D=6.0A$

\*Pulsed

## ●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	$V_{SD}$ *	—	—	1.2	V	$I_S=6.4A$ , $V_{GS}=0V$

\*Pulsed

## Transistors

## P-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	—	—	$\pm 10$	$\mu A$	$V_{GS} = \pm 20V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	$\mu A$	$V_{DS} = -30V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	—	-2.5	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	40	56	m $\Omega$	$I_D = -4.5A, V_{GS} = -10V$
		—	57	80		$I_D = -2.5A, V_{GS} = -4.5V$
		—	65	90		$I_D = -2.5A, V_{GS} = -4.0V$
Forward transfer admittance	$ Y_{fs} $ *	3.5	—	—	S	$I_D = -2.5A, V_{DS} = -10V$
Input capacitance	$C_{iss}$	—	850	—	pF	$V_{DS} = -10V$
Output capacitance	$C_{oss}$	—	190	—	pF	$V_{GS} = 0V$
Reverse transfer capacitance	$C_{rss}$	—	120	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	10	—	ns	$I_D = -2.5A, V_{DD} \doteq -15V$
Rise time	$t_r$ *	—	25	—	ns	$V_{GS} = -10V$
Turn-off delay time	$t_{d(off)}$ *	—	60	—	ns	$R_L = 6.0\Omega$
Fall time	$t_f$ *	—	25	—	ns	$R_G = 10\Omega$
Total gate charge	$Q_g$ *	—	8.5	—	nC	$V_{DD} \doteq -15V$
Gate-source charge	$Q_{gs}$ *	—	2.5	—	nC	$V_{GS} = -5V$
Gate-drain charge	$Q_{gd}$ *	—	3.0	—	nC	$I_D = -4.5A$

\*Pulsed

## ●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	$V_{SD}$	—	—	-1.2	V	$I_S = -1.6A, V_{GS} = 0V$

## Transistors

## N-ch

## ●Electrical characteristic curves

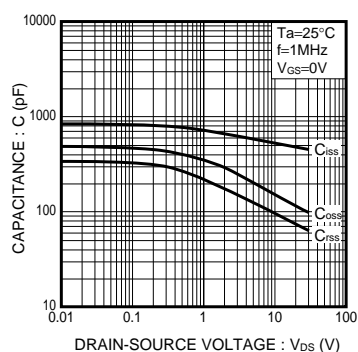


Fig.1 Typical Capacitance vs. Drain-Source Voltage

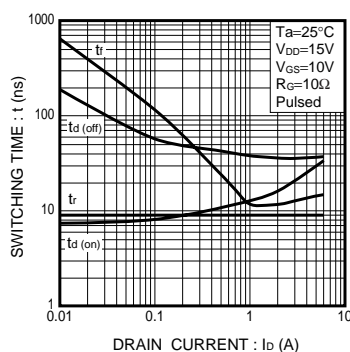


Fig.2 Switching Characteristics

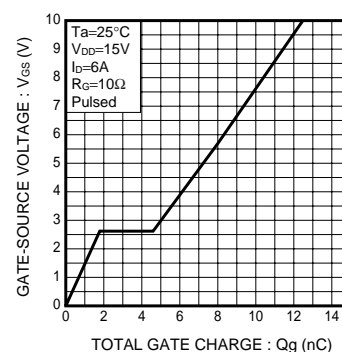


Fig.3 Dynamic Input Characteristics

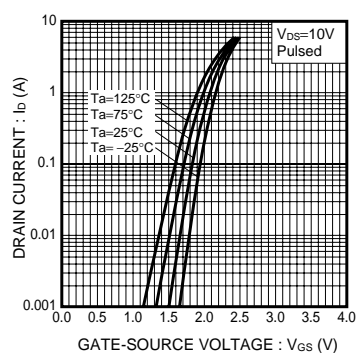


Fig.4 Typical Transfer Characteristics

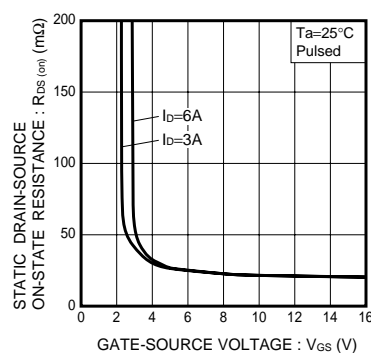


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

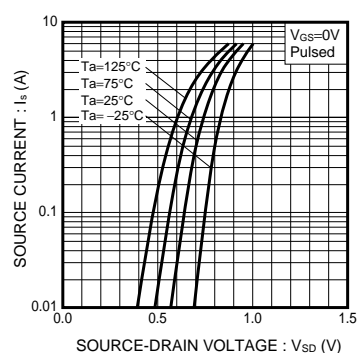


Fig.6 Source Current vs. Source-Drain Voltage

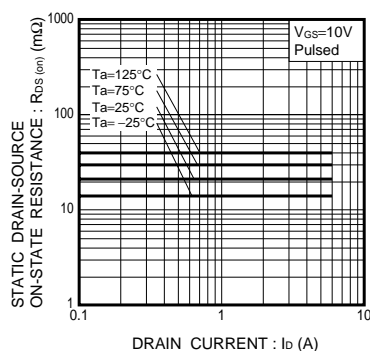


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

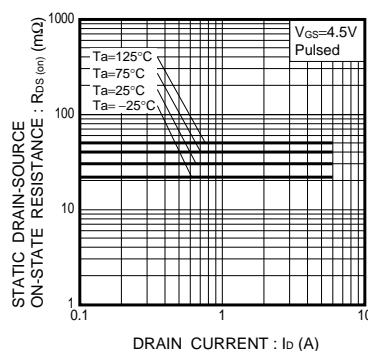


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

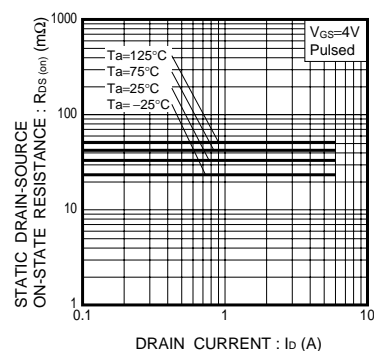


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

## Transistors

## P-ch

## ●Electrical characteristic curves

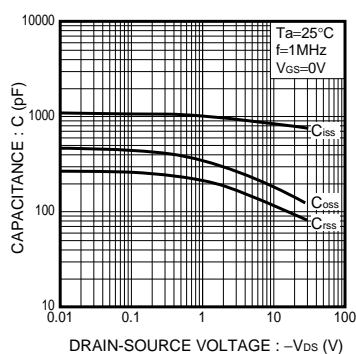


Fig.1 Typical Capacitance vs. Drain-Source Voltage

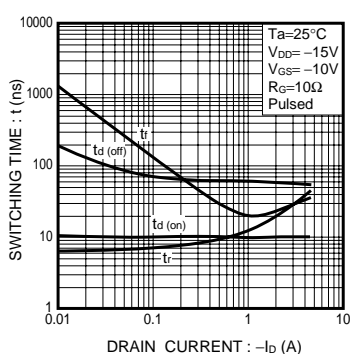


Fig.2 Switching Characteristics

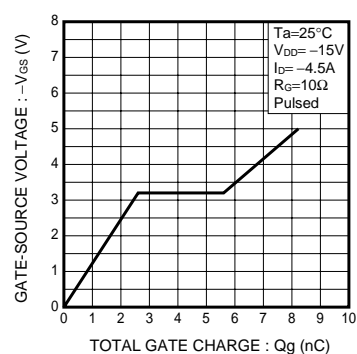


Fig.3 Dynamic Input Characteristics

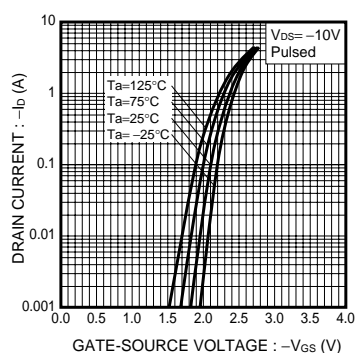


Fig.4 Typical Transfer Characteristics

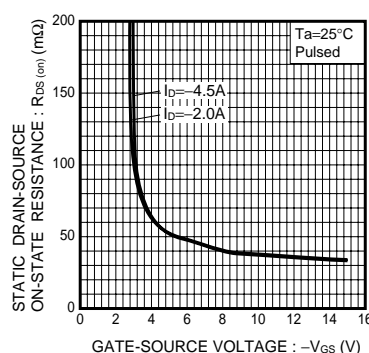


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

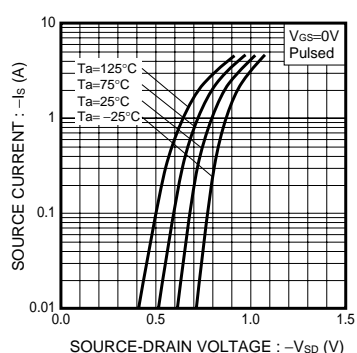


Fig.6 Source Current vs. Source-Drain Voltage

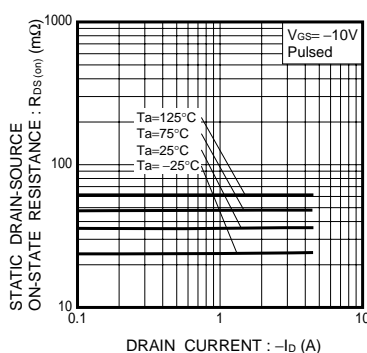


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

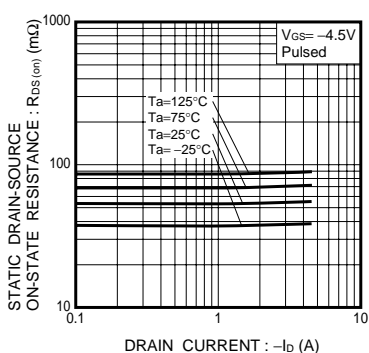


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

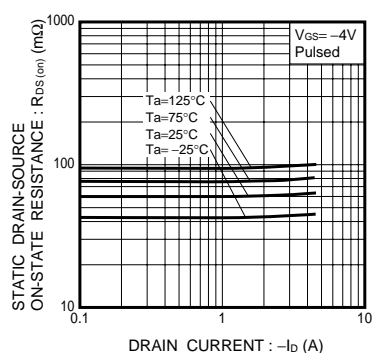


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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