National Semiconductor

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LM8272 Dual
RRIO, High Output Current & Unlimited Cap Load Op Amp in Miniature Package

General Description

The LM8272 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability while requiring only 0.95mA/channel supply current. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50dB of Common Mode Rejection, allows high side and low side sensing, among many applications, without having any concerns over exceeding the range and no compromise in accuracy. Exceptionally wide operating supply voltage range of 2.5V to 24V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in multitude of applications. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage.

The LM8272 is offered in the 8-pin MSOP package.

Features

(V_S = 12V, T_A = 25˚C, Typical values unless specified).

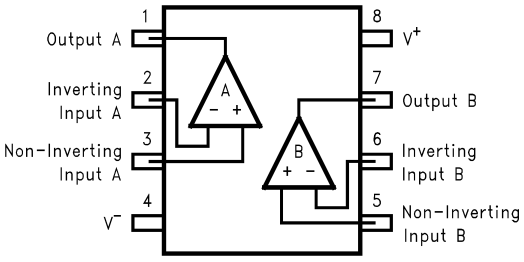
- GBWP 15MHz
- Wide supply voltage range 2.5V to 24V
- Slew rate 15V/µs
- Supply current/channel 0.95mA
- Cap load tolerance Unlimited
- Output short circuit current ±130mA
- Output current (1V from rails) ±65mA
- Input common mode voltage 0.3V beyond rails
- Input voltage noise 15nV/ $\sqrt{Hz}$
- Input current noise 1.4pA/ $\sqrt{Hz}$

Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side/low side sensing
- Headphone amplifier

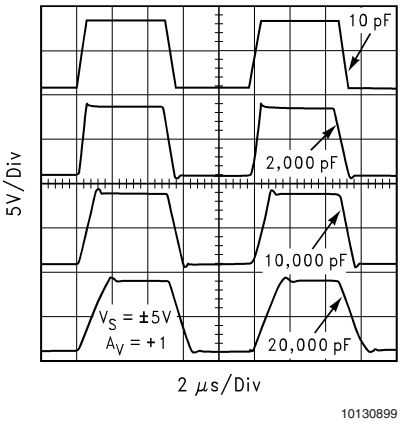
Connection Diagram

8-Pin MSOP



Top View

Large Signal Step Response for Various Cap. Load



Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin MSOP	LM8272MM	A60	1k Unit Tape and Reel	MUA08A
	LM8272MMX		3.5k Unit Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2) 200V(Note 9)
V_{IN} Differential	+/–10V
Output Short Circuit Duration	(Notes 3, 11)
Supply Voltage (V^+ - V^-)	27V
Voltage at Input/Output pins	V^+ +0.3V, V^- –0.3V
Storage Temperature Range	–65˚C to +150˚C
Junction Temperature (Note 4)	+150˚C
Soldering Information:	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C

Operating Ratings

Supply Voltage (V^+ - V^-)	2.5V to 24V
Junction Temperature Range(Note 4)	–40˚C to +85˚C
Package Thermal Resistance, θ_{JA},(Note 4)	
8-Pin MSOP	235C/W

5V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 4.5V	+/–0.7	+/–5 **+/– 7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 4.5V (Note 12)	+/–2	—	µV/˚C
I_B	Input Bias Current	(Note 7)	—	±2.00 **±2.70**	µA max
I_{OS}	Input Offset Current		20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 5V	80	64 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V	100	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–0.3	–0.1 **0.0**	V max
			5.3	5.1 **5.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10kΩ to V^+/2	80	64 **60**	dB min
V_O	Output Swing High	R_L = 10kΩ to V^-	4.93	4.85	V min
		I_{SOURCE} = 5mA	4.85	4.70	
	Output Swing Low	R_L = 10kΩ to V^+	215	250	mV max
		I_{SINK} = 5mA	300	350	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	100	—	mA
		Sinking to V^+ V_{ID} = –200mV (Note 10)	100	—	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±55	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.8	2.3 **2.8**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $5V_{PP}$	12	—	V/µs
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2KΩ to V^+/2	7.5	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	13	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	55	—	deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	$nV/\sqrt{Hz}$

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = (20pF ‖ 10kΩ) to V^+/2	700	—	KHz

12V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25˚C, V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 11.5V	+/–0.7	+/–7 **+/– 9**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 11.5V (Note 12)	+/–2	—	µV/˚C
I_B	Input Bias Current	(Note 7)	—	±2.00 **±2.80**	µA max
I_{OS}	Input Offset Current		30	275 **550**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 12V	88	74 **72**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V, V_{CM} = 0.5V	100	78 **74**	dB min
–PSRR	Negative Power Supply Rejection Ratio		85	—	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–0.3	–0.1 **0**	V max
			12.3	12.1 **12.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 11V R_L = 10kΩ to V^+/2	83	74 **70**	dB min
V_O	Output Swing High	R_L 10kΩ to V^+/2	11.8	11.7	V min
		I_{SOURCE} = 5mA	11.6	11.5	
	Output Swing Low	R_L = 10kΩ to V^+/2	0.25	0.3	V max
		I_{SINK} = 5mA	.40	.45	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	130	110	mA min
		Sinking to V^+ V_{ID} = 200mV (Note 10)	130	110	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±65	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.9	2.4 **2.9**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $10V_{PP}$, C_L = 10pF	15	—	V/µs
		A_V = +1, V_I = $10V_{PP}$, C_L = 0.1µF	1	—	
R_{OUT}	Close Loop Output Resistance	A_V = +1, f = 100KHz	3	—	Ω
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2kΩ to V^+/2	8	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	15	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	57	—	Deg
GM	Gain Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	20	—	dB

12V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25˚C, V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
–3dB BW	Small Signal -3db Bandwidth	A_V = +1, R_L = 2kΩ to $V^+/2$	12.5	—	MHz
		A_V = +1, R_L = 600Ω to $V^+/2$	10.5	—	
		A_V = +10, R_L = 600Ω to $V^+/2$	1.0	—	
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = (20pF ‖ 10kΩ) to $V^+/2$	300	—	KHz
THD+N	Total Harmonic Distortion +Noise	A_V = +2, R_L = 2kΩ to $V^+/2$ V_O = $8V_{PP}$, V_S = ±5V	0.02	—	%
CT Rej.	Cross-Talk Rejection	f = 5MHz, Driver R_L = 10kΩ to $V^+/2$	68	—	dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Note 9: Machine Model, 0Ω is series with 200pF.

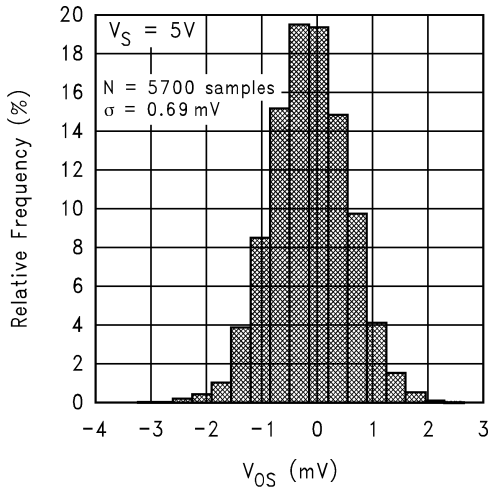
Note 10: Short circuit test is a momentary test. See Note 11.

Note 11: Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

Note 12: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Typical Performance Charateristics

V_{OS} Distribution



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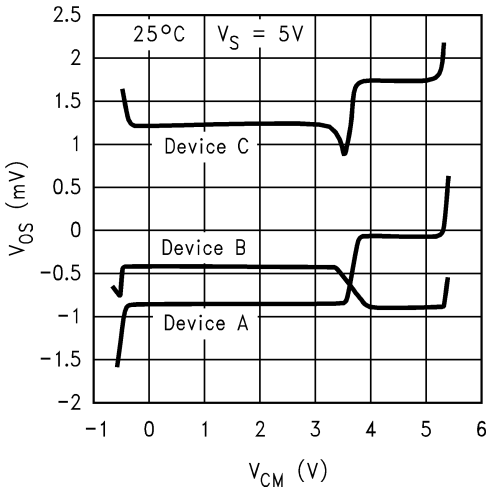
V_{OS} vs. V_{CM} for 3 Representative Units



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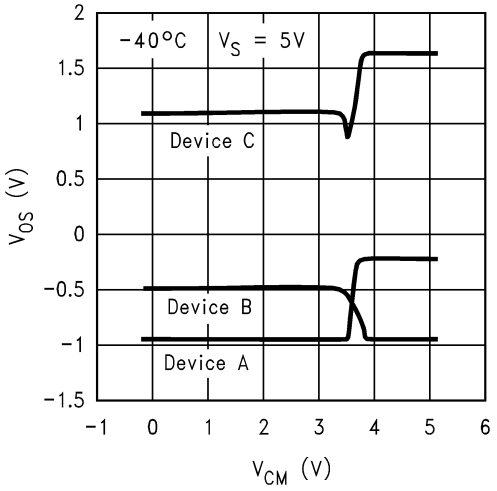
V_{OS} vs. V_{CM} for 3 Representative Units



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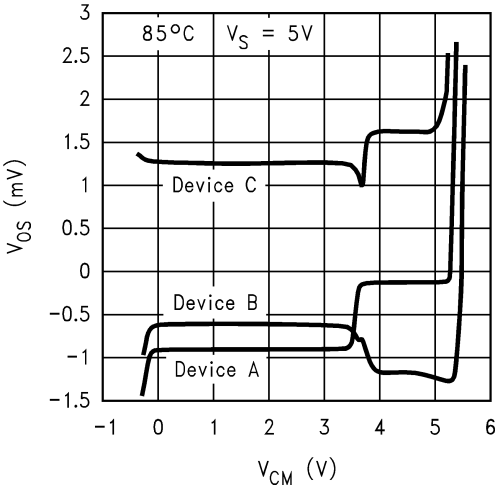
V_{OS} vs. V_{CM} for 3 Representative Units



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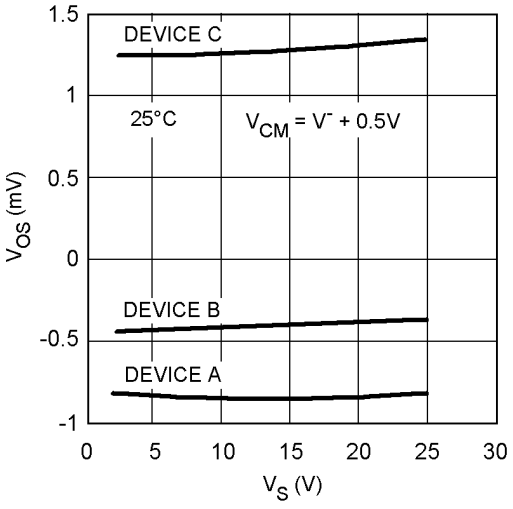
V_{OS} vs. V_S for 3 Representative Units



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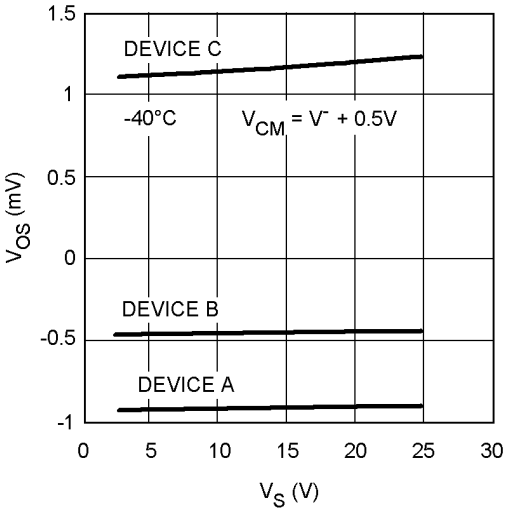
V_{OS} vs. V_S for 3 Representative Units



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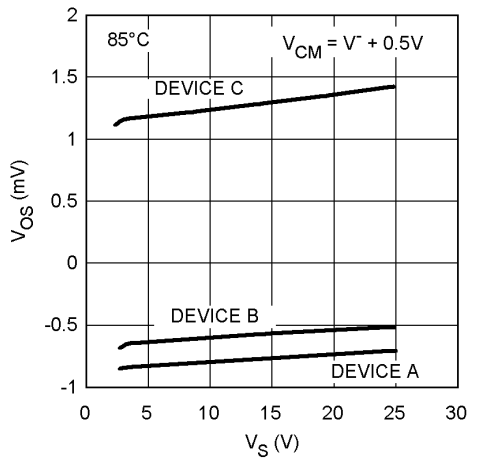
Typical Performance Charateristics (Continued)

V_{OS} vs. V_S for 3 Representative Units



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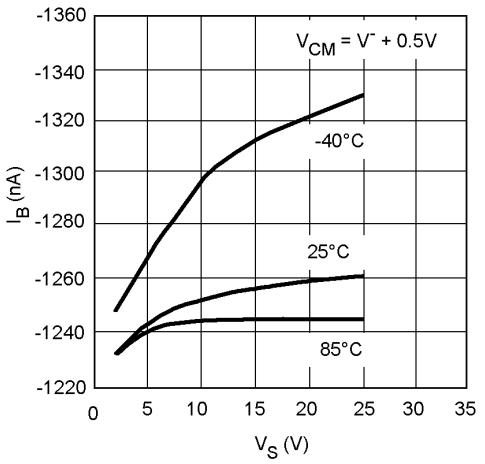
I_B vs. V_S



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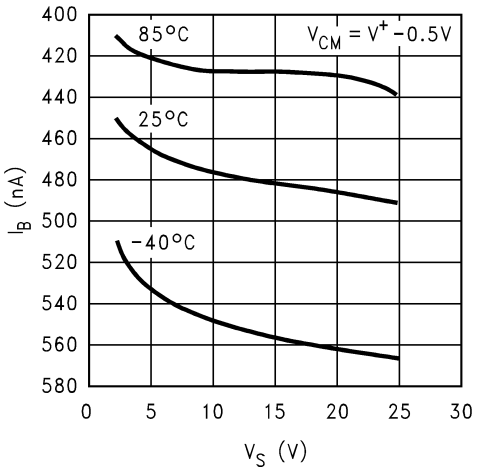
I_B vs. V_S



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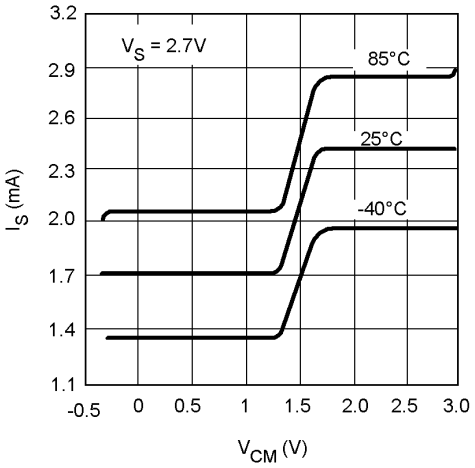
I_S vs. V_{CM}



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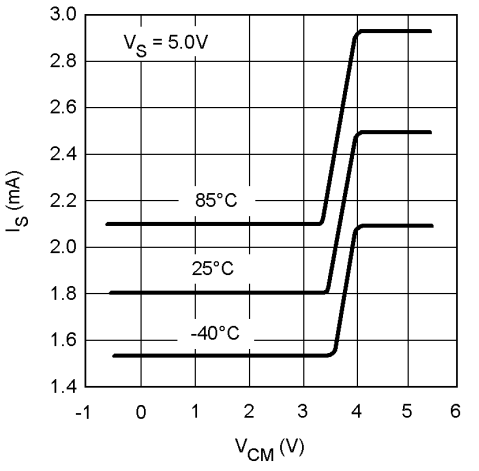
I_S vs. V_{CM}



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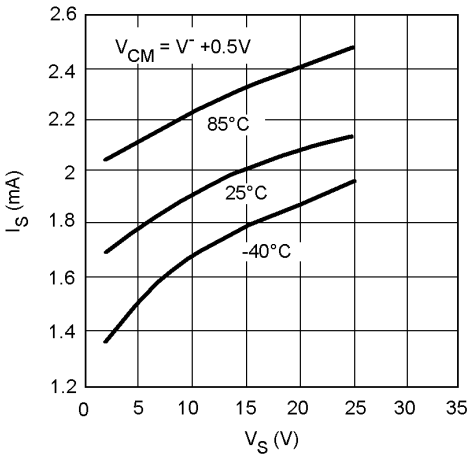
I_S vs. V_S



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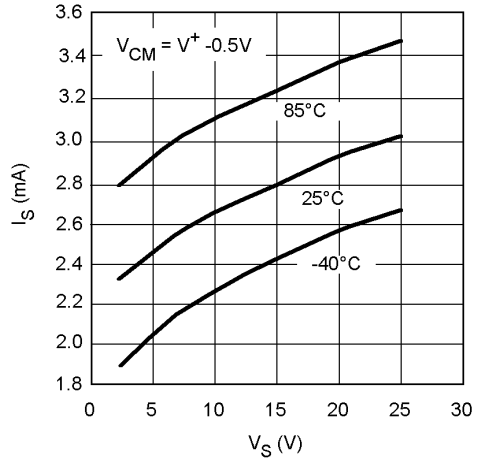
Typical Performance Charateristics (Continued)

I_S vs. V_S



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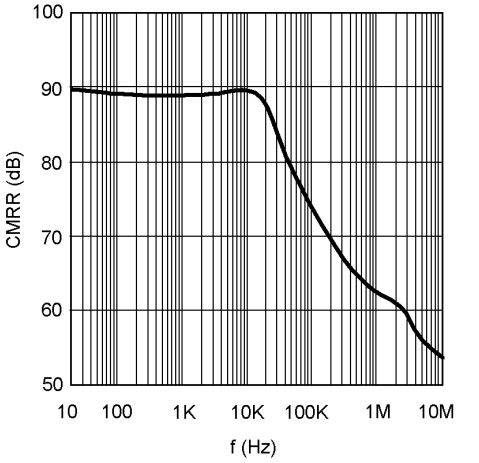
CMRR vs. Frequency



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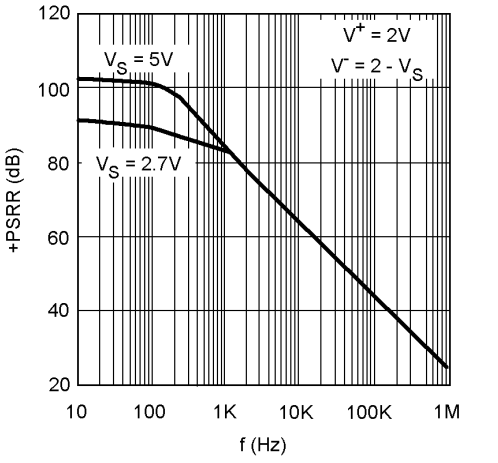
+PSRR vs. Frequency



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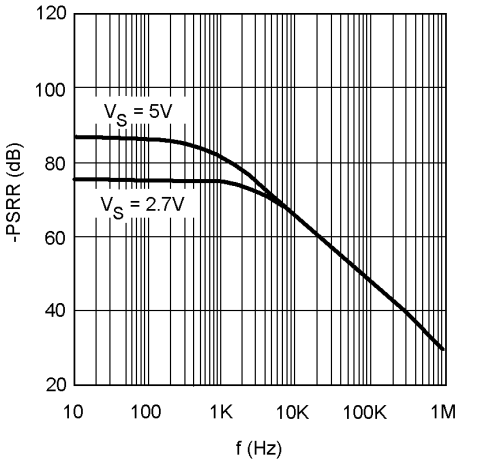
–PSRR vs. Frequency



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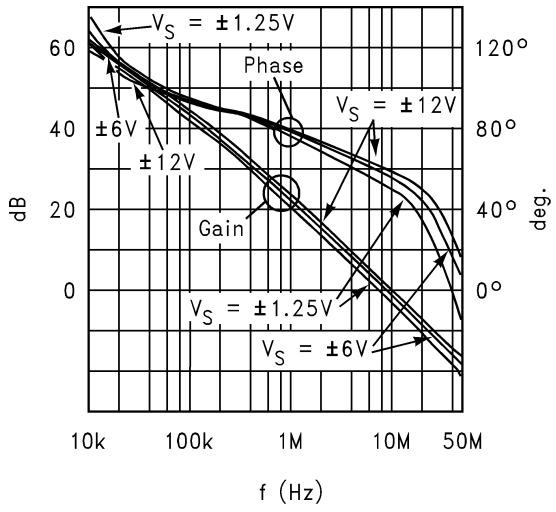
Open Loop Gain/Phase for Various Supplies



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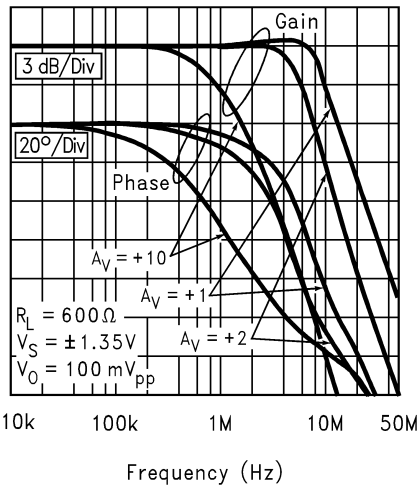
Closed Loop Frequency Response for Various Gains



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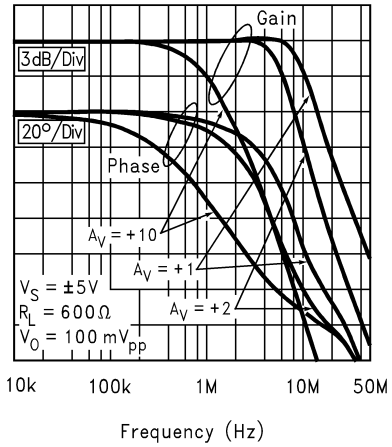
Typical Performance Charateristics (Continued)

Closed Loop Frequency Response for Various Gains



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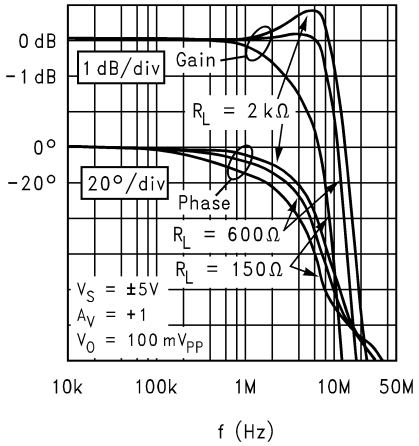
Closed Loop Frequency Response for Various Gains R_L



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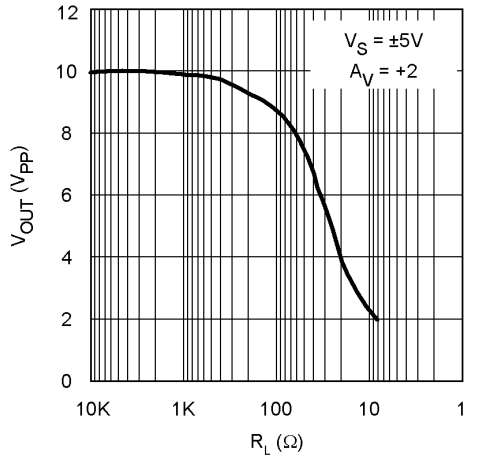
Maximum Output Swing vs. Load (1% Distortion)



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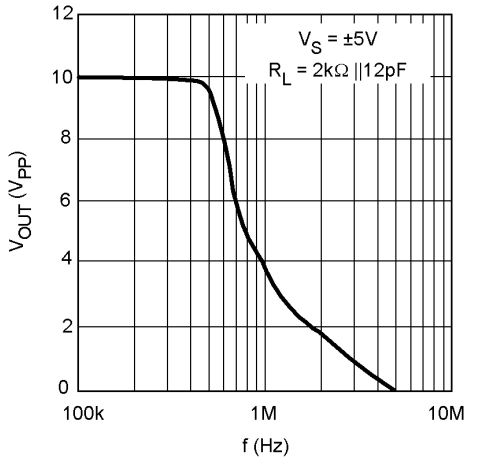
Maximum Output Swing vs. Frequency (1% Distortion)



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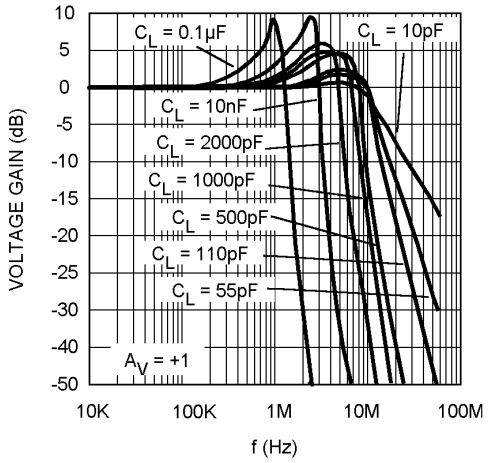
Closed Loop Small Signal Frequency Response for Various C_L



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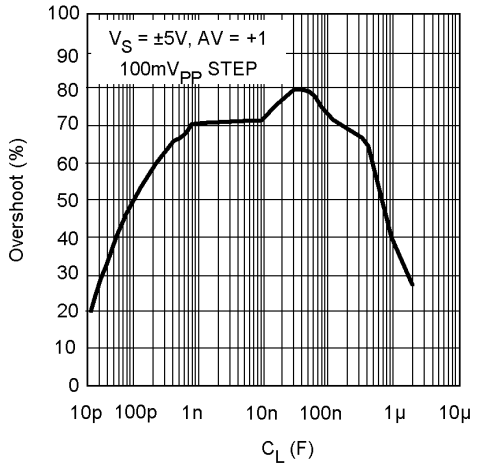
Overshoot vs. Cap Load



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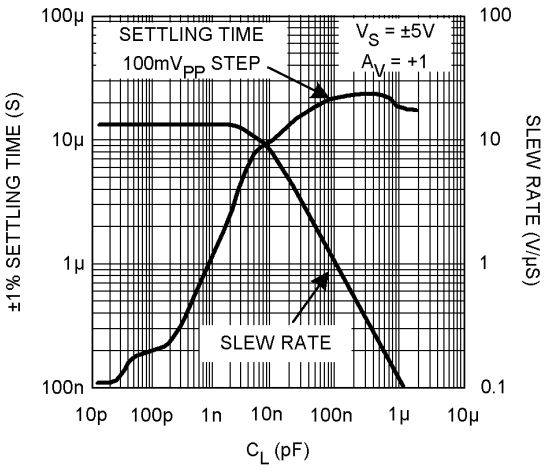
Typical Performance Charateristics (Continued)

Settling Time (±1%) & Slew Rate vs. Cap Load



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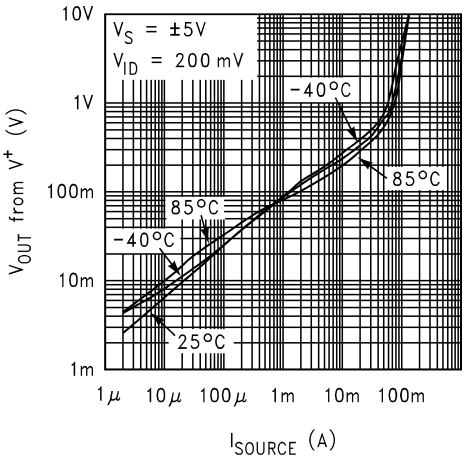
V_{OUT} from V^+ vs. I_{SOURCE}



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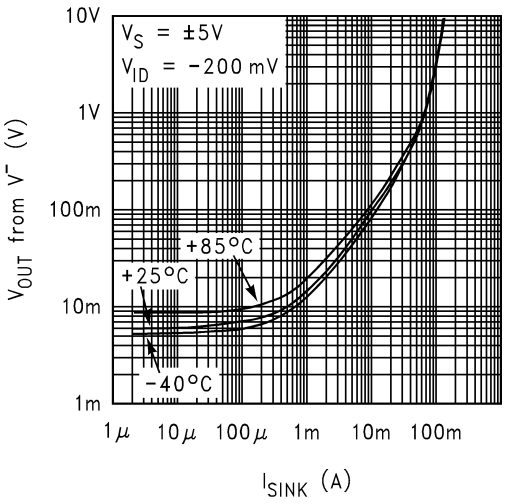
V_{OUT} from V^- vs. I_{SINK}



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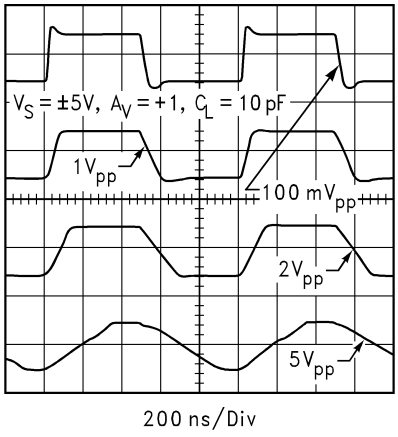
Step Response for Various Amplitudes



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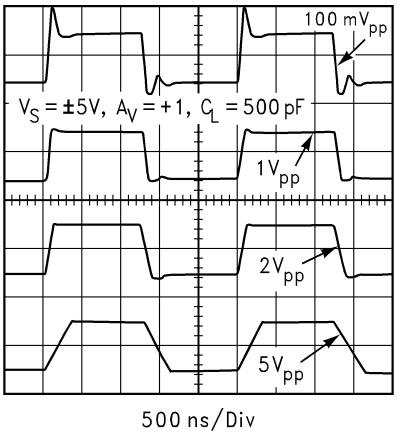
Step Response for Various Amplitudes



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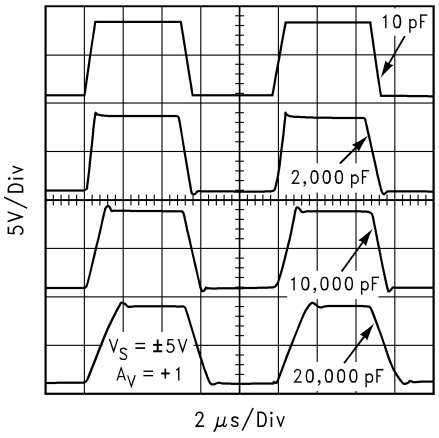
Large Signal Step Response for Various Cap Loads



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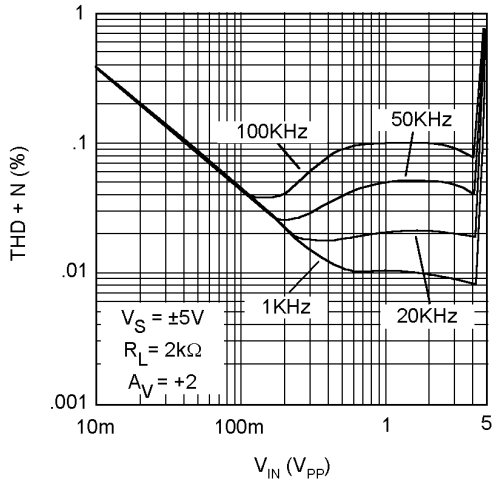
Typical Performance Charateristics (Continued)

THD+N vs. Input Amplitude for Various Frequency



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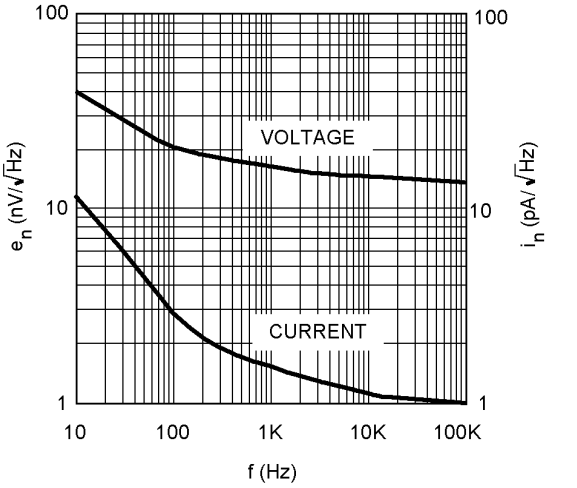
Input Referred Noise Density



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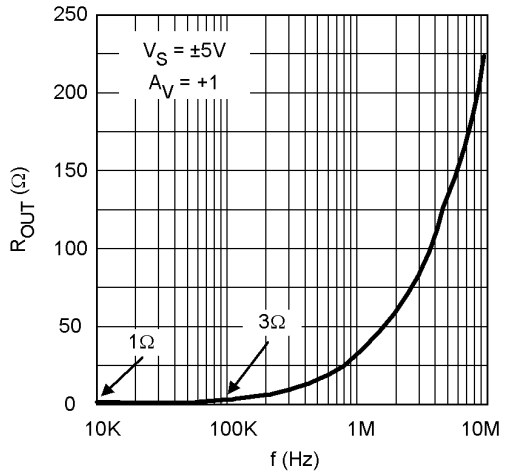
Closed Loop Output Impedance vs. Frequency



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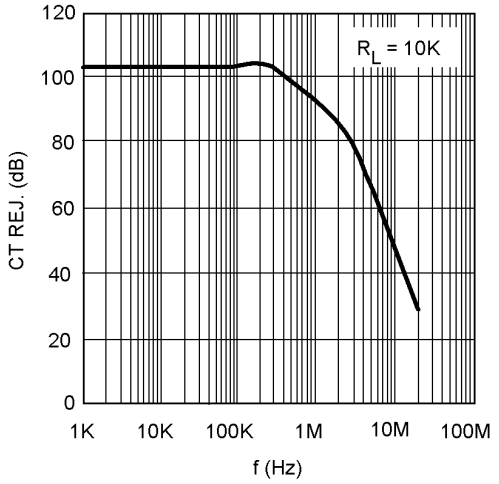
Crosstalk Rejection vs. Frequency



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Application Notes

BLOCK DIAGRAM AND OPEATIONAL DESCRIPTION
A) INPUT STAGE:

As can be seen from the simplified schematic in *Figure 1*, the input stage consists of two distinct differential pairs (Q1-Q2 and Q3-Q4) in order to accommodate the full Rail-to-Rail input common mode voltage range. The voltage drop across R5, R6, R7 and R8 is kept to less than 200mV in order to allow the input to exceed the supply rails. Q13 acts as a switch to steer current away from Q3-Q4 and into Q1-Q2, as the input increases beyond 1.4 of V^+. This in turn shifts the signal path from the bottom stage differential pair to the top one and causes a subsequent increase in the supply current.

In transitioning from one stage to another, certain input stage parameters (V_{OS}, I_b, I_{OS}, e_n, and i_n) are determined based on which differential pair is "on" at the time. Input Bias current, I_b, will change in value and polarity as the input crosses the transition region. In addition, parameter such as PSRR and CMRR which involve the input offset voltage will also be effected by changes in V_{CM} across the differential pair transition region.

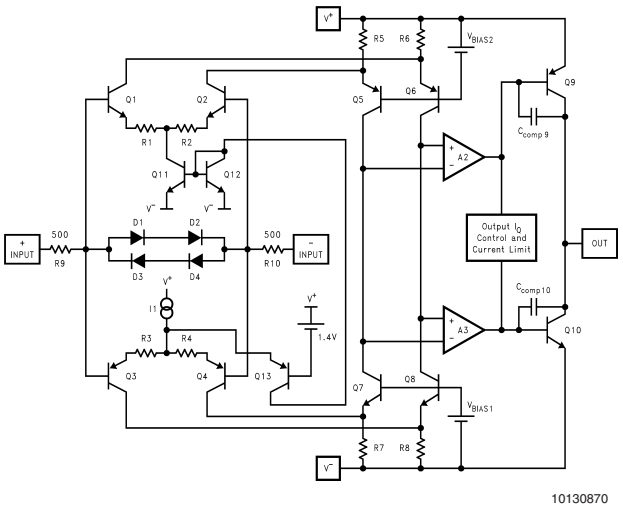


FIGURE 1. Simplified Schematic Diagram

The input stage is protected with the combination of R9-R10 and D1, D2, D3 and D4 against differential input overvoltages. This fault condition could otherwise harm the differential pairs or cause offset voltage shift in case of prolonged over voltage. As shown in *Figure 2*, if this voltage reaches approximately ±1.4V at 25˚C, the diodes turn on and current flow is limited by the internal series resistors (R9 and R10). The Absolute Maximum Rating of ±10V differential on V_{IN} still needs to be observed. With temperature variation, the point were the diodes turn on will change at the rate of 5mV/˚C

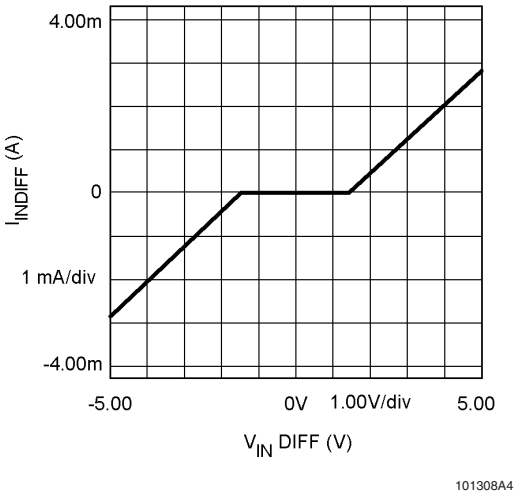


FIGURE 2. Input Stage Current vs. Differential Input Voltage

B) OUTPUT STAGE:

The output stage (see *Figure 1*) is comprised of complimentary NPN and PNP common-emitter stages to permit voltage swing to within a $V_{ce(sat)}$ of either supply rail. Q9 supplies the sourcing and Q10 supplies the sinking current load. Output current limiting is achieved by limiting the V_{ce} of Q9 and Q10; using this approach to current limiting, alleviates the draw back to the conventional scheme which requires one V_{be} reduction in output swing.

The frequency compensation circuit includes Miller capacitors from collector to base of each output transistor (see *Figure 1*, C_{comp9} and C_{comp10}). At light capacitive loads, the high frequency gain of the output transistors is high, and the Miller effect increases the effective value of the capacitors thereby stabilizing the Op Amp. Large capacitive loads greatly decrease the high frequency gain of the output transistors thus lowering the effective internal Miller capacitance - the internal pole frequency increases at the same time a low frequency pole is created at the Op Amp output due to the large load capacitor. In this fashion, the internal dominant pole compensation, which works by reducing the loop gain to less than 0dB when the phase shift around the feedback loop is more than 180˚, varies with the amount of capacitive load and becomes less dominant when the load capacitor has increased enough. Hence the Op Amp is very stable even at high values of load capacitance resulting in the uncharacteristic feature of stability under all capacitive loads.

C) OUTPUT VOLTAGE SWING CLOSE TO V^-:

The LM8272's output stage design allows voltage swings to within millivolts of either supply rail for maximum flexibility and improved useful range. Because of this design architecture, as can be seen from *Figure 1* diagram, with Output approaching either supply rail, either Q9 or Q10 Collector-Base junction reverse bias will decrease. With output less than a V_{be} from either rail, the corresponding output transistor operates near saturation. In this mode of operation, the transistor will exhibit higher junction capacitance and lower f_t which will reduce Phase Margin. With the Noise Gain (NG = 1 + Rf/Rg, Rf & Rg are external gain setting resistors) of 2 or higher, there is sufficient Phase Margin that this reduction (in Phase Margin) is of no consequence. However, with lower

Application Notes (Continued)

Noise Gain (<2) and with less than 150mV voltage to the supply rail, if the output loading is light, the Phase Margin reduction could result in unwanted oscillations.

In the case of the LM8272, due to inherent architectural specifics, the oscillation occurs only with respect to Q10 when output swings to within 150mV of V^-. However, if Q10 collector current is larger than its idle value of a few microamps, the Phase Margin loss becomes insignificant. In this case, 300µA is the required Q10 collector current to remedy this situation. Therefore, when all the aforementioned critical conditions are present at the same time (NG < 2, V_{OUT} < 150mV from supply rails, & output load is light) it is possible to ensure stability by adding a load resistor to the output to provide the necessary Q10 minimum Collector Current (300µA).

For 12V (or ±6V) operation, for example, add a 39kΩ resistor from the output to V^+ to cause 300µA output sinking current and ensure stability. This is equivalent to about 15% increase in total quiescent power dissipation.

DRIVING CAPACTIVE LOADS:

The LM8272 is specifically designed to drive unlimited capacitive loads without oscillations (see Settling Time and Overshoot vs. Cap Load plots in the typical performance characteristics section). In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads (Settling Time and Slew Rate vs. Cap Load plot). The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, etc.

However, as in most Op Amps, addition of a series isolation resistor between the Op Amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to the Settling Time and Slew Rate vs. Cap Load plots (typical performance characteristics section), two distinct regions can be identified. Below about 10,000pF, the output Slew Rate is solely determined by the Op Amp's compensation capacitor value and available current into that capacitor. Beyond 10nF, the Slew Rate is determined by the Op Amp's available output current. An estimate of positive and negative slew rates for loads larger than 100nF can be made by dividing the short circuit current value by the capacitor.

ESTIMATING THE OUTPUT VOLTAGE SWING

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, *Figure 3* and *Figure 4* plots can be used to predict the output swing. These plots also show several load lines corresponding to loads tied between the output and ground. In each case, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 600Ω load can accommodate an output swing to within 100mV of V^- and to 250mV of V^+ (V_S = ±5V) corresponding to a typical 9.65V_{PP} unclipped swing.

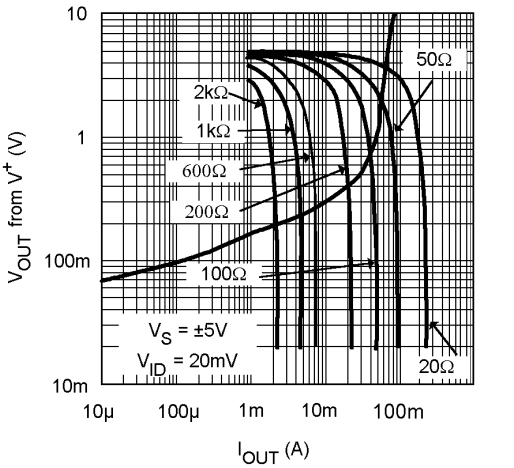


FIGURE 3. Steady State Output Sourcing Characteristics with Load Lines

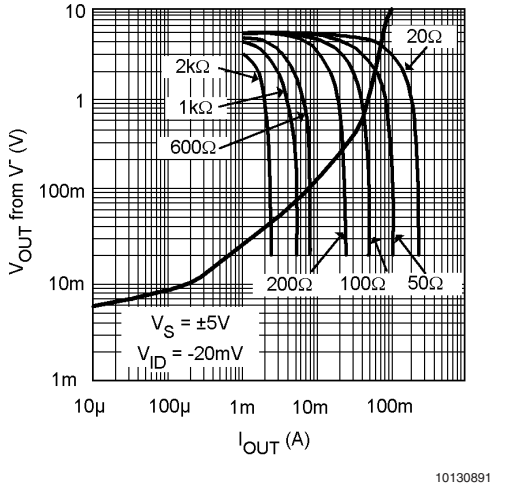


FIGURE 4. Steady State Output Sinking Characteristics with Load Lines

Application Notes (Continued)

OUTPUT SHORT CIRCUIT CURRENT AND DISSIPATION ISSUES:

The LM8272 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, output short circuit condition can be tolerated indefinitely.

With the Op Amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the Op Amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$P_{total} = P_Q + P_{DC} + P_{AC}$

$P_Q = I_S \cdot V_S$ Op Amp Quiescent Power Dissipation

$P_{DC} = I_O \cdot (V_r - V_o)$ DC Load Power

P_{AC} = See Table 1 below AC Load Power

where:

I_S: Supply Current

V_S: Total Supply Voltage ($V^+ - V^-$)

V_O: Average Output Voltage

V_r: V^+ for sourcing and V^- for sinking current

Table 1 below shows the maximum AC component of the load power dissipated by the Op Amp for standard Sinusoidal, Triangular, and Square Waveforms:

TABLE 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V²)		
Sinusoidal	Triangular	Square
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot [24^2/600] = 45.0\text{mW}$$

OTHER APPLICATION HINTS:

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge "bucket" for fast load current spikes at the Op Amp output. The combination of these capacitors will provide supply decoupling and will help keep the Op Amp oscillation free under any load.

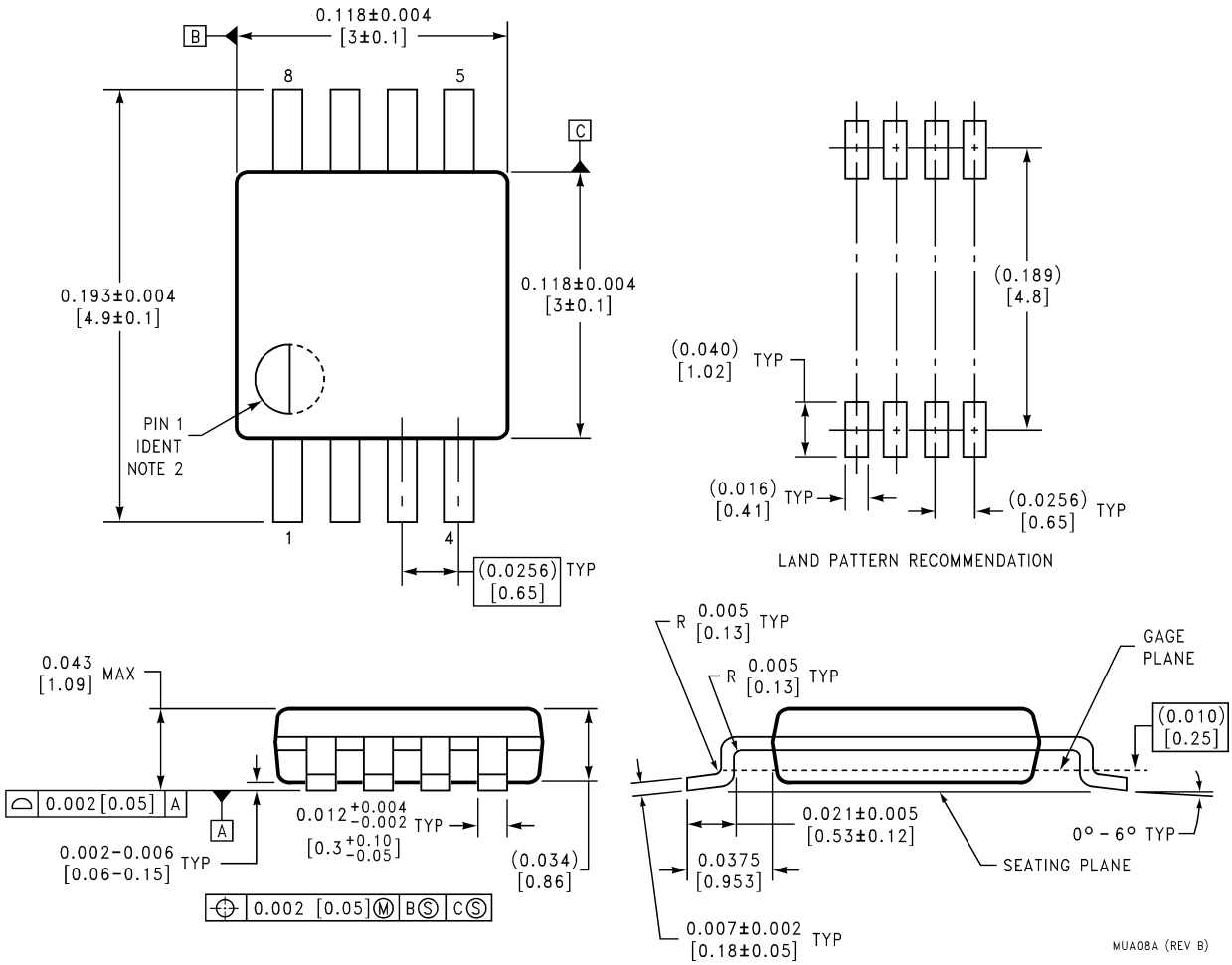
LM8272 ADVANTAGES:

Compared to other Rail-to-Rail Input/Output devices, the LM8272 offers several advantages such as:

- Improved cross over distortion
- Nearly constant supply current throughout the output voltage swing range and close to either rail.
- Nearly constant Unity gain frequency (f_u) and Phase Margin (Phi_m) for all operating supplies and load conditions.
- No output phase reversal under input overload condition.

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin MSOP
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