Data Sheet | September 25, 2007 | FN6557.0

MP3/USB 2.0 High Speed Switch with Negative Signal Handling

The Intersil ISL54205B dual SPDT (Single Pole/Double Throw) switches combine low distortion audio and accurate USB 2.0 high speed data (480Mbps) signal switching in the same low voltage device. When operated with a 2.7V to 3.6V single supply these analog switches allow audio signal swings below-ground, allowing the use of a common USB and audio headphone connector in Personal Media Players and other portable battery powered devices.

The ISL54205B incorporates circuitry for detection of the USB V_{BUS} voltage, which is used to switch between the audio and USB signal sources in the portable device. The part has a control pin to open all the switches and put the part in a low power down state.

The ISL54205B is available in a small 10 Ld 2.1mmx1.6mm ultra-thin µTQFN package and a 10Ld 3mmx3mm TDFN package. It operates over a temperature range of -40 to +85°C.

Related Literature

- Application Note AN1280 “ISL54205EVAL1Z Evaluation Board User’s Manual.
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

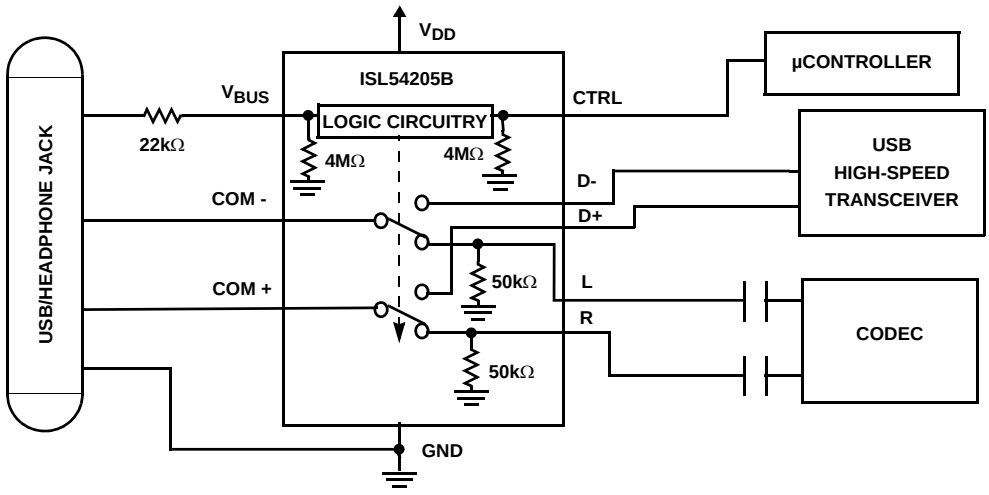
Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Low Distortion Negative Signal Capability
- Detection of V_{BUS} Voltage on USB Cable
- Control Pin to Open all Switches and Enter Low Power State
- Low Distortion Headphone Audio Signals
  - THD+N at 20mW into 32Ω Load . . . . . <0.1%
- Cross-talk (20Hz to 20kHz) . . . . . -110dB
- Single Supply Operation (V_{DD}) . . . . . 2.7V to 3.6V
- -3dB Bandwidth USB Switch 630MHz
- Available in µTQFN and TDFN Packages
- Pb-Free (RoHS Compliant)
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components

Applications

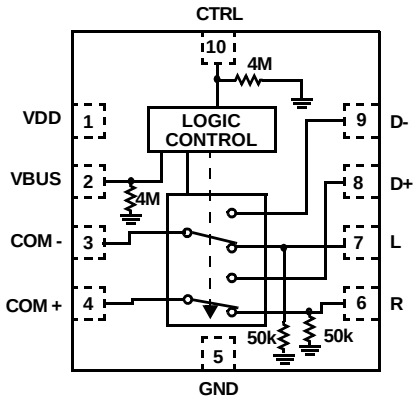
- MP3 and Other Personal Media Players
- Cellular/Mobile Phones
- PDA’s
- Audio/USB Switching

Application Block Diagram

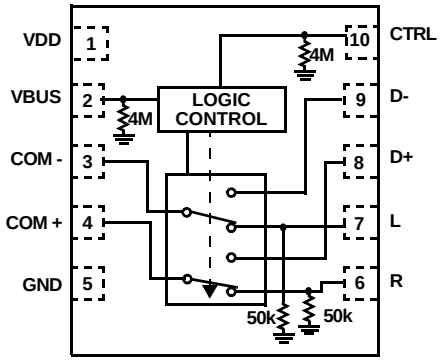


Pinouts (Note 1)

ISL54205B
(10 LD μTQFN)
TOP VIEW



ISL54205B
(10 LD TDFN)
TOP VIEW



NOTE:

1. ISL54205B Switches shown for V_{BUS} = Logic “0” and CTRL = Logic “1”.

Truth Table

ISL54205B			
V_{BUS}	CTRL	L, R	D+, D-
0	0	OFF	OFF
0	1	ON	OFF
1	X	OFF	ON

CTRL: Logic “0” when ≤ 0.5V or Float, Logic “1” when ≥ 1.4V
V_{BUS}: Logic “0” when ≤ V_{DD} + 0.2V or Float, Logic “1” when ≥V_{DD} + 0.8V

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54205BIRUZ-T* (Note 2)	FW	-40 to +85	10 Ld μTQFN Tape and Reel	L10.2.1x1.6A
ISL54205BIRTZ-T* (Note 3)	205B	-40 to +85	10 Ld TDFN Tape and Reel	L10.3x3A
ISL54205BIRTZ (Note 3)	205B	-40 to +85	10 Ld TDFN	L10.3x3A
ISL54205EVAL1Z	Evaluation Board			

*Please refer to TB347 for details on reel specifications.

NOTES:

2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN NUMBER	NAME	FUNCTION
1	VDD	Power Supply
2	VBUS	Digital Control Input
3	COM-	Voice and Data Common Pin
4	COM+	Voice and Data Common Pin
5	GND	Ground Connection
6	R	Audio Right Input
7	L	Audio Left Input
8	D+	USB Differential Input
9	D-	USB Differential Input
10	CTRL	Digital Control Input (Audio Enable)

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3 to 6.0V
Input Voltages
D+, D-, L, R (Note 4) . . . . . - 2V to ((V_{DD}) + 0.3V)
V_{BUS} (Note 4) . . . . . -2V to 5.5V
CTRL (Note 4) . . . . . -0.3 to ((V_{DD}) + 0.3V)
Output Voltages
COM-, COM+ (Note 4) . . . . . -2V to ((V_{DD}) + 0.3V)
Continuous Current (Audio Switches) . . . . . ±150mA
Peak Current (Audio Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±300mA
Continuous Current (USB Switches) . . . . . ±40mA
Peak Current (USB Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
HBM . . . . . >7kV
MM . . . . . >450V
CDM . . . . . >2kV

Thermal Information

Thermal Resistance (Typical, Notes 5, 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld µTQFN Package	130	48.3
10 Ld 3x3 TDFN Package	110	20

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

4. Signals on D+, D-, L, R, COM-, COM+, CTRL, V_{BUS} exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{BUSH} = 3.8V, V_{BUSL} = 3.2V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Notes 7, 8), unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
AUDIO SWITCHES (L, R)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.0V, V_{BUS} = float, CTRL = 1.4V	Full	-1.5	-	1.5	V
ON-Resistance, r_{ON}	V_{DD} = 3.0V, V_{BUS} = float, CTRL = 1.4V, I_{COMx} = 100mA, V_L or V_R = -0.85V to 0.85V (See Figure 3)	+25	-	2.65	4	Ω
		Full	-	-	5.5	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.0V, V_{BUS} = float, CTRL = 1.4V, I_{COMx} = 100mA, V_L or V_R = Voltage at max r_{ON} over signal range of -0.85V to 0.85V (Note 11)	+25	-	0.02	0.13	Ω
		Full	-	-	0.16	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.0V, V_{BUS} = float, CTRL = 1.4V, I_{COMx} = 100mA, V_L or V_R = -0.85V to 0.85V (Note 10)	+25	-	0.03	0.05	Ω
		Full	-	-	0.07	Ω
Discharge Pull-Down Resistance, R_L, R_R	V_{DD} = 3.6V, V_{BUS} = float, CTRL = 1.4V, V_{COM-} or V_{COM+} = -0.85V, 0.85V, V_L or V_R = -0.85V, 0.85V, V_{D+} and V_{D-} = floating, Measure current through the discharge pull-down resistor and calculate resistance value.	+25	-	50	-	kΩ
USB SWITCHES (D+, D-)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V	Full	0	-	V_{DD}	V
ON-Resistance, r_{ON}	V_{DD} = 3.3V, V_{BUS} = 4.4V, CTRL = 3.3V, I_{COMx} = 1mA, V_{D+} or V_{D-} = 3.3V (See Figure 4)	+25	-	23.5	30	Ω
		Full	-	-	35	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.6V, V_{BUS} = 4.4V, CTRL = 0V or 3.6V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV (See Figure 4)	+25	-	4.6	5	Ω
		Full	-	-	6.5	Ω

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{BUSH} = 3.8V, V_{BUSL} = 3.2V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Notes 7, 8), unless otherwise specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.6V, V_{BUS} = 4.4V, CTRL = 0V or 3.6V, I_{COMx} = 40mA, V_{D+} or V_{D-} = Voltage at max r_{ON}, (Note 11)	+25	-	0.06	0.5	Ω
		Full	-	-	0.55	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 3.6V, V_{BUS} = 4.4V, CTRL = 0V or 3.6V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV, (Note 10)	+25	-	0.4	0.6	Ω
		Full	-	-	1.0	Ω
OFF Leakage Current, $I_{D+(OFF)}$ or $I_{D-(OFF)}$	V_{DD} = 3.6V, V_{BUS} = 0V, CTRL = 3.6V, V_{COM-} or V_{COM+} = 0.5V, 0V, V_{D+} or V_{D-} = 0V, 0.5V, V_L and V_R = float	+25	-10	-	10	nA
		Full	-70	-	70	nA
ON Leakage Current, I_{Dx}	V_{DD} = 3.3V, V_{BUS} = 5.25V, CTRL = 0V or 3.6V, V_{D+} or V_{D-} = 2.0V, V_{COM-}, V_{COM+}, V_L and V_R = float	+25	-10	2	10	nA
		Full	-75	-	75	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF (See Figure 1)	+25	-	67	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF (See Figure 1)	+25	-	48	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF (See Figure 2)	+25	-	18	-	ns
Skew, t_{SKEW}	V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 720ps at 480Mbps, (Duty Cycle = 50%) (See Figure 7)	+25	-	50	-	ps
Total Jitter, t_J	V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, R_L = 50Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps	+25	-	210	-	ps
Propagation Delay, t_{PD}	V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, R_L = 45Ω, C_L = 10pF (See Figure 7)	+25	-	250	-	ps
Crosstalk (Channel-to-Channel), R to COM-, L to COM+	V_{DD} = 3.0V, V_{BUS} = float, CTRL = 3.0V, R_L = 32Ω, f = 20Hz to 20kHz, V_R or V_L = 0.707V_{RMS} ($2V_{P-P}$) (See Figure 6)	+25	-	-110	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, V_{BUS} = float, CTRL = 3.0V, V_L or V_R = 0.707V_{RMS} ($2V_{P-P}$), R_L = 32Ω	+25	-	0.06	-	%
USB Switch -3dB Bandwidth	Signal = 0dBm, 0.2V_{DC} offset, R_L = 50Ω, C_L = 5pF	+25	-	630	-	MHz
D+/D- OFF Capacitance, $C_{D+(OFF)}$, $C_{D-(OFF)}$	f = 1MHz, V_{DD} = 3.0V, V_{BUS} = float, CTRL = 3.0V, V_{D-} or V_{D+} = V_{COMx} = 0V (See Figure 5)	+25	-	6	-	pF
L/R OFF Capacitance, C_{LOFF}, C_{ROFF}	f = 1MHz, V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, V_L or V_R = V_{COMx} = 0V (See Figure 5)	+25	-	9	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 1MHz, V_{DD} = 3.0V, V_{BUS} = 5.0V, CTRL = 0V or 3V, V_{D-} or V_{D+} = V_{COMx} = 0V, (See Figure 5)	+25	-	10	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	2.7	-	3.6	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, V_{BUS} = float or 5.25V, CTRL = 1.4V	+25	-	6	8	µA
		Full	-	-	10	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 3.6V, V_{BUS} = 0V or float, CTRL = 0V or float	+25	-	1	7	nA
		Full	-	-	140	nA
DIGITAL INPUT CHARACTERISTICS						
V_{BUS} Voltage Low, V_{BUSL}	V_{DD} = 2.7V to 3.6V	Full	-	-	V_{DD} + 0.2	V
V_{BUS} Voltage High, V_{BUSH}	V_{DD} = 2.7V to 3.6V	Full	V_{DD} + 0.8	-	-	V
CTRL Voltage Low, V_{CTRLL}	V_{DD} = 2.7V to 3.6V	Full	-	-	0.5	V

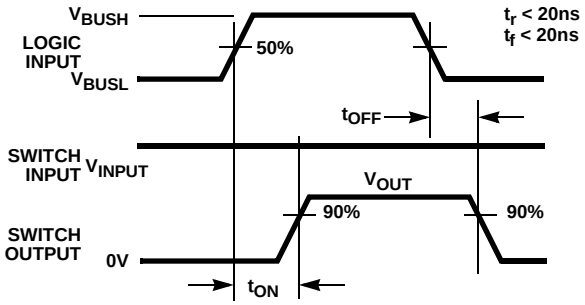
Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{BUSH} = 3.8V, V_{BUSL} = 3.2V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Notes 7, 8), unless otherwise specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
CTRL Voltage High, V_{CTRLH}	V_{DD} = 2.7V to 3.6V	Full	1.4	-	-	V
Input Current, I_{BUSL}, I_{CTRLL}	V_{DD} = 3.6V, V_{BUS} = 0V or float, CTRL = 0V or float	Full	-50	20	50	nA
Input Current, I_{BUSH}	V_{DD} = 3.6V, V_{BUS} = 5.25V, CTRL = 0V or float	Full	-2	1.1	2	µA
Input Current, I_{CTRLH}	V_{DD} = 3.6V, V_{BUS} = 0V or float, CTRL = 3.6V	Full	-2	1.1	-2	µA
V_{BUS} Pull-Down Resistor, R_{VBUS}	V_{DD} = 3.6V, V_{BUS} = 5.25V, CTRL = 0V or float	Full	-	4	-	MΩ
CTRL Pull-Down Resistor, R_{CTRL}	V_{DD} = 3.6V, V_{BUS} = 0V or float, CTRL = 3.6V	Full	-	4	-	MΩ

NOTES:

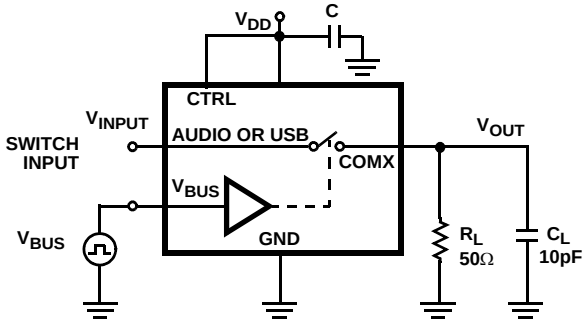
7. V_{LOGIC} = Input voltage to perform proper function.
8. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
9. Parts are 100% tested at +25°C**.** Over-temperature limits established by characterization and are not production tested.
10. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
11. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between L and R or between D+ and D-.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

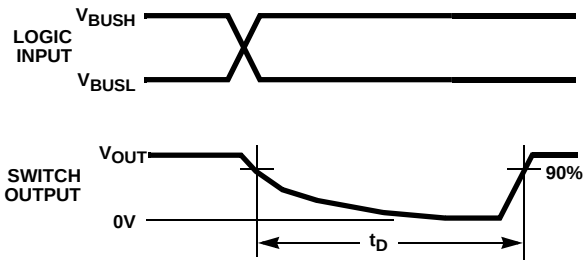
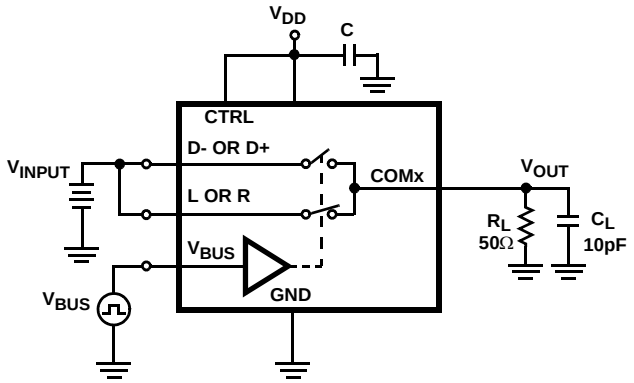


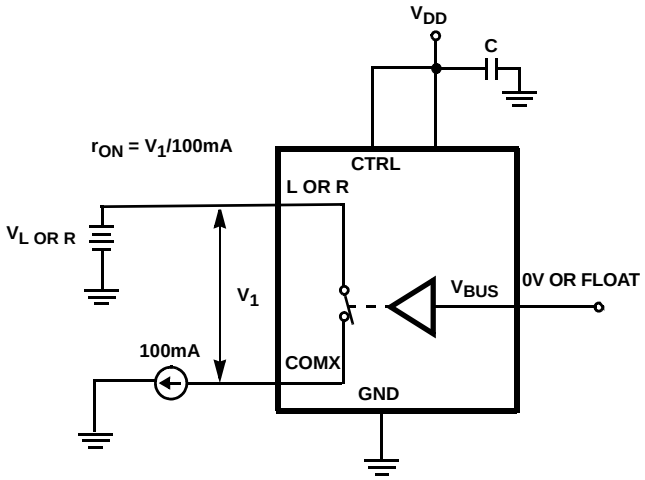
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

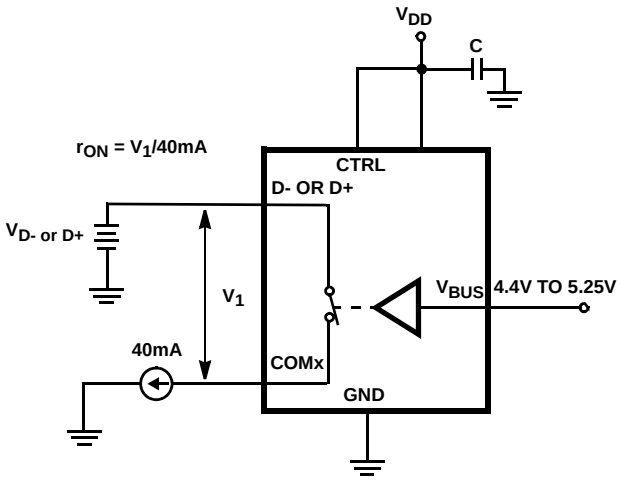
FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

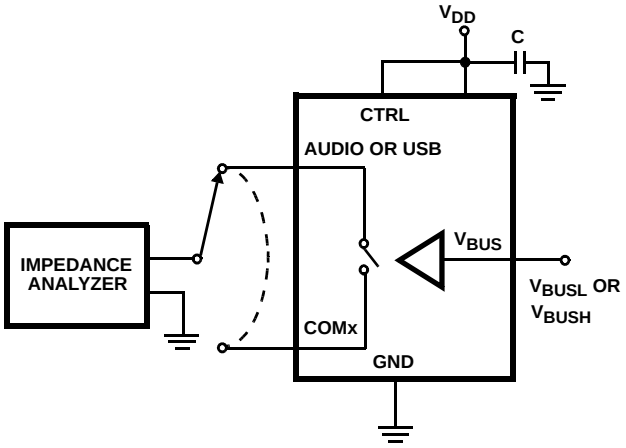
FIGURE 3. AUDIO r_{ON} TEST CIRCUIT



Repeat test for all switches.

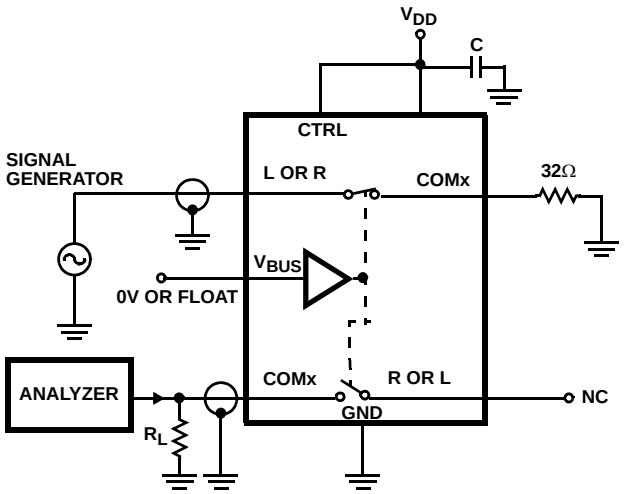
FIGURE 4. USB r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 5. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. AUDIO CROSSTALK TEST CIRCUIT

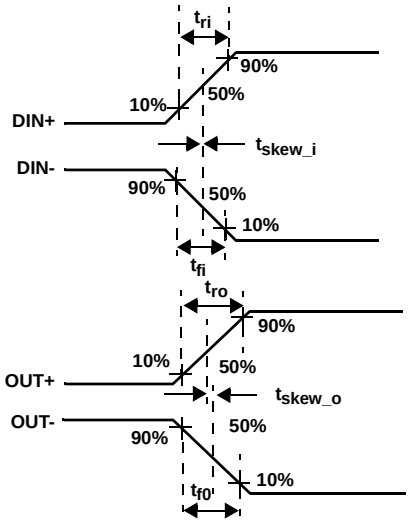
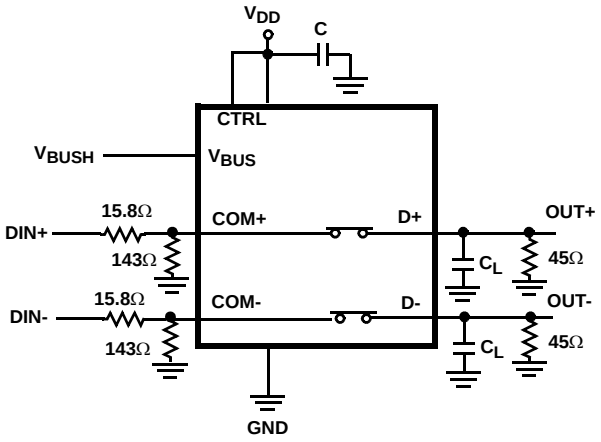


FIGURE 7A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

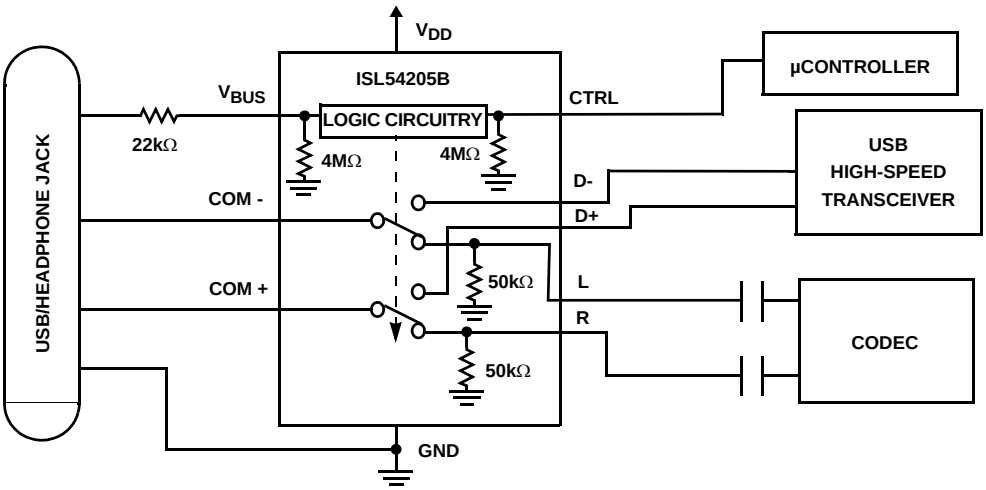
|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 7B. TEST CIRCUIT

FIGURE 7. SKEW TEST

Application Block Diagram



Detailed Description

The ISL54205B device is a dual single pole/double throw (SPDT) analog switch device that operates from a single DC power supply in the range of 2.7V to 3.6V. It was designed to function as a dual 2 to 1 multiplexer to select between USB differential data signals and audio L and R stereo signals. It comes in tiny µTQFN and TDFN packages for use in MP3 players, PDAs, cell phones, and other personal media players.

The part consists of two 3Ω audio switches and two 5Ω USB switches. The audio switches can accept signals that swing below ground. They were designed to pass audio left and right stereo signals, that are ground referenced, with minimal distortion. The USB switches were designed to pass high-speed USB differential data signals with minimal edge and phase distortion.

The ISL54205B was specifically designed for MP3 players, cell phones and other personal media player applications that need to combine the audio headphone jack and the USB data connector into a single shared connector, thereby saving space and component cost. See "Application Block Diagram" on page 9.

The ISL54205B incorporates circuitry for the detection of the USB V_{BUS} voltage, which is used to switch between the audio CODEC drivers and USB transceiver of the MP3 player or cell phone. The ISL54205B contains a logic control pin (CTRL) that when driven low while V_{BUS} is low, opens all switches and puts the part into a low power state, drawing typically 1nA of I_{DD} current.

A detailed description of the two types of switches is provided in the following sections. The USB transmission and audio playback are intended to be mutually exclusive operations.

Audio Switches

The two audio switches (L, R) are 3Ω switches that can pass signals that swing below ground. Crosstalk between the audio switches over the audio band is <-110dB.

Over a signal range of ±1V ($0.707V_{RMS}$) with V_{DD} >2.7V, these switches have an extremely low r_{ON} resistance variation. They can pass ground referenced audio signals with very low distortion (<0.06% THD+N) when delivering 15.6mW into a 32Ω headphone speaker load. See Figures 8, 9, 10, and 11 THD+N in the "Typical Performance Curves on page 11.

These switches are uni-directional switches. The audio drivers should be connected at the L and R side of the switch (pins 7 and 8) and the speaker loads should be connected at the COM side of the switch (pins 3 and 4).

The audio switches are active (turned ON) whenever the V_{BUS} voltage is ≤ to V_{DD} + 0.2V or floating and the CTRL voltage ≥ to 1.4V.

Note: Whenever the audio switches are ON the USB transceivers need to be in the high impedance state.

USB Switches

The two USB switches (D+, D-) are bidirectional switches that can pass rail-to-rail signals. When powered with a 3.6V supply these switches have a nominal $r_{(ON)}$ of 4.6Ω over the signal range of 0V to 400mV with a $r_{(ON)}$ flatness of 0.4Ω. The $r_{(ON)}$ matching between the D+ and D- switches over this signal range is only 0.06Ω ensuring minimal impact by the switches to USB high speed signal transitions. As the signal level increases the $r_{(ON)}$ resistance increases. At signal level of 3.3V the switch resistance is nominally 23Ω.

The USB switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with

minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications. See high-speed eye diagram in the “Typical Performance Curves” on page 12, Figure 12.

The USB switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See full-speed eye diagram in the “Typical Performance Curves” on page 13, Figure 13.

The maximum signal range for the USB switches is from -1.5V to V_{DD}. The signal voltage at D- and D+ should not be allowed to exceed the V_{DD} voltage rail or go below ground by more than -1.5V.

The USB switches are active (turned ON) whenever the V_{BUS} voltage is ≥ to V_{DD} + 0.8V. V_{BUS} is internally pulled low, so when V_{BUS} is floating, the USB switches are OFF.

Note: Whenever the USB switches are ON the audio drivers of the CODEC need to be at AC or DC ground or floating to keep from interfering with the data transmission.

ISL54205B Operation

The discussion that follows will discuss using the ISL54205B in the “Application Block Diagram” on page 9.

LOGIC CONTROL

The state of the ISL54205B device is determined by the voltage at the VBUS pin (pin 2) and the CTRL pin (pin 10). Refer to “Truth Table” on page 2.

The VBUS pin and CTRL pin are internally pulled low through 4MΩ resistors to ground and can be left floating. The CTRL control pin is only active when V_{BUS} is logic “0”.

Logic Control Voltage Levels:

V_{BUS} = Logic “0” (Low) when $V_{BUS} \leq V_{DD}$ + 0.2V or Floating.
V_{BUS} = Logic “1” (High) when $V_{BUS} \geq V_{DD}$ + 0.8V
CTRL = Logic “0” (Low) when ≤ 0.5V or floating.
CTRL = Logic “1” (High) when ≥ 1.4V

Audio Mode

If the VBUS pin = Logic “0” and CTRL pin = Logic “1,” the part will be in the Audio mode. In Audio mode the L (left) and R (right) 3Ω audio switches are ON and the D- and D+ 5Ω switches are OFF (high impedance). In a typical application, V_{DD} will be in the range of 2.7V to 3.6V and will be connected to the battery or LDO of the MP3 player or cell phone. When a headphone is plugged into the common connector, nothing gets connected at the VBUS pin (it is floating) and as long as the CTRL = Logic “1,” the ISL54205B part remains in the audio mode and the audio drivers of the player can drive the headphones and play music.

USB Mode

If the VBUS pin = Logic “1” and CTRL pin = Logic “0” or Logic “1,” the part will go into USB mode. In USB mode, the D- and D+ 5Ω switches are ON and the L and R 3Ω audio switches are OFF (high impedance). When a USB cable from a computer or USB hub is connected at the common connector, the voltage at the VBUS pin will be driven to be in the range of 4.4V to 5.25V. The ISL54205B part will go into the USB mode. In USB mode, the computer or USB hub transceiver and the MP3 player or cell phone USB transceiver are connected and digital data will be able to be transmitted back and forth.

When the USB cable is disconnected, the ISL54205B automatically turns the D+ and D- switches OFF.

Low Power Mode

If the VBUS pin = Logic “0” and CTRL pin = Logic “0,” the part will be in the Low Power mode. In the Low Power mode, the audio switches and the USB switches are OFF (high impedance). In this state, the device draws typically 1nA of current.

EXTERNAL VBUS SERIES RESISTOR

The ISL54205B contains a clamp circuit between VBUS and VDD. Whenever the VBUS voltage is greater than the VDD voltage by more than 2.55V, current will flow through this clamp circuitry into the V_{DD} power supply bus.

During normal USB operation, V_{DD} is in the range of 2.7V to 3.6V and V_{BUS} is in the range of 4.4V to 5.25V. The clamp circuit is not active and no current will flow through the clamp into the V_{DD} supply.

In a USB application, the situation can exist where the V_{BUS} voltage from the computer could be applied at the VBUS pin before the V_{DD} voltage is up to its normal operating voltage range and current will flow through the clamp into the V_{DD} power supply bus. This current could be quite high when V_{DD} is OFF or at 0V and could potentially damage other components connected in the circuit. In the application circuit, a 22kΩ resistor has been put in series with the VBUS pin to limit the current to a safe level during this situation.

It is recommended that a current limiting resistor in the range of 10kΩ to 50kΩ be connected in series with the VBUS pin. It will have minimal impact on the logic level at the VBUS pin during normal USB operation and protect the circuit during the time VBUS is present before VDD is up to its normal operating voltage.

Note: No external resistor is required in applications where V_{BUS} will not exceed V_{DD} by more than 2.55V.

POWER

The power supply connected at VDD (pin 1) provides power to the ISL54205B part. Its voltage should be kept in the range of 2.7V to 3.6V when used in a USB/Audio application to ensure you get proper switching when the V_{BUS} voltage is at its lower limit of 4.4V.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

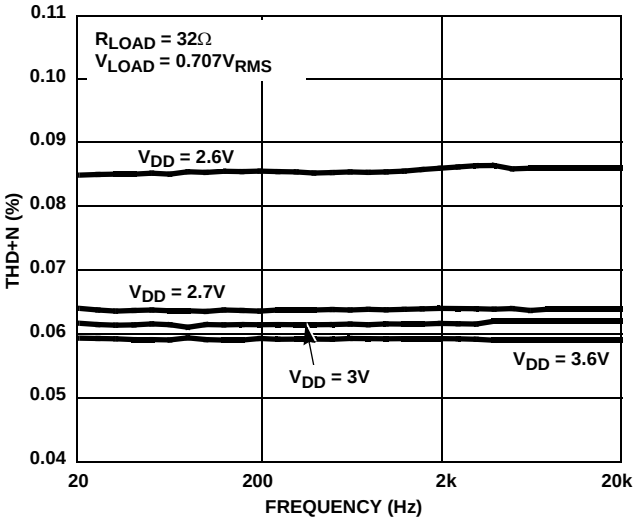


FIGURE 8. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

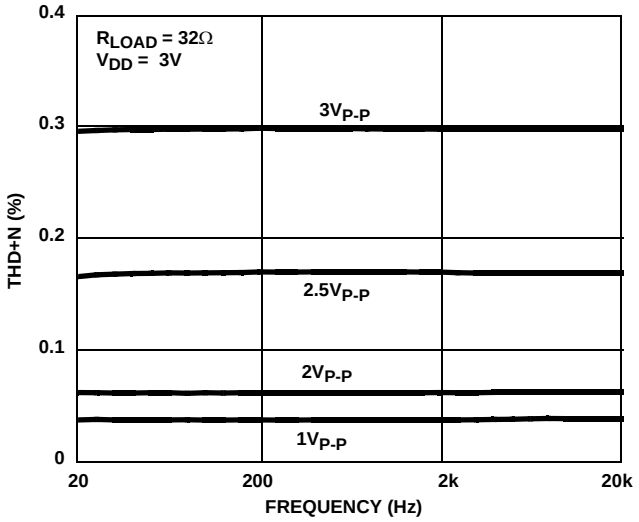


FIGURE 9. THD+N vs SIGNAL LEVELS vs FREQUENCY

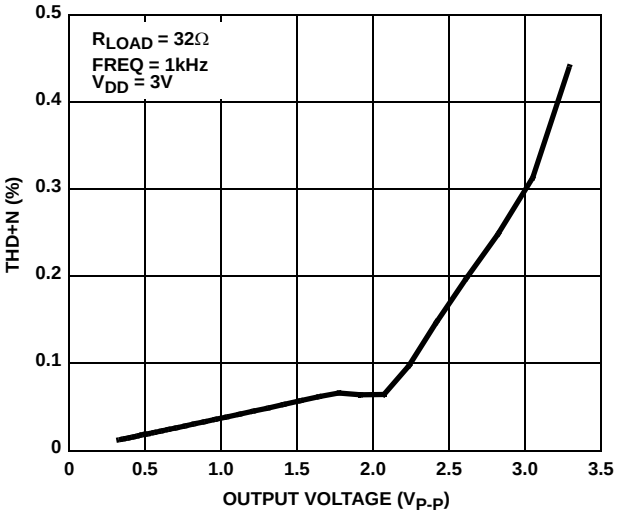


FIGURE 10. THD+N vs OUTPUT VOLTAGE

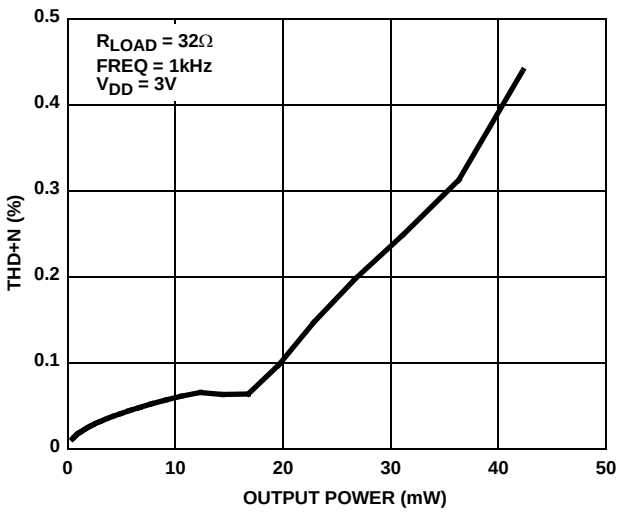
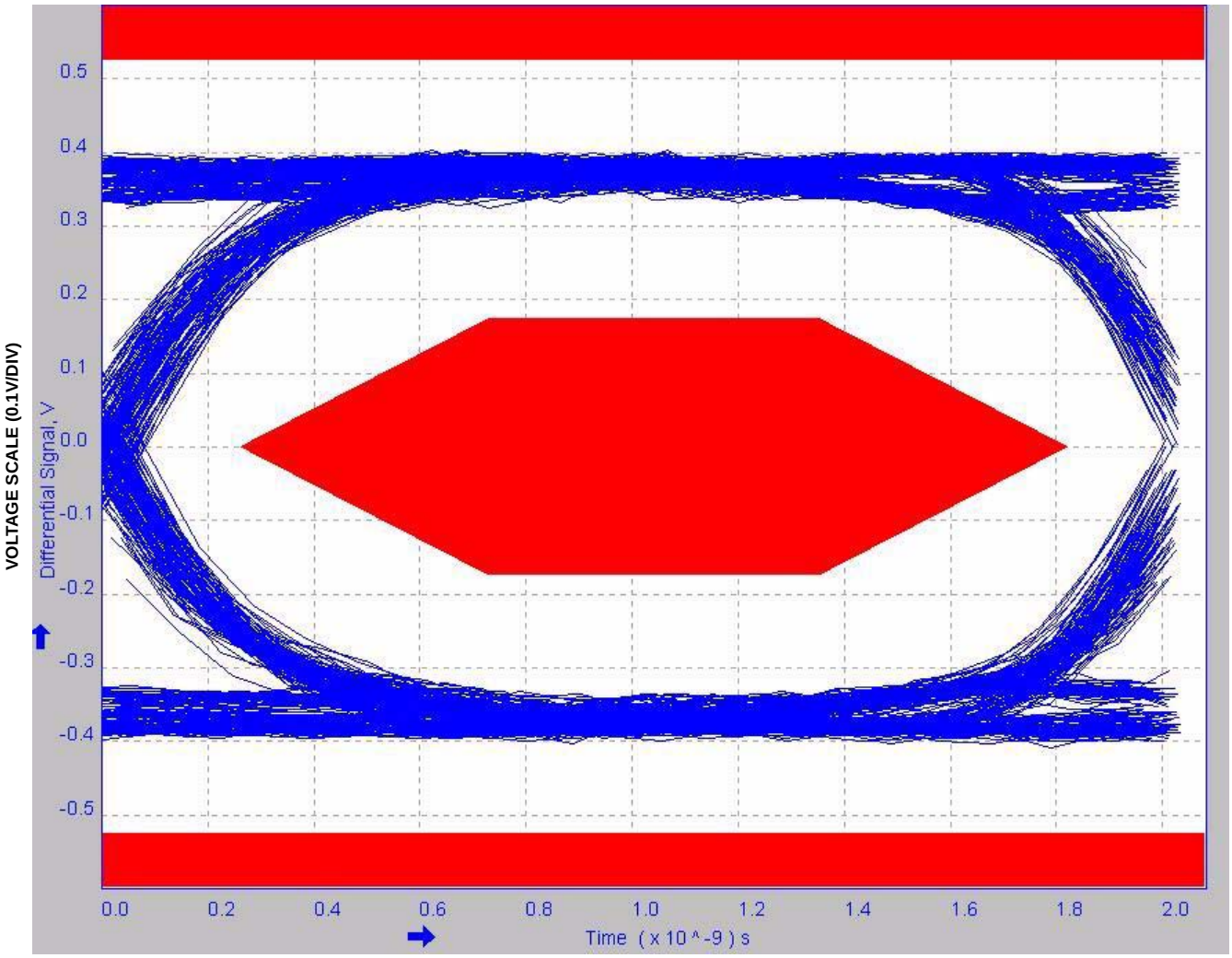


FIGURE 11. THD+N vs OUTPUT POWER

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**



VOLTAGE SCALE (0.1V/DIV)

TIME SCALE (10ns/DIV)

FIGURE 12. EYE PATTERN: 480Mbps WITH SWITCH IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

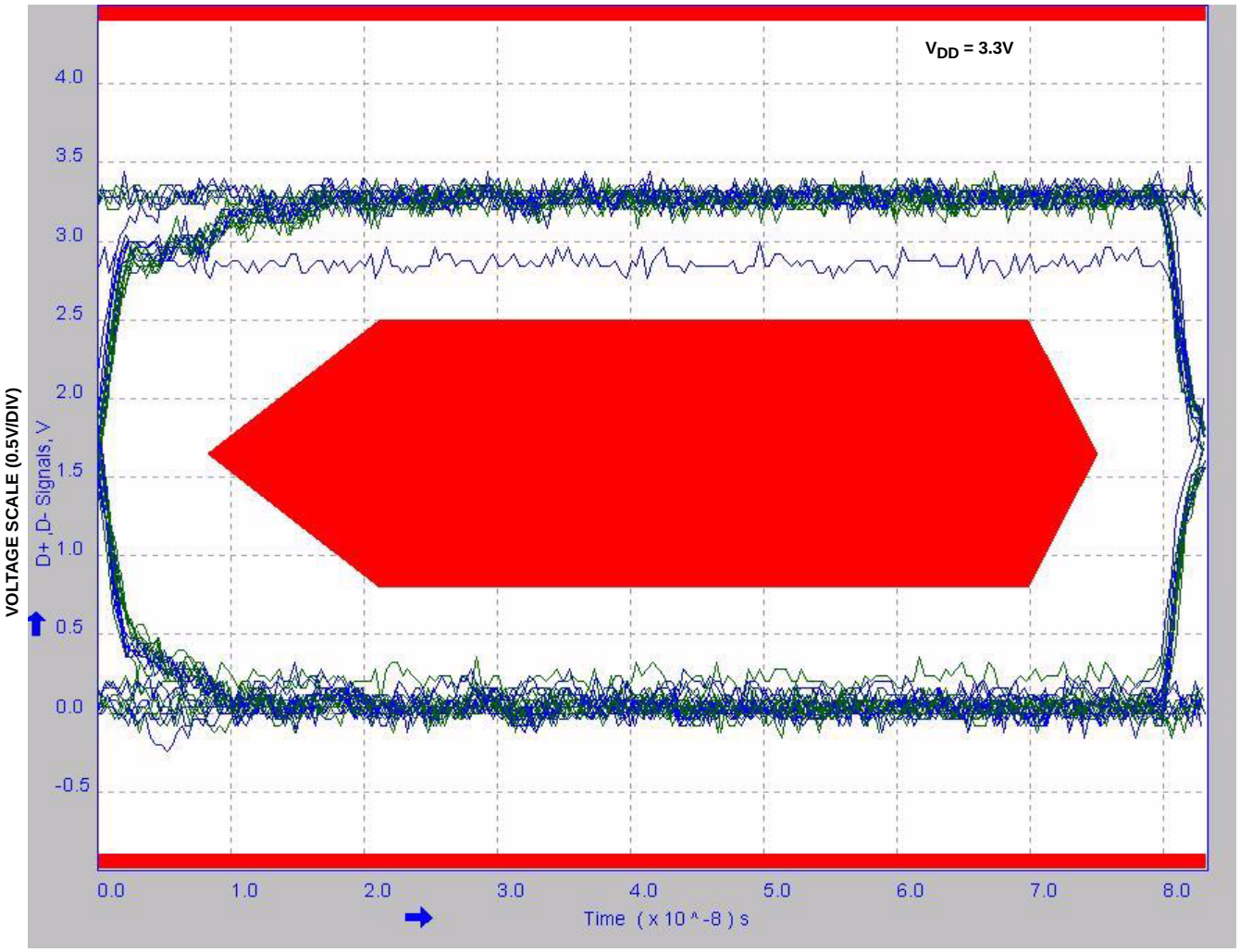


FIGURE 13. EYE PATTERN: 12MBps WITH SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

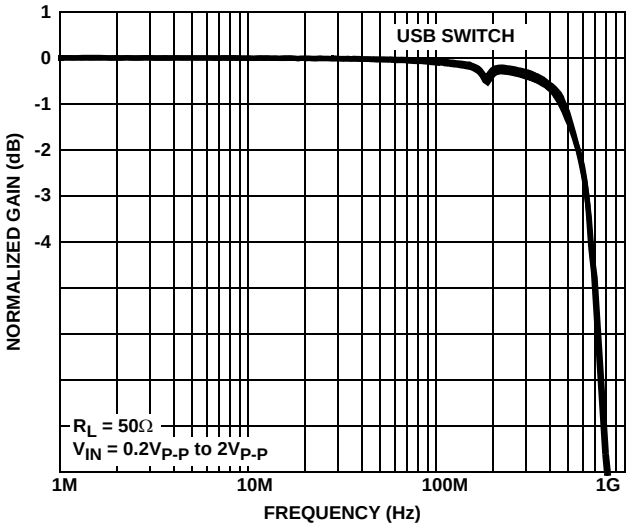


FIGURE 14. FREQUENCY RESPONSE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

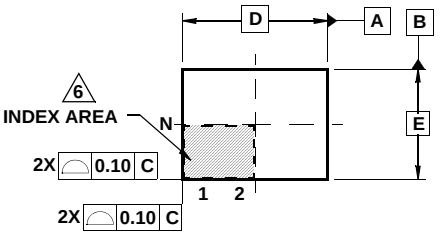
TRANSISTOR COUNT:

98

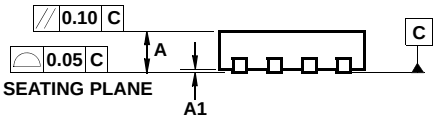
PROCESS:

Submicron CMOS

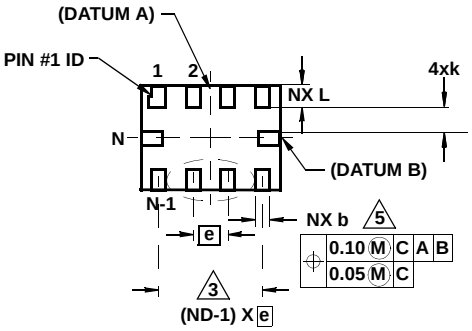
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



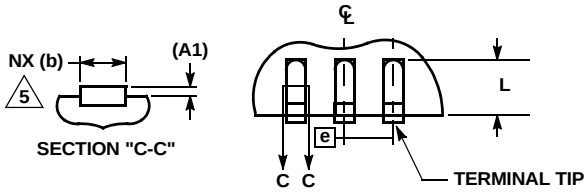
TOP VIEW



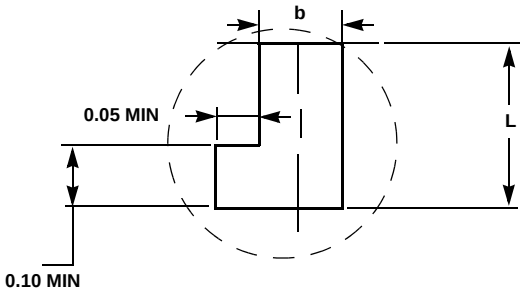
SIDE VIEW



BOTTOM VIEW



FOR ODD TERMINAL/SIDE



DETAIL “A” PIN 1 ID

L10.2.1x1.6A

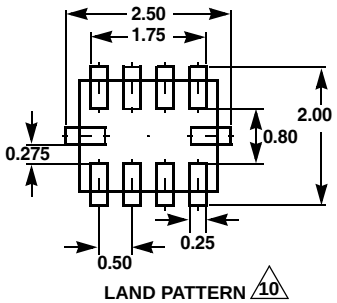
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		10		2
Nd		4		3
Ne		1		3
θ	0	-	12	4

Rev. 3 6/06

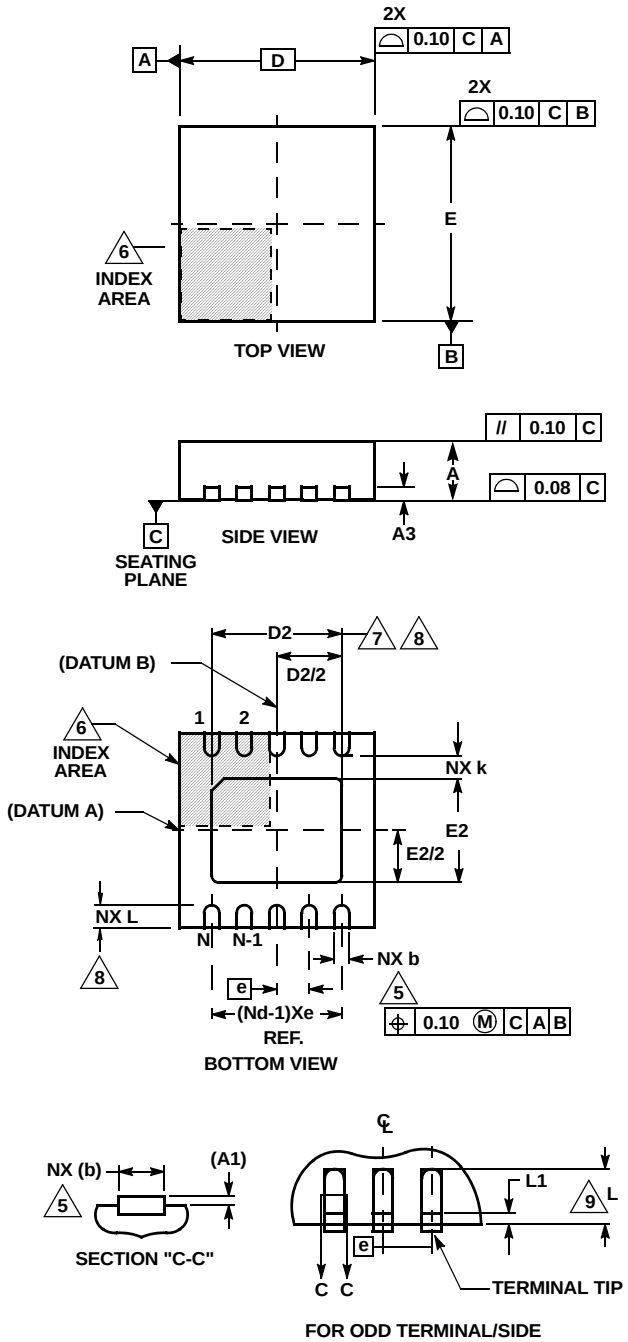
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



LAND PATTERN 10

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N		10		2
Nd		5		3

Rev. 3 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.