

## TC7MH573FK

## Octal D-Type Latch with 3-State Output

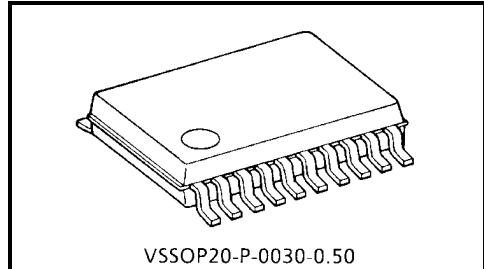
The TC7MH573FK is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

This 8 bit D-type latch is controlled by a latch enable input (LE) and a output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.



Weight: 0.03 g (typ.)

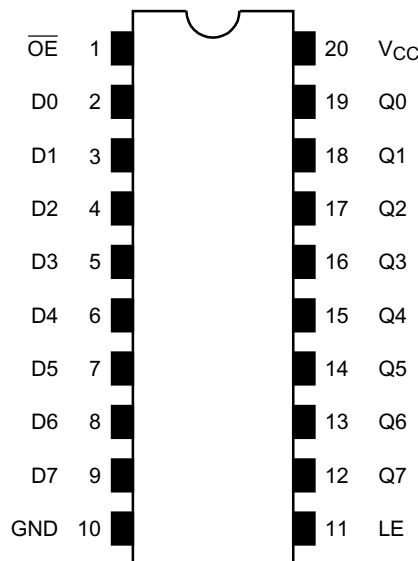
## Features

- High speed:  $t_{pd} = 4.5$  ns (typ.) ( $V_{CC} = 5$  V)
- Low power dissipation:  $I_{CC} = 4 \mu A$  (max) ( $T_a = 25^\circ C$ )
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range:  $V_{CC}$  (opr) = 2~5.5 V
- Low noise:  $V_{OLP} = 1.0$  V (max)
- Pin and function compatible with 74ALS573

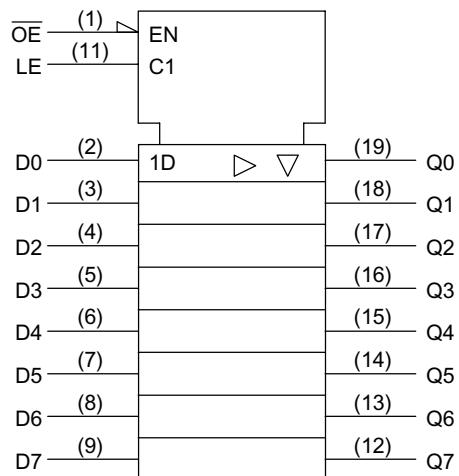
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## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

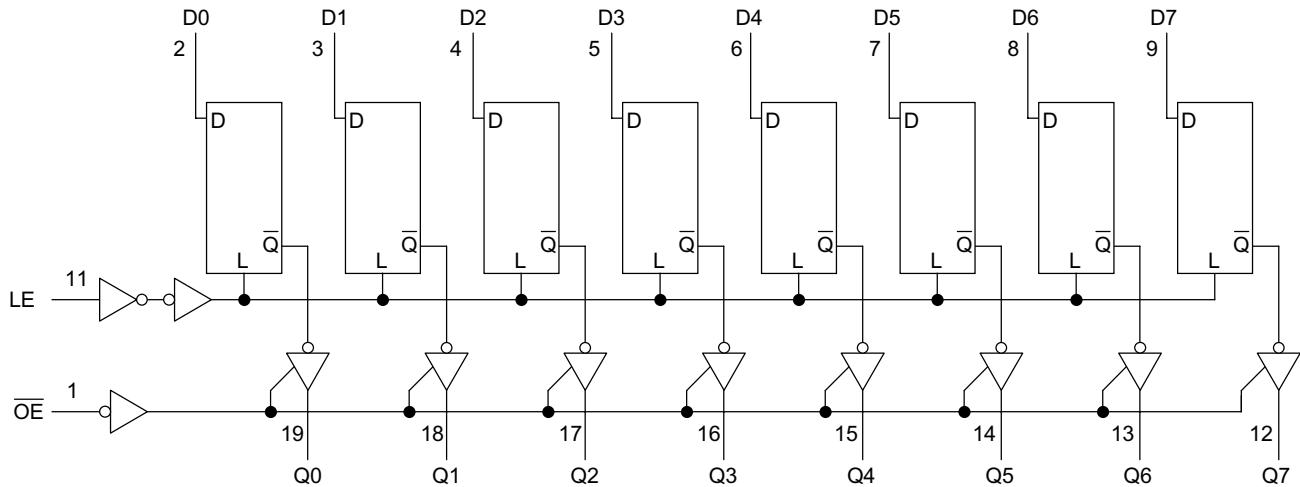
Inputs			Outputs
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	$Q_n$
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

 $Q_n$ : Q outputs are latched at the time when the LE input is taken to a low logic level.

## System Diagram



**Maximum Ratings**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5~7.0	V
DC input voltage	$V_{IN}$	-0.5~7.0	V
DC output voltage	$V_{OUT}$	-0.5~ $V_{CC}$ + 0.5	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65~150	°C

**Recommended Operating Conditions**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0~5.5	V
Input voltage	$V_{IN}$	0~5.5	V
Output voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating temperature	$T_{opr}$	-40~85	°C
Input rise and fall time	$dt/dv$	0~100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0~20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

## Electrical Characteristics

## DC Characteristics

Characteristics		Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		Unit		
Input voltage	High level				Min	Typ.	Max	Min	Max			
Input voltage	Low level	V <sub>IL</sub>	—	2.0	1.50	—	—	1.50	—	V		
				3.0~5.5	V <sub>CC</sub> × 0.7	—	—	V <sub>CC</sub> × 0.7	—			
Output voltage	High level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	V		
				3.0	2.9	3.0	—	2.9	—			
				4.5	4.4	4.5	—	4.4	—			
	Low level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	V		
				I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80			
				I <sub>OL</sub> = 50 μA	2.0	—	0	0.1	—			
3-state output off-state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.25	—	±2.50	μA	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0~5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA	

Timing Requirements (Input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40~85°C		Unit
				Typ.	Limit	Typ.	Limit	
Minimum pulse width (LE)	t <sub>w</sub> (H)	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	— —	5.0 5.0	ns
Minimum set-up time	t <sub>s</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	3.5 3.5	— —	3.5 3.5	ns
Minimum hold time	t <sub>h</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	1.5 1.5	— —	1.5 1.5	ns

AC Characteristics (Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit	
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max		
Propagation delay time (LE-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	3.3 ± 0.3	15	—	7.6	11.9	1.0	14.0
				50	—	10.1	15.4	1.0	17.5
			5.0 ± 0.5	15	—	5.0	7.7	1.0	9.0
				50	—	6.5	9.7	1.0	11.0
Propagation delay time (D-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	3.3 ± 0.3	15	—	7.0	11.0	1.0	13.0
				50	—	9.5	14.5	1.0	16.5
			5.0 ± 0.5	15	—	4.5	6.8	1.0	8.0
				50	—	6.0	8.8	1.0	10.0
3-state output enable time	t <sub>pZL</sub> t <sub>pZH</sub>	R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	15	—	7.3	11.5	1.0	13.5
				50	—	9.8	15.0	1.0	17.0
			5.0 ± 0.5	15	—	5.2	7.7	1.0	9.0
				50	—	6.7	9.7	1.0	11.0
3-state output disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	50	—	10.7	14.5	1.0	16.5
			5.0 ± 0.5	50	—	6.7	9.7	1.0	11.0
Output to output skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note1)	3.3 ± 0.3	50	—	—	1.5	—	1.5
			5.0 ± 0.5	50	—	—	1.0	—	1.0
Input capacitance	C <sub>IN</sub>	—	—	—	4	10	—	10	pF
Output capacitance	C <sub>OUT</sub>	—	—	—	6	—	—	—	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note2)			—	29	—	—	pF

Note1: This parameter is guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLM} - t_{pHLn}|$$

Note2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

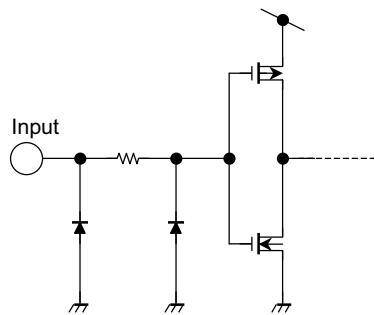
And the total C<sub>PD</sub> when n pcs of latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 21 + 8 \cdot n$$

Noise Characteristics (Input:  $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.8	1.0	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.8	-1.0	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

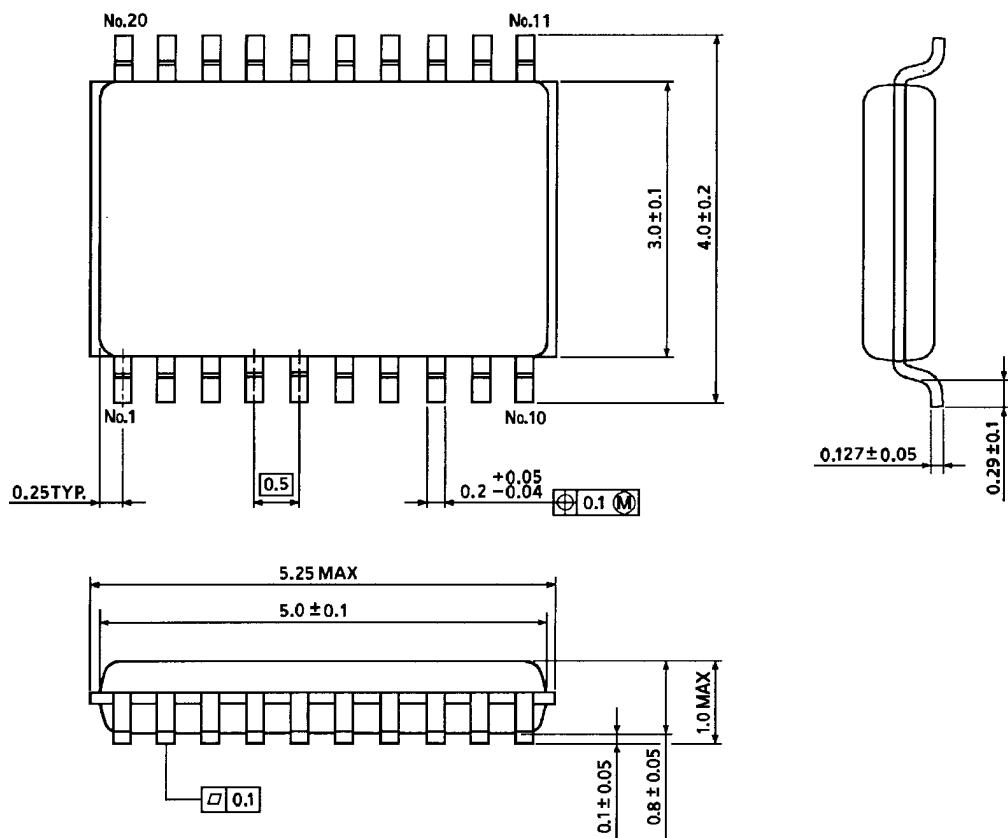
## Input Equivalent Circuit



**Package Dimensions**

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)