# **Signetics**

## 74LS283 Adder

4-Bit Full Adder With Fast Carry Product Specification

## **Logic Products**

## **FEATURES**

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal carry lookahead

## DESCRIPTION

The '283 adds two 4-bit binary words ( $A_n$  plus  $B_n$ ) plus the incoming carry. The binary sum appears on the Sum outputs ( $\Sigma_1 - \Sigma_4$ ) and the outgoing carry ( $C_{OUT}$ ) according to the equation:

$$\begin{array}{l} C_{\text{IN}} + (A_1 + B_1) + 2(A_2 + B_2) \\ + 4(A_3 + B_3) + 8(A_4 + B_4) \\ = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{\text{OUT}} \\ \text{Where (+)} = \text{plus.} \end{array}$$

Due to the symmetry of the binary add function, the '283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic) – see Function Table. In case of all active LOW operands the results  $\Sigma_1 - \Sigma_4$  and  $C_{\rm OUT}$  should be interpreted also as active LOW. With active HIGH inputs,  $C_{\rm IN}$  cannot be left open; it must be held LOW when no "carry in" is

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS283	13ns	20mA

## ORDERING CODE

PACKAGES	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±5%; T <sub>A</sub> = 0°C to +70°C
Plastic DIP	N74LS283N
Plastic SO-16	N74LS283D

#### NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

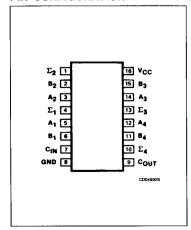
PINS	DESCRIPTION	74LS
A, B	Inputs	2LSul
C <sub>IN</sub>	Input	1LSul
All	Outputs	10LSul

## NOTE:

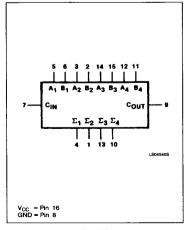
A 74LS unit load (LSul) is 20 µA IIH and -0.4mA IIL.

intended. Interchanging inputs of equal thus  $C_{IN}$ ,  $A_1$ ,  $B_1$  can arbitrarily be asweight does not affect the operation, signed to pins 5, 6, 7, etc.

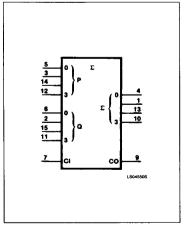
#### PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



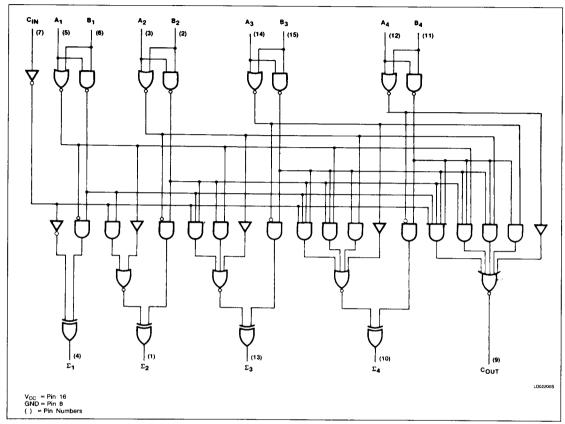
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## LOGIC DIAGRAM



## **FUNCTION TABLE**

PINS	CIN	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	A <sub>4</sub>	B <sub>1</sub>	B <sub>2</sub>	В3	B <sub>4</sub>	Σ1	Σ2	Σ3	Σ4	C <sub>OUT</sub>
Logic levels	L	L	Н	L	Н	Н	L	L	Н	н	Н	L	L	Н
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Example: 1001 1010 10011 (10 + 9 = 19) (carry + 5 + 6 = 12)

H = HIGH voltage level

L = LOW voltage level

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	74LS	UNIT
V <sub>CC</sub>	Supply voltage	7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +1	mA
V <sub>OUT</sub>	Voltage applied to output in HIGH output state	-0.5 to +V <sub>CC</sub>	V
TA	Operating free-air temperature range	0 to 70	°C

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## RECOMMENDED OPERATING CONDITIONS

	PARAMETER	Min	Nom	Max	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5.0	5.25	٧
V <sub>1H</sub>	HIGH-level input voltage	2.0			V
V <sub>IL</sub>	LOW-level input voltage			+ 0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
Гон	HIGH-level output current			-400	μА
lor	LOW-level output current			8	mA
TA	Operating free-air temperature	0		70	°C

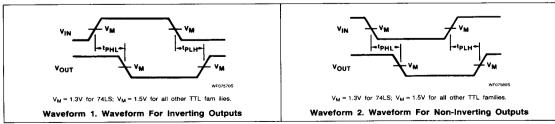
## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER					74LS283		
		. TEST COND	Min	Typ <sup>2</sup>	Max	UNIT	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>I</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OH</sub> = MAX		3.4		٧
V <sub>OL</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN,	I <sub>OL</sub> = MAX		0.35	0.5	٧
	LOW-level output voltage	V <sub>IL</sub> = MAX	I <sub>OL</sub> = 4mA (74LS)		0.25	0.4	٧
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-1.5	٧
	Input current at maximum		A, B inputs			0.2	mA
l <sub>l</sub>	input voltage	$V_{CC} = MAX, V_I = 7.0V$	C <sub>IN</sub> input			0.1	mA
		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V	A, B inputs			40	μΑ
l <sub>iH</sub>	HIGH-level input current		C <sub>IN</sub> input			20	μΑ
			A, B inputs			-0.8	mA
ΉL	LOW-level input current	input current $V_{CC} = MAX, V_I = 0.4V$	C <sub>IN</sub> input			-0.4	mA
los	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-20		-100	mA
			Condition 1		22	39	mA
lcc	Supply current <sup>4</sup> (total)	V <sub>CC</sub> = MAX	Condition 2		19	34	mA
_ 2			Condition 3	1	19	34	mA

## NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- 2. All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25$ °C.
- 3. Ios is tested with V<sub>OUT</sub> = +0.5V and V<sub>CC</sub> = V<sub>CC</sub> MAX +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- 4.  $I_{\text{CC}}$  should be measured with all outputs open and the following conditions:
  - Condition 1: All inputs grounded.
  - Condition 2: All B inputs LOW, other inputs at 4.5V.
  - Condition 3: All inputs at 4.5V.

## **AC WAVEFORMS**



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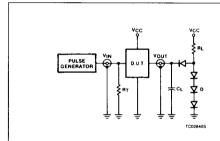
## Adder

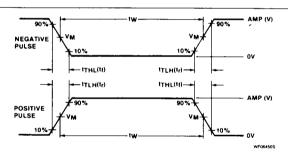
74LS283

## AC ELECTRICAL CHARACTERISTICS TA = 25°C, VCC = 5.0V

				74LS		
	PARAMETER	TEST CONDITIONS	C <sub>L</sub> = 15pF	UNIT		
			Min	Max	7	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $C_{\text{IN}}$ to $\Sigma_1$	Waveforms 1 & 2		24 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $C_{\text{IN}}$ to $\Sigma_2$	Waveforms 1 & 2		24 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $C_{\text{IN}}$ to $\Sigma_3$	Waveforms 1 & 2		24 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $C_{\text{IN}}$ to $\Sigma_4$	Waveforms 1 & 2		24 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $A_i$ or $BV_i$ to $\Sigma_i$	Waveforms 1 & 2		24 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay C <sub>IN</sub> to C <sub>OUT</sub>	Waveform 2		17 22	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>I</sub> or B <sub>I</sub> to C <sub>OUT</sub>	Waveforms 1 & 2		17 17	ns	

## TEST CIRCUITS AND WAVEFORMS





 $V_M = 1.3V$  for 74LS;  $V_M = 1.5V$  for all other TTL families.

Input Pulse Definition

## Test Circuit For 74 Totem-Pole Outputs

## **DEFINITIONS**

R<sub>L</sub> = Load resistor to V<sub>CC</sub>; see AC CHARACTERISTICS for value.

C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

 $t_{\mathsf{TLH}},\,t_{\mathsf{THL}}$  Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS								
FAMILI	Amplitude	Rep. Rate	Pulse Width	t <sub>TLH</sub>	t <sub>THL</sub>				
74	3.0V	1MHz	500ns	7ns	7ns				
74LS	3.0V	1MHz	500ns	15ns	6ns				
748	3.0V	1MHz	500ns	2.5ns	2.5ns				