Description

The uClamp™0503C is a three line flip chip Transient Voltage Suppressor (TVS). MicroClamp's are state-of-the-art devices that utilize solid-state technology for superior clamping performance and DC electrical characteristics. These devices are designed to protect sensitive semiconductor components from damage or latch-up due to cable discharge events (CDE), electro-static discharge (ESD) and other voltage induced transient events.

The uClamp0503C is a 4-bump, 0.5mm pitch flip chip array with a 2 x 2 bump grid. It measures approximately 1.0 x 0.9 x 0.65 mm. This small outline makes these devices especially well suited for portable applications.

Each device will protect two bidirectional (signal swings above and below ground) or three unidirectional (signal above ground) lines. The flip chip design results in lower inductance, virtually eliminating voltage overshoot due to leads and interconnecting bond wires. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

The uClamp0503C is fabricated using Semtech's proprietary solid-state process technology. It is bidirectional and may be used on lines where the signal swings above and below ground. The uClamp0503C is for use on lines operating up to 5.0 volts.

Features

- 150 Watts peak pulse power (tp = 8/20µs)
- Transient protection for data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 12A (8/20µs)
- Small chip scale package requires less board space
- Low profile (< 0.65mm)
- No need for underfill material
- Protects up to three data or I/O lines
- Low clamping voltage
- Working voltage: 5.0V
- Solid-state technology

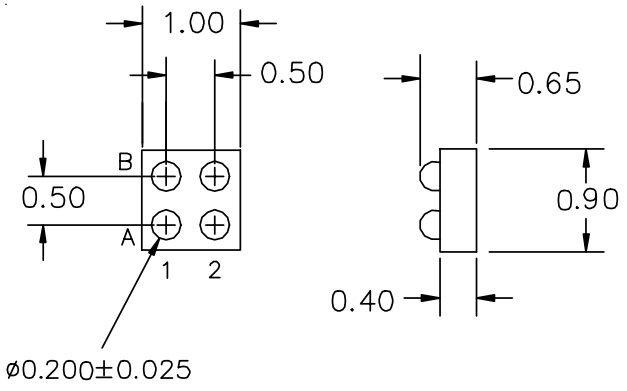
Mechanical Characteristics

- JEDEC MO-211, Variation BA, 0.50 mm Pitch Flip Chip Package
- RoHS/WEEE Compliant
- Marking : Marking Code + Orientation Mark
- Non-conductive top side coating
- Packaging : Tape and Reel

Applications

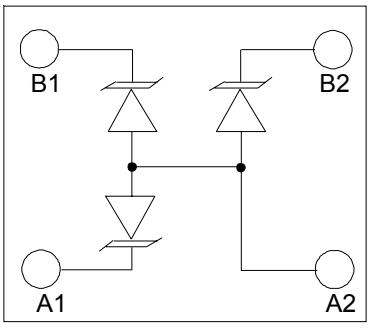
- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDA's)
- Notebook & Hand Held Computers
- Portable Instrumentation
- Pagers
- Smart Cards
- MP3 Players

Device Dimensions



Maximum Dimensions (mm)

Schematic & PIN Configuration



2 x 2 Grid Flip Chip TVS (Bump Up View)

Absolute Maximum Rating

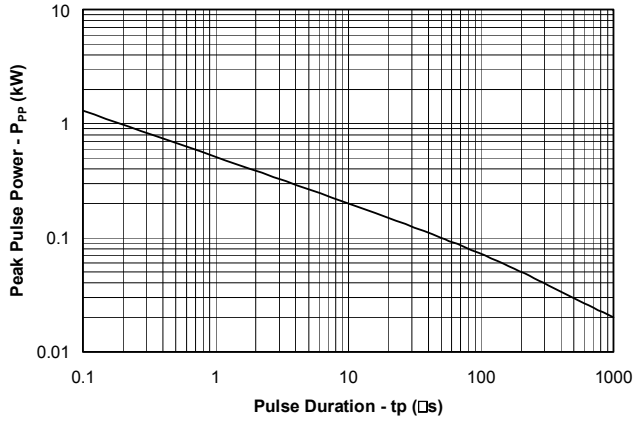
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	150	Watts
Maximum Peak Pulse Current (tp = 8/20µs)	I_{pp}	13	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{PP}	+/- 20 +/- 15	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

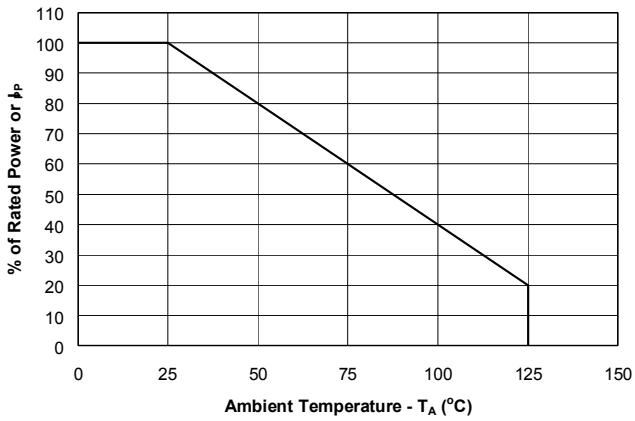
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20µs I/O to Ground			9.8	V
Clamping Voltage	V_C	I_{PP} = 13A, tp = 8/20µs I/O to Ground			10	V
Clamping Voltage	V_C	I_{PP} = 13A, tp = 8/20µs I/O to I/O			11.5	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz I/O to Ground			100	pF
Junction Capacitance	C_j	V_R = 0V, f = 1MHz I/O tol/O			50	pF

Typical Characteristics

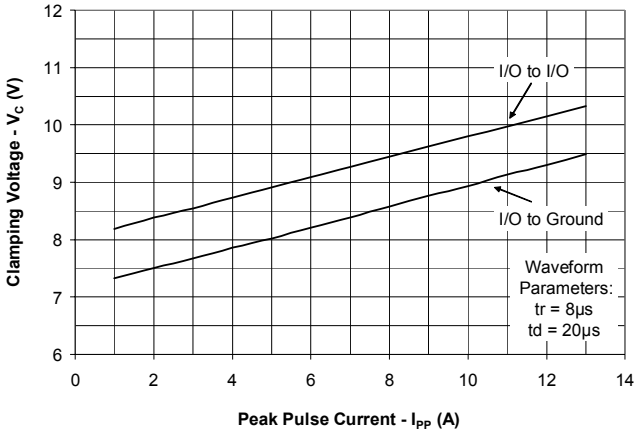
Non-Repetitive Peak Pulse Power vs. Pulse Time



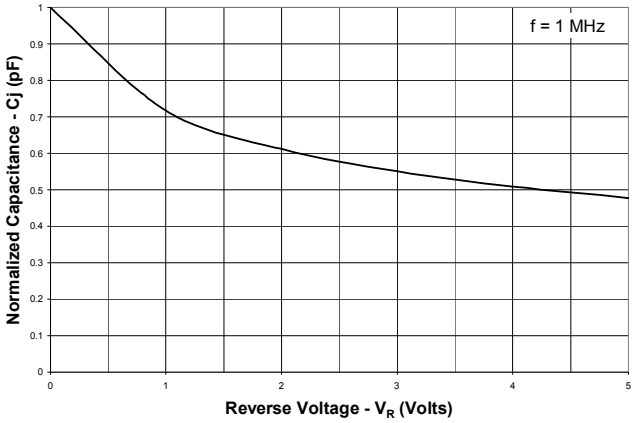
Power Derating Curve



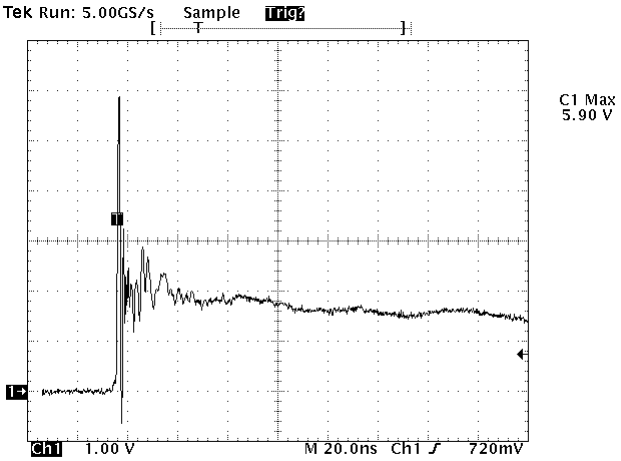
Clamping Voltage vs. Peak Pulse Current



Normalized Capacitance vs. Reverse Voltage



ESD Clamping (8kV Contact Discharge)



Applications Information

Device Connection Options

The uClamp0503C has solder bumps located in a 2 x 2 matrix layout on the active side of the device. The bumps are designated as A1, A2, B1, and B2. The lines to be protected are connected at bumps A1, B1, and B2. Bump A2 is connected to ground. For protection of two bidirectional lines, connect one of the I/O pins to ground and leave Bump A2 not connected. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.

Flip Chip TVS

Flip Chip TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting the flip chip TVS. Solder mask defined (SMD) pads produce stress points near the solder mask on the PCB side that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.225 ± 0.010 mm with a solder mask opening of 0.350 ± 0.025 mm. The stencil should be laser cut and electro-polished with a nominal thickness of 0.100mm.

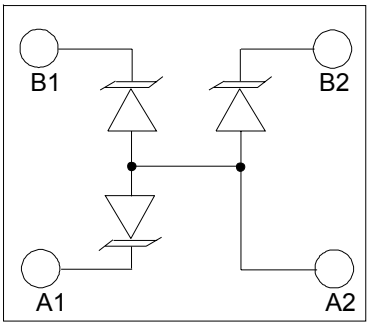
Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

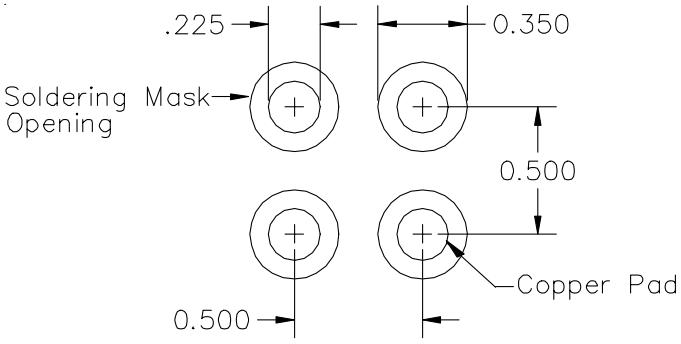
Reflow Profile

The flip chip TVS can be assembled using the reflow requirements for IPC/JEDEC standard J-STD-020B for Sn-Pb eutectic assembly of small body components. During reflow, the component will self-align itself on the pad.

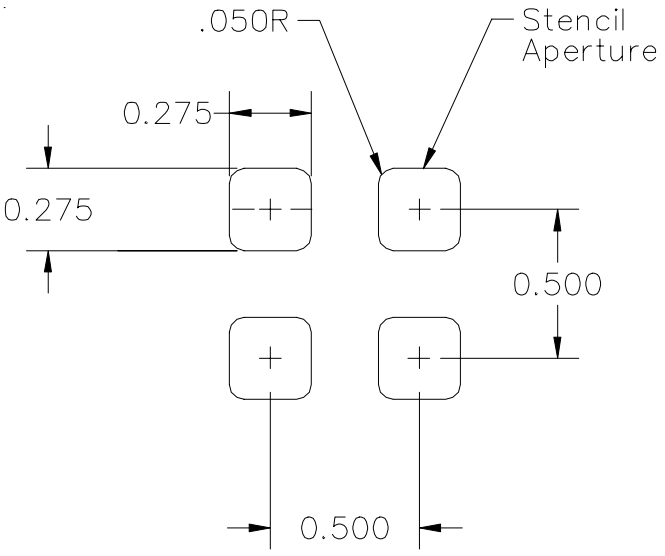
Device Schematic & Pin Configuration



NSMD Package Footprint (Dimensions in mm)



Stencil Design

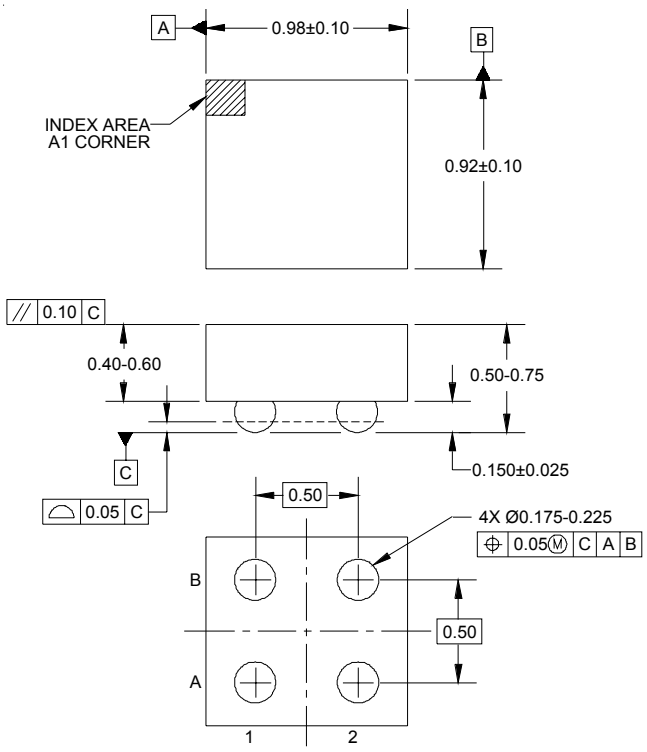


Assembly Guideline for Pb-Free Soldering

The following are recommendations for the assembly of this device:

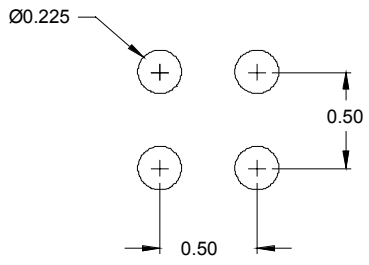
Assembly Parameter	Recommendation
Solder Ball Composition	95.5Sn/3.8Ag/0.7Cu
Solder Stencil Design	Same as the SnPb design
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Composition	Sn Ag (3-4) Cu (0.5-0.9)
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	per JEDEC J-STD-020
PCB Solder Pad Design	Same as the SnPb Design
PCB Pad Finish	OSP or AuNi

Outline Drawing



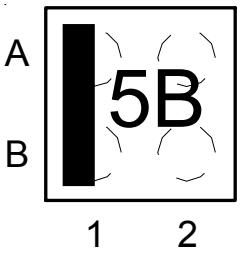
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. REFERENCE JEDEC REGISTRATION MO-211.
3. Sn63/Pb37 FOR STANDARD DEVICES OR Sn95.5/Ag3.8/Cu0.7 FOR Pb-FREE DEVICES.

Land Pattern



NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking



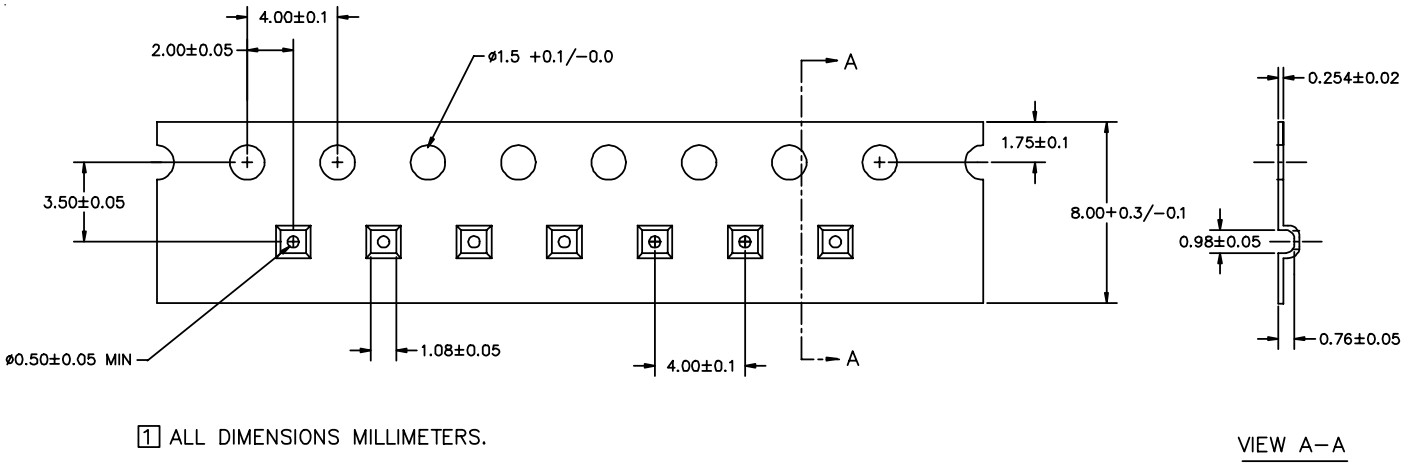
2 x 2 Grid Flip Chip TVS (Top View)

Top Coating: The top (non-bump side) of the device is coated with a white, non-conductive coating. The coating is laser markable and helps prevent die chipping during the PCB assembly process. This material is compliant with UL 94V-0 flammability requirements.

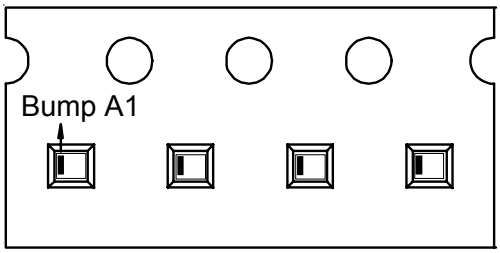
Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
uClamp0503C.WC	SnPb	3,000	7 Inch
uClamp0503C.WCT	SnAgCu	3,000	7 Inch

Tape and Reel Specification



Tape Specifications



Device Orientation in Tape

Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804