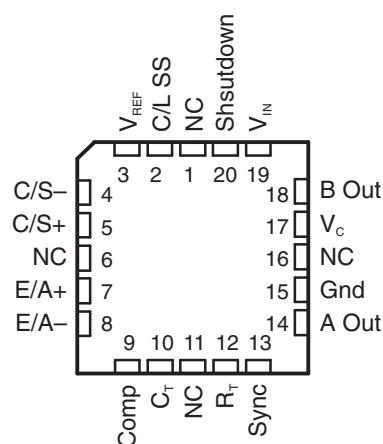


## RAD-TOLERANT CLASS-V, CURRENT-MODE PWM CONTROLLER

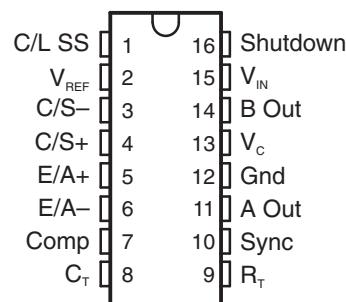
### FEATURES

- QML-V Qualified, SMD 5962-86806
- Rad-Tolerant: 30 kRad (Si) TID <sup>(1)</sup>
- Automatic Feed-Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-Pull Configuration
- Enhanced Load Response Characteristics
- Parallel-Operation Capability for Modular Power Systems
- Differential Current-Sense Amplifier With Wide Common-Mode Range
- Double-Pulse Suppression
- 500-mA (Peak) Totem-pole Outputs
- $\pm 1\%$  Bandgap Reference
- Undervoltage Lockout
- Soft-Start Capability
- Shutdown Terminal
- 500-kHz Operation

**FK PACKAGE  
(TOP VIEW)**



**J PACKAGE  
(TOP VIEW)**



(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

### DESCRIPTION

The UC1846 control devices provide all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double-pulse suppression, deadline adjust capability, a  $\pm 1\%$  trimmed bandgap reference, and low outputs in the OFF state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

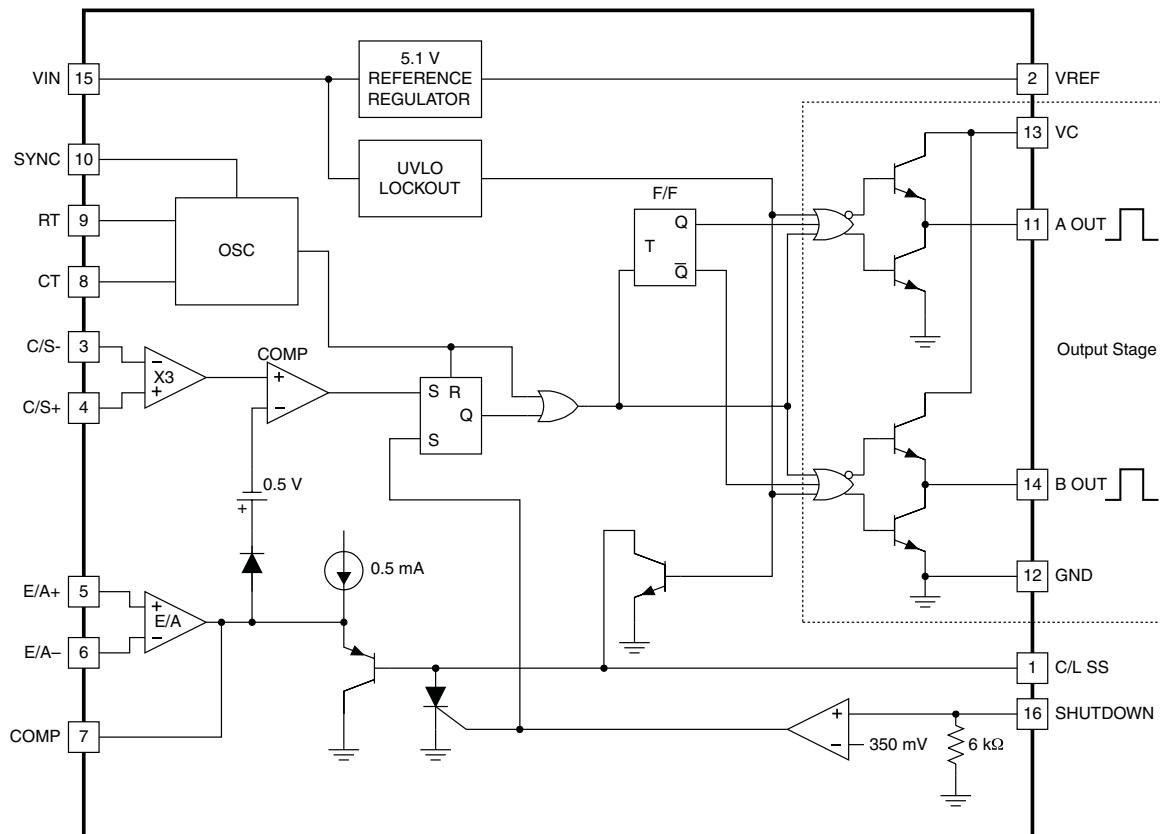
ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – J	5962-8680603VEA	UC1846J-SP
	LCCC – FK	5962-8680603V2A	UC1846FK-SP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

## BLOCK DIAGRAM



NOTE: Pin numbers shown are for the J package.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

$V_{CC}$	Supply voltage	40 V
	Collector supply voltage	40 V
$I_O$	Output current, source or sink	500 mA
$V_I$	Analog input voltage (C/S-, C/S+, E/A+, E/A-, Shutdown)	-0.3 V to $V_{IN}$
	Reference output current	-30 mA
	Sync output current	-5 mA
	Error amplifier output current	-5 mA
	Soft-start sink current	50 mA
	Oscillator charging current	5 mA
$P_D$	Power dissipation	$T_A = 25^\circ\text{C}$
		$T_C = 25^\circ\text{C}$
$T_{stg}$	Storage temperature range	-65°C to 150°C
$T_{lead}$	Lead temperature (soldering, 10 seconds)	300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

**ELECTRICAL CHARACTERISTICS**
 $V_{IN} = 15 \text{ V}$ ,  $R_T = 10\text{k}\Omega$ ,  $C_T = 4.7 \text{ nF}$ ,  $T_A = T_J = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Reference Section</b>					
Output voltage	$T_J = 25^\circ\text{C}$ , $I_O = 1 \text{ mA}$	5.04	5.10	5.16	V
Line regulation	$V_{IN} = 8 \text{ V}$ to $40 \text{ V}$		5	20	mV
Load regulation	$I_L = 1 \text{ mA}$ to $10 \text{ mA}$		3	15	mV
Temperature stability	Over operating range		0.4		mV/°C
Total output variation	Over line, load, and temperature <sup>(1)</sup>	5		5.2	V
Output noise voltage	$10 \text{ Hz} \leq f \leq 10 \text{ kHz}$ , $T_J = 25^\circ\text{C}$ <sup>(1)</sup>		100		µV
Long-term stability	$T_J = 125^\circ\text{C}$ , 1000 hr		5		mV
Short-circuit output current	$V_{REF} = 0 \text{ V}$	-10	-45		mA
<b>Oscillator Section</b>					
Initial accuracy	$T_J = 25^\circ\text{C}$	39	43	47	kHz
Voltage stability	$V_{IN} = 8 \text{ V}$ to $40 \text{ V}$		-1	2	%
Temperature stability	Over operating range		-1		%
Sync output high level		3.9	4.35		V
Sync output low level			2.3	2.5	V
Sync input high level	$C_T = 0 \text{ V}$	3.9			V
Sync input low level	$C_T = 0 \text{ V}$			2.5	V
Sync input current	Sync = $5.25 \text{ V}$ , $C_T = 0 \text{ V}$		1.3	1.5	mA
<b>Error Amp Section</b>					
Input offset voltage		0.5	5		mV
Input bias current		-1	-0.6		µA
Input offset current		40	250		nA
Common mode range	$V_{IN} = 8 \text{ V}$ to $40 \text{ V}$	0	$V_{IN} - 2$		V
Open-loop voltage gain	$\Delta V_O = 1.2 \text{ V}$ to $3 \text{ V}$ , $V_{CM} = 2 \text{ V}$	80	105		dB
Unity-gain bandwidth	$T_J = 25^\circ\text{C}$ <sup>(1)</sup>	0.7	1		MHZ
CMRR	$V_{CM} = 0 \text{ V}$ to $38 \text{ V}$ , $V_{IN} = 40 \text{ V}$	75	100		dB

(1) Parameters ensured by design and/or characterization, if not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 15 \text{ V}$ ,  $R_T = 10\text{k}\Omega$ ,  $C_T = 4.7 \text{ nF}$ ,  $T_A = T_J = -55^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	$V_{IN} = 8 \text{ V}$ to $40 \text{ V}$	80	105		dB
Output sink current	$V_{ID} = -15 \text{ mV}$ to $-5 \text{ V}$ , Comp = $1.2 \text{ V}$	2	6		mA
Output source current	$V_{ID} = 15 \text{ mV}$ to $5 \text{ V}$ , Comp = $2.5 \text{ V}$		-0.5	-0.4	mA
High-level output voltage	$R_L = (\text{Comp}) 15 \text{ k}\Omega$	4.3	4.6		V
Low-level output voltage	$R_L = (\text{Comp}) 15 \text{ k}\Omega$		0.7	1	V
<b>Current Sense Amplifier Section</b>					
Amplifier gain	$V_{C/S-} = 0 \text{ V}$ , C/L SS open <sup>(2)(3)</sup>	2.5	2.75	3.1	V/V
Maximum differential input signal ( $V_{C/S+} - V_{C/S-}$ )	C/L SS open <sup>(2)</sup> , $R_L$ (Comp)= $15 \text{ k}\Omega$	1.1	1.2		V
Input offset voltage	$V_{C/L \text{ SS}} = 0.5 \text{ V}$ , Comp open <sup>(2)</sup>		5	25	mV
CMRR	$V_{CM} = 1 \text{ V}$ to $12 \text{ V}$	60	83		dB
PSRR	$V_{IN} = 8 \text{ V}$ to $40 \text{ V}$	60	84		dB
Input bias current	$V_{C/L \text{ SS}} = 0.5 \text{ V}$ , Comp open <sup>(2)</sup>	-10	-2.5		µA
Input offset current	$V_{C/L \text{ SS}} = 0.5 \text{ V}$ , Comp open <sup>(2)</sup>		0.08	1	µA
Input common-mode range				$V_{IN} - 3$	V
Delay to outputs	$T_J = 25^\circ\text{C}$ <sup>(4)</sup>	200	500		ns
<b>Current Limit Adjust Section</b>					
Current limit offset	$V_{C/S-} = 0 \text{ V}$ , $V_{C/S+} = 0 \text{ V}$ , Comp open <sup>(5)</sup>	0.45	0.5	0.55	V
Input bias current	$V_{E/A+} = V_{REF}$ , $V_{E/A-} = 0 \text{ V}$	-30	-10		µA
<b>Shutdown Terminal Section</b>					
Threshold voltage		250	350	400	mV
Input voltage range		0	$V_{IN}$		V
Minimum latching current ( $I_{C/S \text{ SS}}$ ) <sup>(6)</sup>		3	1.5		mA
Maximum non-latching current ( $I_{C/S \text{ SS}}$ ) <sup>(7)</sup>			1.5	0.8	mA
Delay to outputs	$T_J = 25^\circ\text{C}$ <sup>(4)</sup>	300	600		ns
<b>Output Section</b>					
Collector-emitter voltage		40			V
Collector leakage current	$V_C = 40 \text{ V}$		200		µA
Output low-level voltage	$I_{SINK} = 20 \text{ mA}$		0.1	0.4	V
	$I_{SINK} = 100 \text{ mA}$		0.4	2.1	V
Output high-level voltage	$I_{SOURCE} = 20 \text{ mA}$	13	13.5		V
	$I_{SOURCE} = 100 \text{ mA}$	12	13.5		V
Rise time	$C_L = 1 \text{ nF}$ , $T_J = 25^\circ\text{C}$ <sup>(4)</sup>	50	300		ns
Fall time	$C_L = 1 \text{ nF}$ , $T_J = 25^\circ\text{C}$ <sup>(4)</sup>	50	300		ns
<b>Undervoltage Lockout Section</b>					
Start-up threshold		7.7	8		V
Threshold hysteresis		0.75			V
<b>Total Standby Current</b>					
Supply current		17	21		mA

(2) Parameter measured at trip point of latch with  $V_{E/A+} = V_{REF}$ ,  $V_{E/A-} = 0 \text{ V}$ .

(3) Amplifier gain defined as:  $G = \Delta V_{\text{Comp}} / \Delta V_{C/S+}$ ;  $V_{C/S+} = 0$  to  $1 \text{ V}$ .

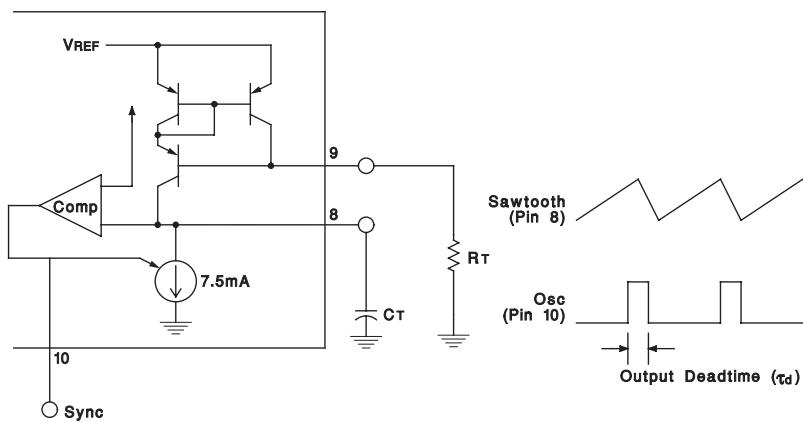
(4) Parameters ensured by design and/or characterization, if not production tested.

(5) Parameter measured at trip point of latch with  $V_{E/A+} = V_{REF}$ ,  $V_{E/A-} = 0 \text{ V}$ .

(6) Current into C/S SS required to latch circuit in shutdown state.

(7) Current into C/S SS assured not to latch circuit in shutdown state.

## APPLICATION INFORMATION



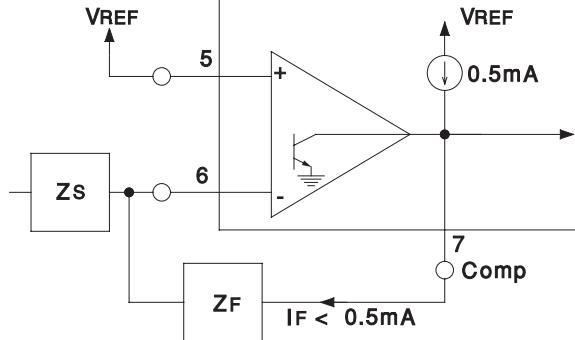
Output deadtime is determined by the external capacitor,  $C_T$ , according to the formula:  $\tau_d (\mu s) = 145CT (\mu F)$  .  
 $ID = \text{Oscillator discharge current at } 25^\circ\text{C is typically 7.5.}$

For large values of  $B_T$ :  $Td$  ( $\mu$ s)  $\approx 145CT$  ( $\mu$ f).

Oscillator frequency is approximated by the formula

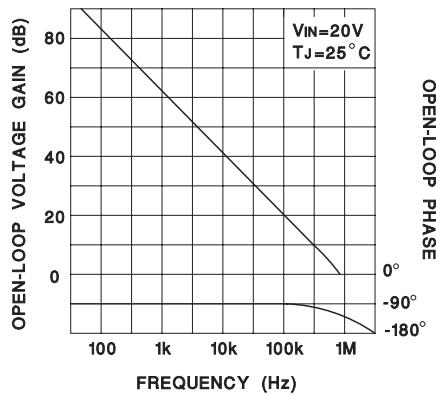
Oscillator frequency is approximated by the formula:  $fT \text{ (kHz)} \approx \frac{1}{RT \text{ (k}\Omega\text{)} \cdot CT \text{ (}\mu\text{f)}}$ .

**Figure 1. Oscillator Circuit**



Error Amplifier can source up to 0.5mA.

## Figure 2. Error Amplifier Output Configuration



**Figure 3. Error Amplifier Gain and Phase vs Frequency**

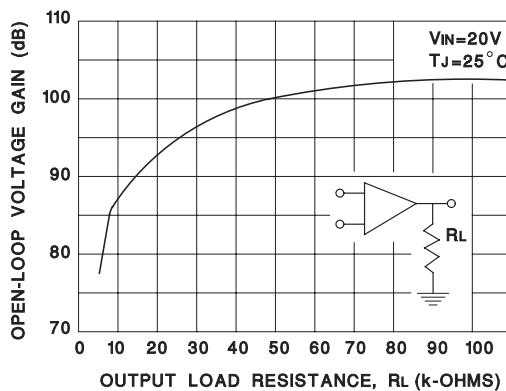
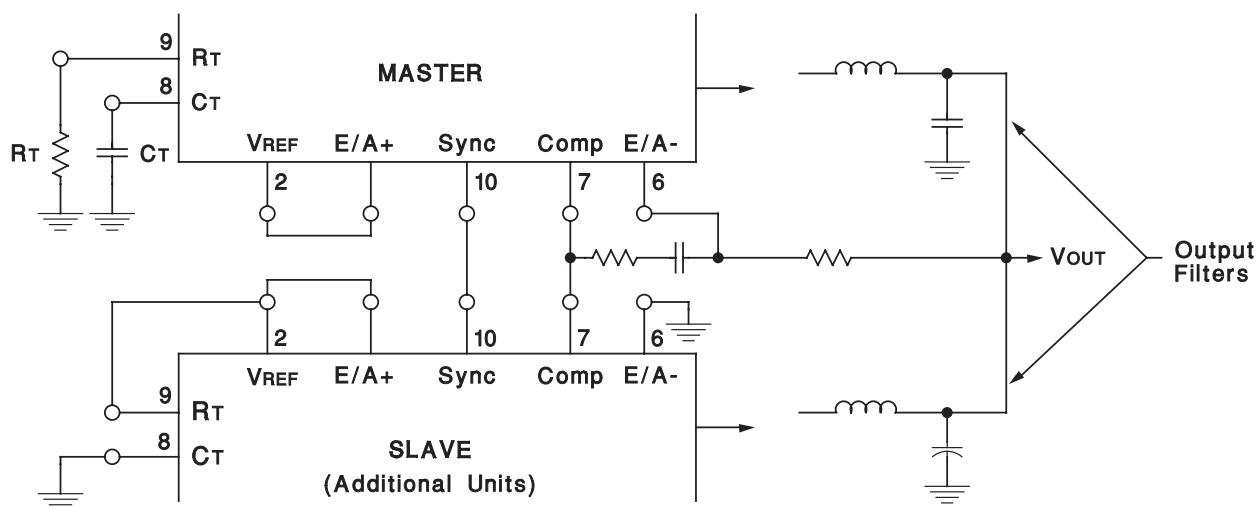
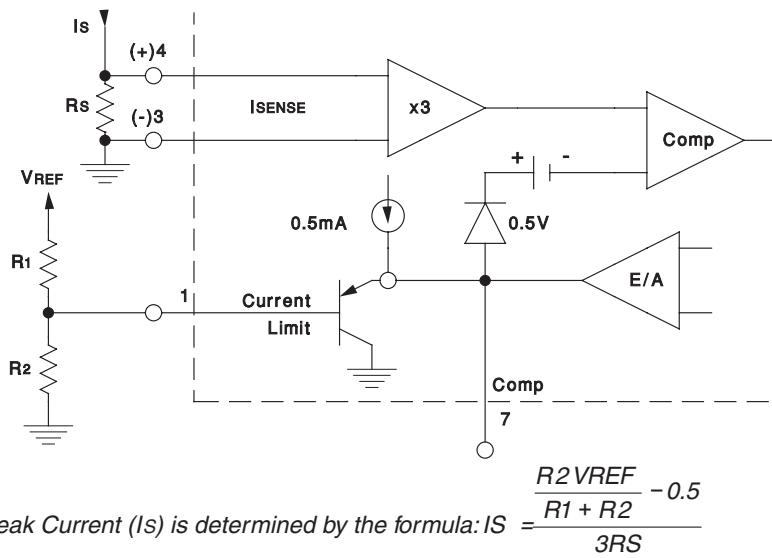


Figure 4. Error Amplifier Open-Logic Gain vs Load Resistance



Slaving allows parallel operation of two or more units with equal current sharing.

Figure 5. Parallel Operation



**Figure 6. Pulse-by-Pulse Current Limiting**

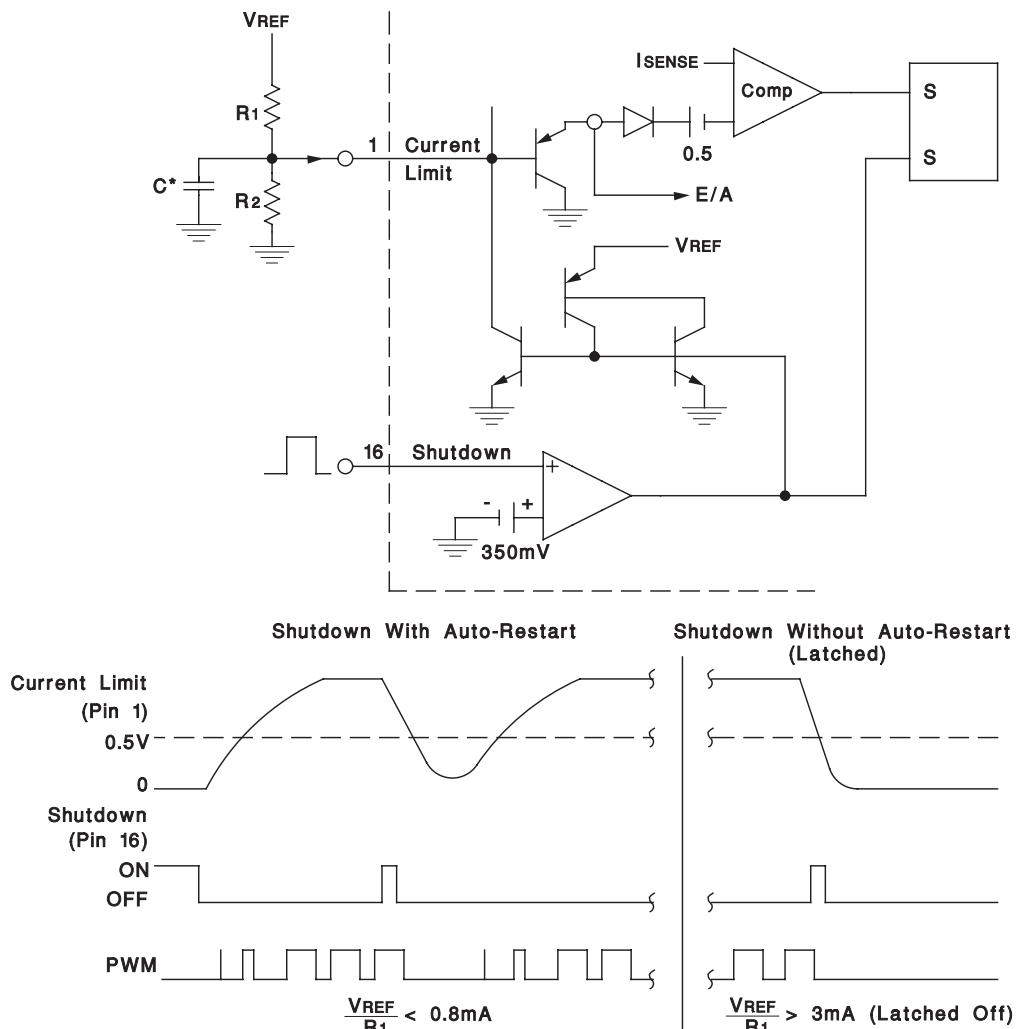
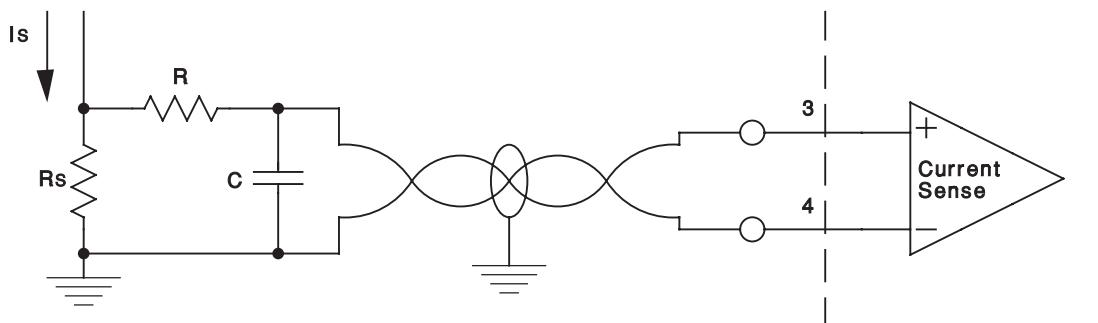
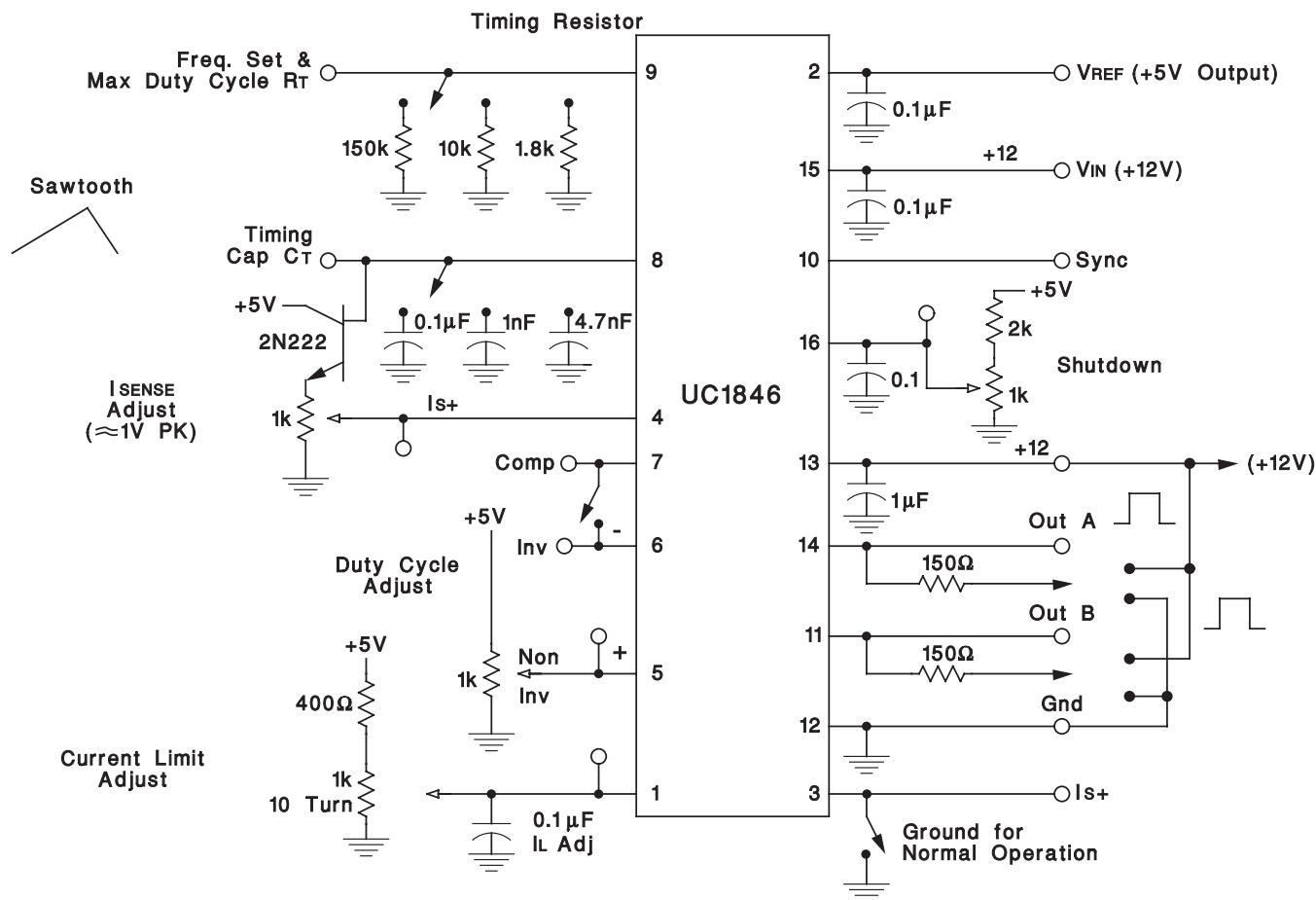


Figure 7. Soft-Start and Shutdown/Restart Functions



A small RC filter may be required in some applications to reduce switch transients.  
Differential input allows remote, noise free sensing.

Figure 8. Current-Sense Amplifier Connection



**Figure 9. Open-Loop Test Circuit**

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-8680601V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8680601VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
5962-8680603V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8680603VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### OTHER QUALIFIED VERSIONS OF UC1846-SP :

- Catalog: [UC1846](#)
- Enhanced Product: [UC1846-EP](#)

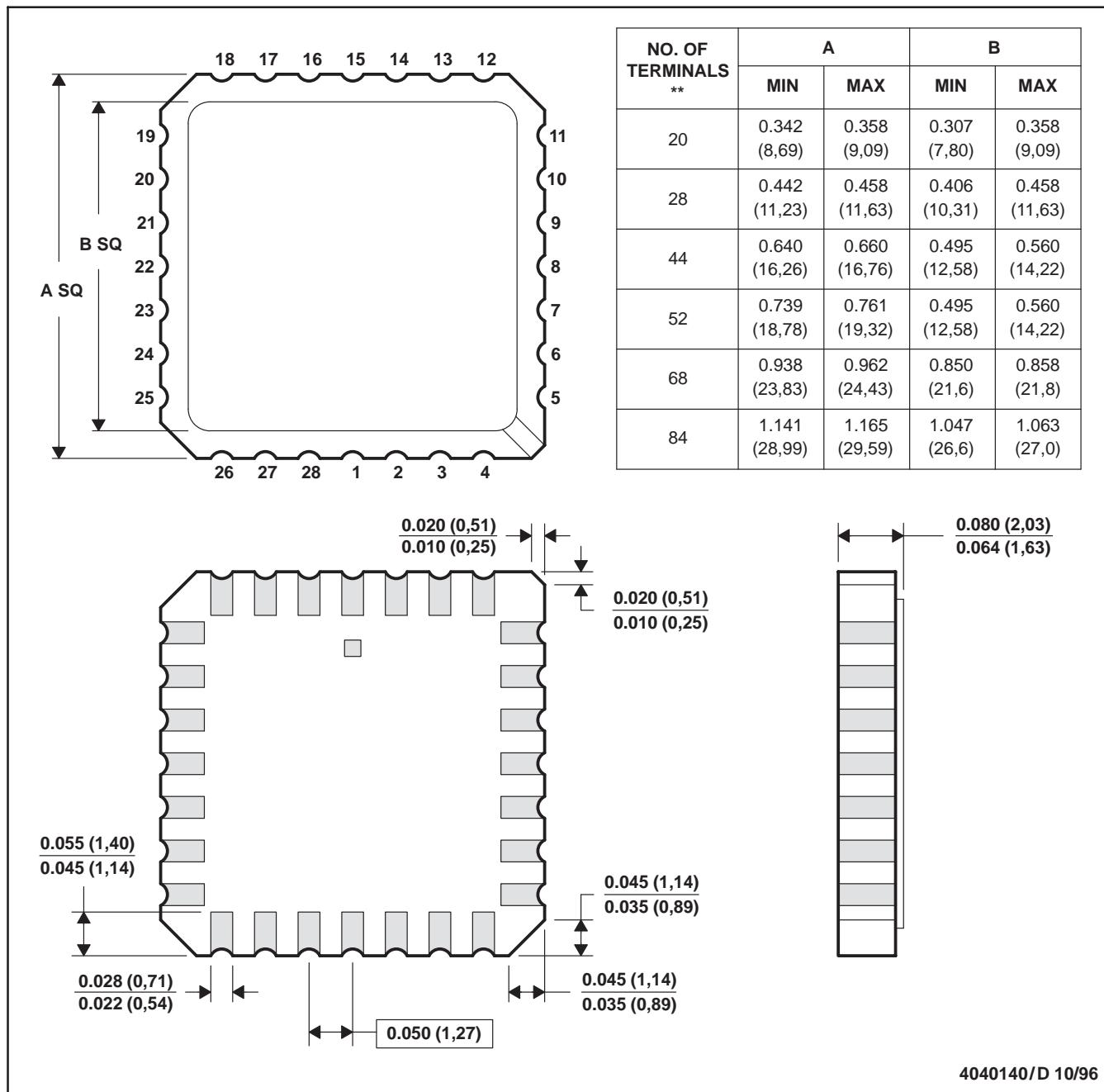
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

## 28 TERMINAL SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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DLP® Products <a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom <a href="http://www.ti.com/communications">www.ti.com/communications</a>
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RF/IF and ZigBee® Solutions <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging <a href="http://www.ti.com/video">www.ti.com/video</a>
	Wireless <a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>