

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PROM VERSION OF M37736MHBXXXGP

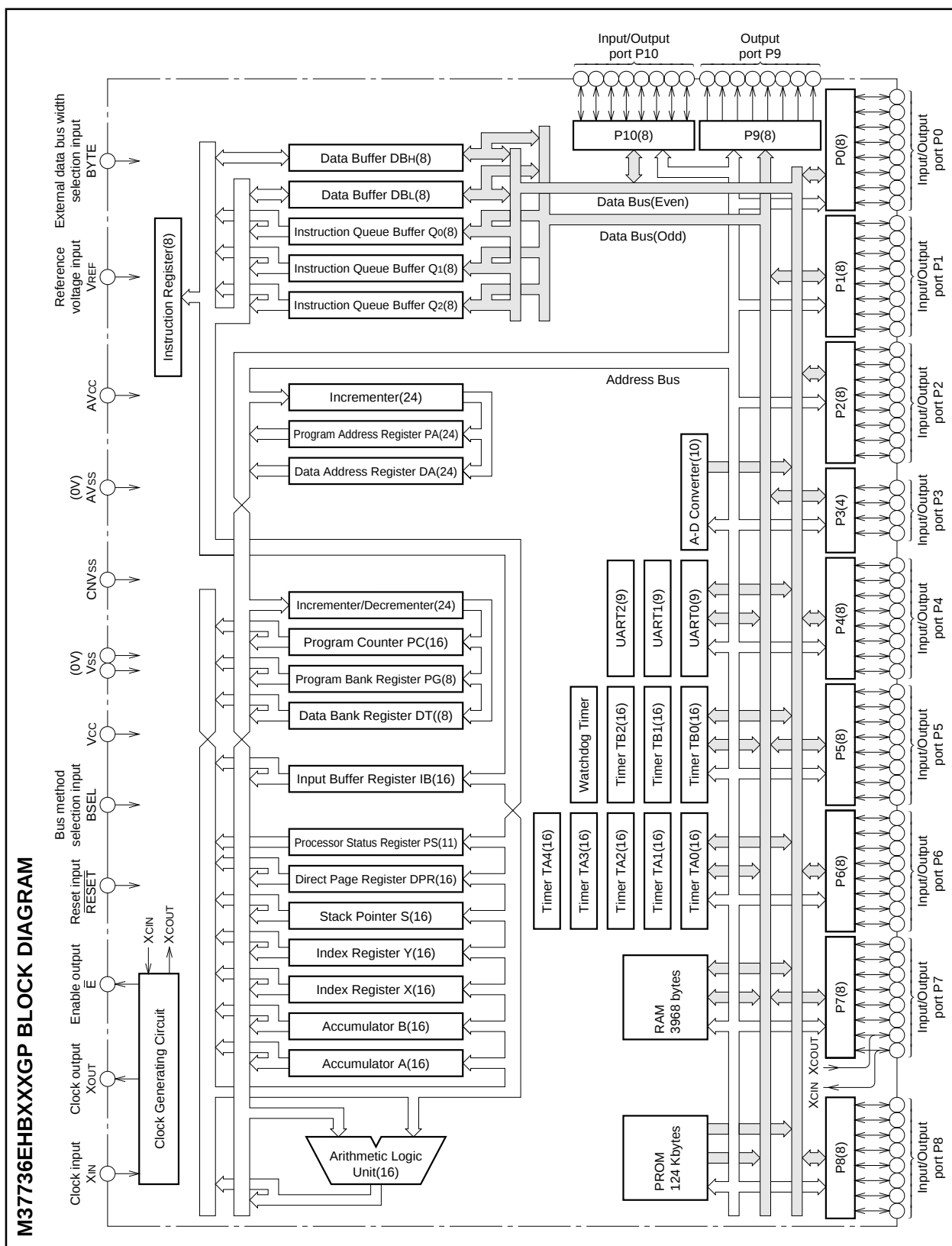
●Number of basic instructions	103
●Memory size	
PROM	124 Kbytes
RAM	3968 bytes
●Instruction execution time	
The fastest instruction at 25 MHz frequency	160 ns

- Note.** Do not use the windowed EPROM version for mass production, because it is a tool for program development (for evaluation).

Outline 100P6S-A

M37736EBHXXXGP M37736EBHGS

PROM VERSION OF M37736MHBXXXGP



FUNCTIONS OF M37736EBXXXXGP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		160 ns (the fastest instruction at external clock 25 MHz frequency)
Memory size	PROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8, P10	8-bit X 9
	P3	4-bit X 1
Output port	P9	8-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		5 V $\pm$ 10%
Power dissipation		47.5 mW (at external clock 25 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		External bus mode A; maximum 16 Mbytes, External bus mode B; maximum 1 Mbytes
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package	M37736EBXXXXGP	100-pin plastic molded QFP (100P6S-A)
	M37736EBBGS	100-pin ceramic LCC (with a window) (100D0)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 5 V $\pm$ 10% to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the external bus mode B and the memory expansion mode or the microprocessor mode, this pin output signal RDE.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
BSEL	Bus method select input	Input	In the memory expansion mode or the microprocessor mode, this pin determines the external bus mode. The bus mode becomes the external bus mode A when "H" signal is input, and the external bus mode B when "L" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P0 ₀ – P0 ₇	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A ₀ – A ₇) at the external bus mode A, and these pins output signals CS ₀ – CS ₄ and RSMP, and addresses (A ₁₆ , A ₁₇) at the external bus mode B.
P1 ₀ – P1 ₇	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D ₈ – D ₁₅) is input/output or an address (A ₈ – A ₁₅) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A ₈ – A ₁₅) is output.
P2 ₀ – P2 ₇	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D ₀ – D ₇) is input/output or an address is output. When using the external bus mode A, the address is A ₁₆ – A ₂₃ . When using the external bus mode B, the address is A ₀ – A ₇ .
P3 ₀ – P3 ₃	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output at the external bus mode A, and WEL, WEH, ALE, and HLDA signals are output at the external bus mode B.
P4 ₀ – P4 ₇	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P4 ₀ , P4 ₁ and P4 ₂ become $\overline{\text{HOLD}}$ and $\overline{\text{RDY}}$ input pins, and a clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P4 ₂ can be selected as an I/O port.
P5 ₀ – P5 ₇	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3.
P6 ₀ – P6 ₇	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input (INT ₀ – INT ₂) and input pins for timers B0 to B2. P6 ₇ also functions as sub-clock ϕ_{SUB} output pin.
P7 ₀ – P7 ₇	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. Additionally, P7 ₆ and P7 ₇ have the function as the output pin (Xc _{OUT}) and the input pin (Xc _{IN}) of the sub-clock (32 kHz) oscillation circuit, respectively. When P7 ₆ and P7 ₇ are used as the Xc _{OUT} and Xc _{IN} pins, connect a resonator or an oscillator between the both.
P8 ₀ – P8 ₇	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.
P9 ₀ – P9 ₇	Output port P9	Output	Port P9 is an 8-bit I/O port. These ports are floating when reset. When writing to the port latch, these ports become the output mode. P9 ₀ – P9 ₃ also function as I/O port for UART 2.
P10 ₀ – P10 ₇	I/O port P10	I/O	In addition to having the same functions as port P0 in the single-chip mode, P10 ₄ – P10 ₇ also function as input pins for key input interrupt input (KI ₀ – KI ₃).
EVL0, EVL1	—	Output	These pins should be left open.

BASIC FUNCTION BLOCKS

The M37736EBXXXGP has the same function as the M37736MHBXXXGP except that the built-in ROM is PROM. Refer to the section on the M37736MHBXXXGP.

PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
VCC, VSS	Power supply		Supply 5V±10% to VCC and 0V to VSS.
CNVSS	VPP input	Input	Connect to VPP when programming or verifying.
BYTE	VPP input	Input	Connect to VPP when programming or verifying.
RESET	Reset input	Input	Connect to VSS.
XIN	Clock input	Input	Connect a ceramic resonator between XIN and XOUT.
XOUT	Clock output	Output	
$\bar{E}$	Enable output	Output	Keep open.
AVCC, AVSS	Analog supply input		Connect AVCC to VCC and AVSS to VSS.
VREF	Reference voltage input	Input	Connect to VSS.
P00 – P07	Address input (A0 – A7)	Input	Port P0 functions as the lower 8 bits address input (A0 – A7).
P10 – P17	Address input (A8 – A15)	Input	Port P1 functions as the higher 8 bits address input (A8 – A15).
P20 – P27	Data I/O (D0 – D7)	I/O	Port P2 functions as the 8 bits data input/output (D0 – D7).
P30	Address input (A16)	Input	P30 functions as the most significant bit address input (A16).
P31 – P33	Input port P3	Input	Connect to VSS.
P40 – P47	Input port P4	Input	Connect to VSS.
P50 – P57	Control signal input	Input	P50, P51, and P52 function as PGM, OE, and CE input pins respectively. Connect P53, P54, P55, and P56 to VCC. Connect P57 to VSS.
P60 – P67	Input port P6	Input	Connect to VSS.
P70 – P77	Input port P7	Input	Connect to VSS.
P80 – P87	Input port P8	Input	Connect to VSS.
P90 – P97	Input port P9	Input	Connect to VSS.
P100 – P107	Input port P10	Input	Connect to VSS.
BSEL	_____	Input	Connect to VCC.
EVL0, EVL1	_____	Output	Keep open.

M37736EBBXXXGP M37736EBBGS

PROM VERSION OF M37736MHBXXXGP

EPROM MODE

The M37736EBBXXXGP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, P30, P50, P51, P52, CNVss, and BYTE are used for the EPROM (equivalent to the M5M27C101K).

When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 0100016 – 1FFFF16.

Connect the clock which is either ceramic resonator or external clock to XIN pin and XOUT pin.

Table 1 Pin function in EPROM mode

	M37736EBBXXXGP	M5M27C101K
VCC	VCC	VCC
VPP	CNVss, BYTE	VPP
VSS	VSS	VSS
Address input	Ports P0, P1, P30	A0 – A16
Data I/O	Port P2	D0 – D7
$\overline{CE}$	P52	$\overline{CE}$
$\overline{OE}$	P51	$\overline{OE}$
PGM	P50	PGM

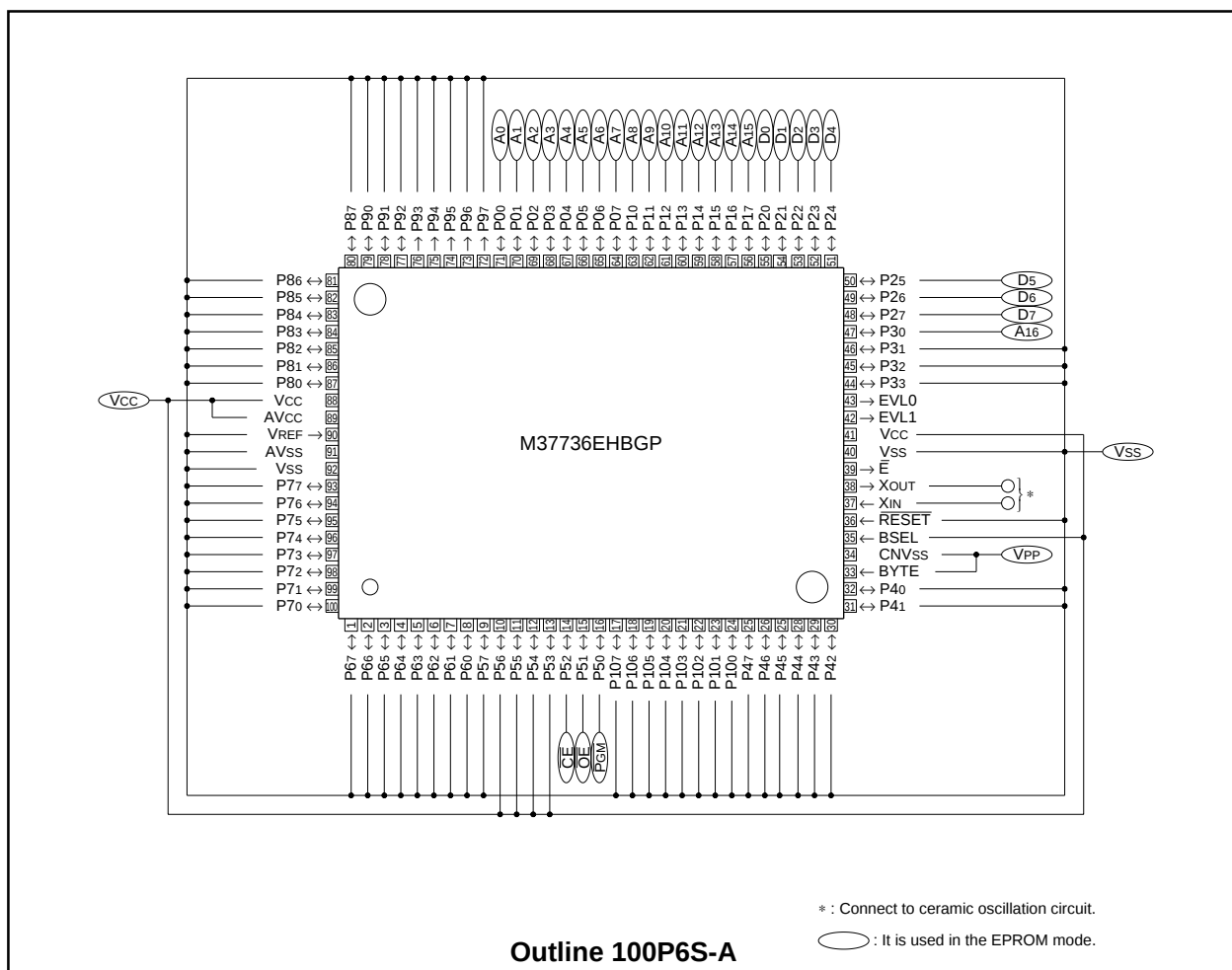


Fig. 1 Pin connection in EPROM mode

FUNCTION IN EPROM MODE

1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins to a "L" level. Input the address of the data ($A_0 - A_{16}$) to be read, and the data will be output to the I/O pins $D_0 - D_7$. The data I/O pins will be floating when either the $\overline{\text{CE}}$ or $\overline{\text{OE}}$ pins are in the "H" state.

Programming

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the $\overline{\text{CE}}$ pin to a "L" level and the $\overline{\text{OE}}$ pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the V_{PP} pin. The address to be programmed to is selected with pins $A_0 - A_{16}$, and the data to be programmed is input to pins $D_0 - D_7$. Set the $\overline{\text{PGM}}$ pin to a "L" level to being programming.

Erasing

To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15 J/cm².

Programming operation

To program the M37733EBXXXXFP, first set $V_{CC} = 6 \text{ V}$, $V_{PP} = 12.5 \text{ V}$, and set the address to 01000₁₆. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses ($0.2 \times X \text{ ms}$).

When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been programmed, read with $V_{CC} = V_{PP} = 5 \text{ V}$ (or $V_{CC} = V_{PP} = 5.5 \text{ V}$).

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	V_{PP}	V_{CC}	Data I/O
Read-out	V _{IL}	V _{IL}	X	5 V	5 V	Output
Output	V _{IL}	V _{IH}	X	5 V	5 V	Floating
Disable	V _{IH}	X	X	5 V	5 V	Floating
Programming	V _{IL}	V _{IH}	V _{IL}	12.5 V	6 V	Input
Programming Verify	V _{IL}	V _{IL}	V _{IH}	12.5 V	6 V	Output
Program Disable	V _{IH}	V _{IH}	V _{IH}	12.5 V	6 V	Floating

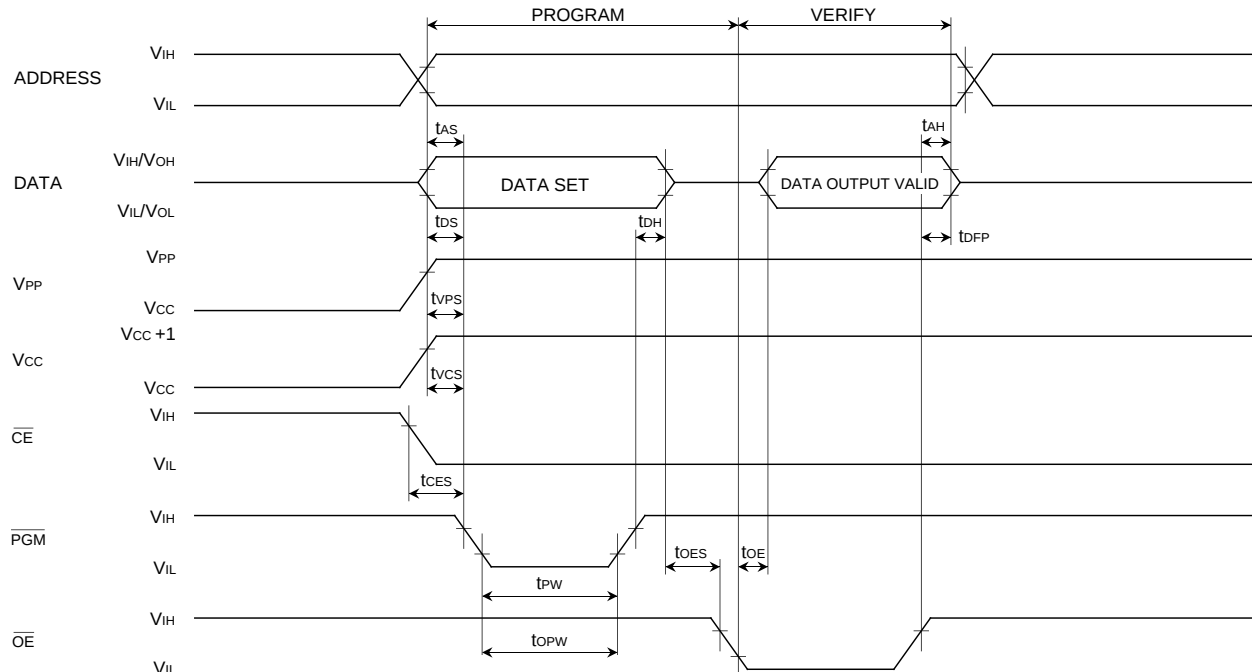
Note 1 : An X indicates either V_{IL} or V_{IH}.

Programming operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5 \text{ }^\circ\text{C}$, $V_{CC} = 6 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \pm 0.3 \text{ V}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{AS}	Address setup time		2			μs
t _{OES}	$\overline{\text{OE}}$ setup time		2			μs
t _{DS}	Data setup time		2			μs
t _{AH}	Address hold time		0			μs
t _{DH}	Data hold time		2			μs
t _{DFP}	Output enable to output float delay		0		130	ns
t _{VCS}	V_{CC} setup time		2			μs
t _{VPS}	V_{PP} setup time		2			μs
t _{PW}	PGM pulse width		0.19	0.2	0.21	ms
t _{OPW}	PGM over program pulse width		0.19		5.25	ms
t _{CES}	$\overline{\text{CE}}$ setup time		2			μs
t _{OE}	Data valid from $\overline{\text{OE}}$				150	ns

AC waveforms



Test conditions for A.C. characteristics

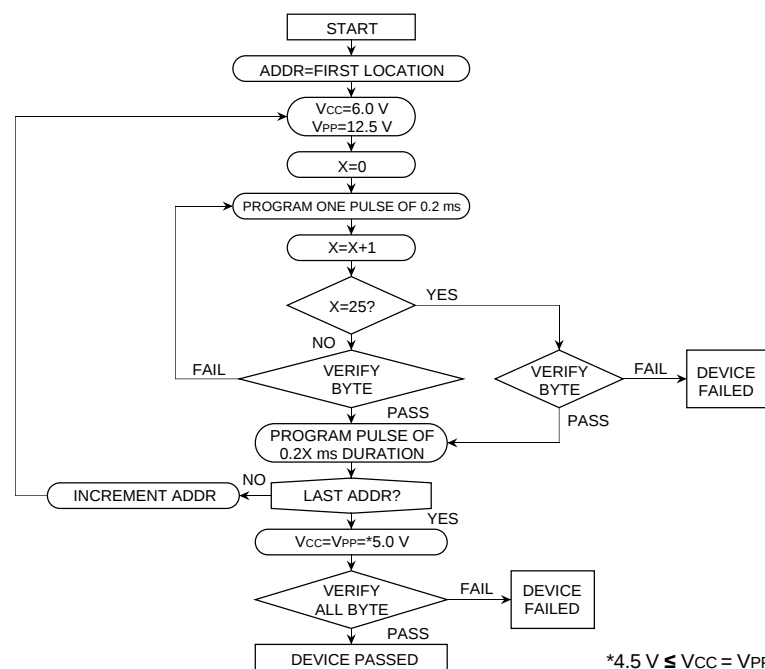
Input voltage : $V_{IL} = 0.45 \text{ V}$, $V_{IH} = 2.4 \text{ V}$

Input rise and fall times (10 % – 90 %) : $\leq 20 \text{ ns}$

Reference voltage at timing measurement : Input, Output

"L" = 0.8 V, "H" = 2 V

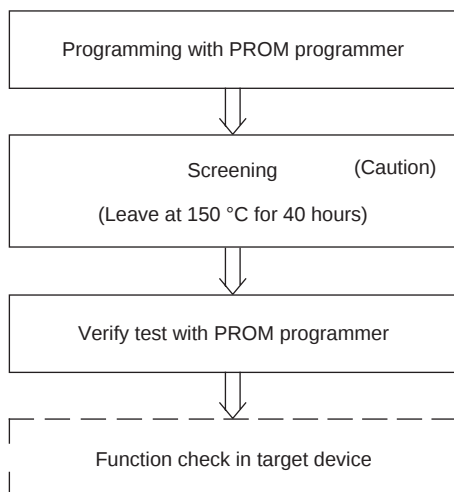
Programming algorithm flow chart



*4.5 V $\leq V_{CC} = V_{PP} \leq 5.5 \text{ V}$

SAFETY INSTRUCTIONS

- (1) Sunlight and fluorescent lamp contain light that can erase written information. When using in read mode, be sure to cover the transparent glass portion with a seal or other materials (ceramic package product).
- (2) Mitsubishi Electric corp. provides the seal for covering the transparent glass. Take care that the seal does not touch the read pins (ceramic package product).
- (3) Clean the transparent glass before erasing. Fingers' fat and paste disturb the passage of ultraviolet rays and may affect badly the erasure capability (ceramic package product).
- (4) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
- (5) The programmable M37736EBBGP that is shipped in blank is also provided. For the M37736EBBGP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.



Caution : Never expose to 150 °C exceeding 100 hours.

ADDRESSING MODES

The M37736EBXXXXGP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

MACHINE INSTRUCTION LIST

The M37736EBXXXXGP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.

- (1) M37736EBXXXXGP writing to PROM order confirmation form
- (2) 100P6S mark specification form
- (3) ROM data (EPROM 3 sets)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		−0.3 to +7	V
AV _{cc}	Analog power source voltage		−0.3 to +7	V
V _i	Input voltage RESET, CNVss, BYTE		−0.3 to +12(Note)	V
V _i	Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, VREF, X _{IN} , BSEL		−0.3 to V _{cc} + 0.3	V
V _o	Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107, X _{OUT} , E		−0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	300	mW
T _{opr}	Operating temperature		−20 to +85	°C
T _{stg}	Storage temperature		−40 to +150	°C

Note. When the EPROM is programmed, input voltage of pins CNVss and BYTE is 13 V respectively.

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 5 V ± 10%, T_a = −20 to +85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{cc}	Power source voltage	f(X _{IN}) : Operating f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz	4.5 2.7	5.0 5.5	V
AV _{cc}	Analog power source voltage		V _{cc}		V
V _{ss}	Power source voltage		0		V
AV _{ss}	Analog power source voltage		0		V
V _{IH}	High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X _{IN} , RESET, CNVss, BYTE, BSEL, X _{CIN} (Note 3)	0.8 V _{cc}		V _{cc}	V
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0.8 V _{cc}		V _{cc}	V
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0.5 V _{cc}		V _{cc}	V
V _{IL}	Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X _{IN} , RESET, CNVss, BYTE, BSEL, X _{CIN} (Note 3)	0		0.2V _{cc}	V
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0		0.2V _{cc}	V
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0		0.16V _{cc}	V
I _{OH(peak)}	High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107			−10	mA
I _{OH(avg)}	High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107			−5	mA
I _{OL(peak)}	Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107			10	mA
I _{OL(peak)}	Low-level peak output current P44 – P47, P100 – P103			20	mA
I _{OL(avg)}	Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107			5	mA
I _{OL(avg)}	Low-level average output current P44 – P47, P100 – P103			15	mA
f(X _{IN})	Main-clock oscillation frequency (Note 4)			25	MHz
f(X _{CIN})	Sub-clock oscillation frequency		32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

- The sum of I_{OL(peak)} for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, P7, and P10 must be 100 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, P7, and P10 must be 80 mA or less.
- Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".
- The maximum value of f(X_{IN}) = 12.5 MHz when the main clock division selection bit = "1".

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107	$I_{OH} = -10\text{ mA}$	3			V
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OH} = -400\text{ }\mu\text{A}$	4.7			V
V_{OH}	High-level output voltage P30 – P32	$I_{OH} = -10\text{ mA}$ $I_{CH} = -400\text{ }\mu\text{A}$	3.1 4.8			V
V_{OH}	High-level output voltage $\overline{E}$	$I_{OH} = -10\text{ mA}$ $I_{OH} = -400\text{ }\mu\text{A}$	3.4 4.8			V
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107	$I_{OL} = 10\text{ mA}$			2	V
V_{OL}	Low-level output voltage P44 – P47, P100 – P103	$I_{OL} = 20\text{ mA}$			2	V
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OL} = 2\text{ mA}$			0.45	V
V_{OL}	Low-level output voltage P30 – P32	$I_{OL} = 10\text{ mA}$ $I_{OL} = 2\text{ mA}$			1.9 0.43	V
V_{OL}	Low-level output voltage $\overline{E}$	$I_{OL} = 10\text{ mA}$ $I_{OL} = 2\text{ mA}$			1.6 0.4	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $\overline{TA0IN} - \overline{TA4IN}$, $\overline{TB0IN} - \overline{TB2IN}$, $\overline{INT0} - \overline{INT2}$, $\overline{ADTRG}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS2}$, $\overline{CLK0}$, $\overline{CLK1}$, $\overline{CLK2}$, $\overline{KI0} - \overline{KI3}$		0.4		1	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$		0.2		0.5	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}		0.1		0.4	V
$V_{T+} - V_{T-}$	Hysteresis X_{CIN} (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X_{IN} , $\overline{RESET}$, $\overline{CNVss}$, $\overline{BYTE}$, $\overline{BSEL}$	$V_I = 5\text{ V}$			5	μA
I_{IL}	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60, P61, P65 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P103, X_{IN} , $\overline{RESET}$, $\overline{CNVss}$, $\overline{BYTE}$, $\overline{BSEL}$	$V_I = 0\text{ V}$			-5	μA
I_{IL}	Low-level input current P104 – P107, P62 – P64	$V_I = 0\text{ V}$, without a pull-up transistor $V_I = 0\text{ V}$, with a pull-up transistor			-5	μA
			-0.25	-0.5	-1.0	mA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC}	Power source current	In single-chip mode, output pins are open, and other pins are V _{SS} . $V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), $f(f_2) = 12.5\text{ MHz}$, $f(X_{CIN}) = 32.768\text{ kHz}$, in operating (Note 1)		9.5	19	mA
		$V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), $f(f_2) = 1.5625\text{ MHz}$, $f(X_{CIN}) = \text{Stopped}$, in operating (Note 1)		1.3	2.6	mA
		$V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), $f(X_{CIN}) = 32.768\text{ kHz}$, when a WIT instruction is executed (Note 2)		10	20	μA
		$V_{CC} = 5\text{ V}$, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, in operating (Note 3)		50	100	μA
		$V_{CC} = 5\text{ V}$, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, when a WIT instruction is executed (Note 4)		5	10	μA
		$T_a = 25\text{ }^{\circ}\text{C}$, when clock is stopped			1	μA
		$T_a = 85\text{ }^{\circ}\text{C}$, when clock is stopped			20	μA

Notes 1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".

2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".

3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4. This applies when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
—	Absolute accuracy	$V_{REF} = V_{CC}$			± 3	LSB
R _{LADDER}	Ladder resistance	$V_{REF} = V_{CC}$	10		25	k Ω
t _{CONV}	Conversion time		9.44			μs
V _{REF}	Reference voltage		2		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

TIMING REQUIREMENTS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted (Note))

Notes 1. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 3)	40		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 4)	15		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 4)	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns

Notes 3. When the main clock division selection bit = "1", the minimum value of $t_c = 80\text{ ns}$.

4. When the main clock division selection bit = "1", values of $t_{w(H)} / t_c$ and $t_{w(L)} / t_c$ must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(P0D-E)$	Port P0 input setup time	60		ns
$t_{su}(P1D-E)$	Port P1 input setup time	60		ns
$t_{su}(P2D-E)$	Port P2 input setup time	60		ns
$t_{su}(P3D-E)$	Port P3 input setup time	60		ns
$t_{su}(P4D-E)$	Port P4 input setup time	60		ns
$t_{su}(P5D-E)$	Port P5 input setup time	60		ns
$t_{su}(P6D-E)$	Port P6 input setup time	60		ns
$t_{su}(P7D-E)$	Port P7 input setup time	60		ns
$t_{su}(P8D-E)$	Port P8 input setup time	60		ns
$t_{su}(P10D-E)$	Port P10 input setup time	60		ns
$t_h(E-P0D)$	Port P0 input hold time	0		ns
$t_h(E-P1D)$	Port P1 input hold time	0		ns
$t_h(E-P2D)$	Port P2 input hold time	0		ns
$t_h(E-P3D)$	Port P3 input hold time	0		ns
$t_h(E-P4D)$	Port P4 input hold time	0		ns
$t_h(E-P5D)$	Port P5 input hold time	0		ns
$t_h(E-P6D)$	Port P6 input hold time	0		ns
$t_h(E-P7D)$	Port P7 input hold time	0		ns
$t_h(E-P8D)$	Port P8 input hold time	0		ns
$t_h(E-P10D)$	Port P10 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su}(D-E)$	Data input setup time (external bus mode A)	32		ns
$t_{su}(D-RDE)$	Data input setup time (external bus mode B)	32		ns
$t_{su}(RDY-\phi 1)$	RDY input setup time	55		ns
$t_{su}(HOLD-\phi 1)$	HOLD input setup time	55		ns
$t_h(E-D)$	Data input hold time (external bus mode A)	0		ns
$t_h(RDE-D)$	Data input hold time (external bus mode B)	0		ns
$t_h(\phi 1-RDY)$	RDY input hold time	0		ns
$t_h(\phi 1-HOLD)$	HOLD input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN input cycle time	80		ns
$t_{w(TAH)}$	TAiN input high-level pulse width	40		ns
$t_{w(TAL)}$	TAiN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN input cycle time (Note)	320		ns
$t_{w(TAH)}$	TAiN input high-level pulse width (Note)	160		ns
$t_{w(TAL)}$	TAiN input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in one-shot pulse mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiN input cycle time (Note)	320		ns
$t_{w(TAH)}$	TAiN input high-level pulse width	80		ns
$t_{w(TAL)}$	TAiN input low-level pulse width	80		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in pulse width modulation mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiN input high-level pulse width	80		ns
$t_{w(TAL)}$	TAiN input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high-level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low-level pulse width	1000		ns
$t_{su(UP-T_{IN})}$	TAiOUT input setup time	400		ns
$t_h(T_{IN-UP})$	TAiOUT input hold time	400		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAj input cycle time	800		ns
$t_{su(TA_{jIN}-TA_{jOUT})}$	TAjIN input setup time	200		ns
$t_{su(TA_{jOUT}-TA_{jIN})}$	TAjOUT input setup time	200		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TBiN input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TBiN input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TBiN input cycle time (both edges count)	160		ns
$t_{w(TBH)}$	TBiN input high-level pulse width (both edges count)	80		ns
$t_{w(TBL)}$	TBiN input low-level pulse width (both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time (Note)	320		ns
$t_{w(TBH)}$	TBiN input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TBiN input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time (Note)	320		ns
$t_{w(TBH)}$	TBiN input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TBiN input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG input cycle time (minimum allowable trigger)	1000		ns
$t_{w(ADL)}$	ADTRG input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK _i input cycle time	200		ns
$t_{w(CKH)}$	CLK _i input high-level pulse width	100		ns
$t_{w(CKL)}$	CLK _i input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxD _i output delay time		80	ns
$t_{h(C-Q)}$	TxD _i hold time	0		ns
$t_{su(D-C)}$	RxD _i input setup time	30		ns
$t_{h(C-D)}$	RxD _i input hold time	90		ns

External interrupt $\overline{INT}_i$ input, key input interrupt $\overline{KI}_i$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT}_i$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT}_i$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI}_i$ input low-level pulse width	250		ns

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TA _{in} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TA _{in} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TA _{in} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TA _{in} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TB _{in} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TB _{in} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TB _{in} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet " M37736MBBXXXGP ".

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_d(E-P0Q)$	Port P0 data output delay time	Fig. 2		80	ns
$t_d(E-P1Q)$	Port P1 data output delay time			80	ns
$t_d(E-P2Q)$	Port P2 data output delay time			80	ns
$t_d(E-P3Q)$	Port P3 data output delay time			80	ns
$t_d(E-P4Q)$	Port P4 data output delay time			80	ns
$t_d(E-P5Q)$	Port P5 data output delay time			80	ns
$t_d(E-P6Q)$	Port P6 data output delay time			80	ns
$t_d(E-P7Q)$	Port P7 data output delay time			80	ns
$t_d(E-P8Q)$	Port P8 data output delay time			80	ns
$t_d(E-P9Q)$	Port P9 data output delay time			80	ns
$t_d(E-P10Q)$	Port P10 data output delay time			80	ns

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

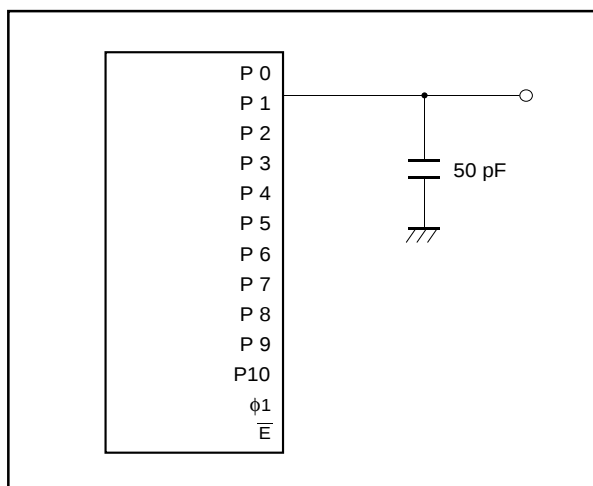


Fig. 2 Measuring circuit for ports P0 – P10 and ϕ_1

[External bus mode A]

Memory expansion mode and microprocessor mode

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 25 °C, f(XIN) = 25 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
td(A _n -E)	Address output delay time	No wait Wait 1 Wait 0	Fig. 2	12		ns
				87		ns
td(A-E)	Address output delay time	No wait Wait 1 Wait 0		12		ns
				75		ns
th(E-A _n)	Address hold time			18		ns
tw(ALE)	ALE pulse width	No wait Wait 1 Wait 0		22		ns
				57		ns
tsu(A-ALE)	Address output setup time	No wait Wait 1 Wait 0		5		ns
				45		ns
th(ALE-A)	Address hold time	No wait Wait 1 Wait 0		9		ns
				15		ns
td(ALE-E)	ALE output delay time	No wait Wait 1 Wait 0		4		ns
				10		ns
td(E-DQ)	Data output delay time				45	ns
th(E-DQ)	Data hold delay time			18		ns
tw(EL)	E pulse width	No wait Wait 1 Wait 0		50		ns
				130		ns
tpxz(E-DZ)	Floating start delay time				5	ns
tpzx(E-DZ)	Floating release delay time			20		ns
td(BHE-E)	BHE output delay time	No wait Wait 1 Wait 0		12		ns
				87		ns
td(R/W-E)	R/W output delay time	No wait Wait 1 Wait 0		12		ns
				87		ns
th(E-BHE)	BHE hold time			18		ns
th(E-R/W)	R/W hold time			18		ns
td(E-φ ₁)	φ ₁ output delay time			0	18	ns
td(φ ₁ -HLDA)	HLDA output delay time				50	ns

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

[External bus mode A]

Memory expansion mode and microprocessor mode

Bus timing data formulas ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(XIN) = 25\text{ MHz}$ (Max., Note), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
$t_{d(An-E)}$	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{d(A-E)}$	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$		ns
$t_{h(E-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{w(ALE)}$	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$		ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{h(ALE-A)}$	Address hold time	No wait	9		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$		ns
$t_{d(ALE-E)}$	ALE output delay time	No wait	4		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{d(E-DQ)}$	Data output delay time			45	ns
$t_{h(E-DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{w(EL)}$	$\overline{E}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{pxz(E-DZ)}$	Floating start delay time			5	ns
$t_{pzx(E-DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{d(R/W-E)}$	$R/\overline{W}$ output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{h(E-R/W)}$	$R/\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{d(E-\phi 1)}$	$\phi 1$ output delay time		0	18	ns

Notes 1. This applies when the main-clock division selection bit = "0".

2. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXGP".

[External bus mode B]

Memory expansion mode and microprocessor mode

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = -20 to 85 °C, f(XIN) = 25 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
t _d (CS-WE) t _d (CS-RDE)	Chip-select output delay time	No wait	Fig.2	12		ns
		Wait 1		87		ns
		Wait 0				
t _h (WE-CS) t _h (RDE-CS)	Chip-select hold time	No wait		4		ns
		Wait 1				
		Wait 0				
t _d (A _n -WE) t _d (A _n -RDE)	Address output delay time	No wait		12		ns
		Wait 1		87		ns
		Wait 0				
t _d (A-WE) t _d (A-RDE)	Address output delay time	No wait		12		ns
		Wait 1		75		ns
		Wait 0				
t _h (WE-A _n) t _h (RDE-A _n)	Address hold time	No wait		18		ns
		Wait 1				
		Wait 0				
t _w (ALE)	ALE pulse width	No wait		22		ns
		Wait 1		57		ns
		Wait 0				
t _{su} (A-ALE)	Address output setup time	No wait		5		ns
		Wait 1		45		ns
		Wait 0				
t _h (ALE-A)	Address hold time	No wait		9		ns
		Wait 1		15		ns
		Wait 0				
t _d (ALE-WE) t _d (ALE-RDE)	ALE output delay time	No wait		4		ns
		Wait 1		10		ns
		Wait 0				
t _d (WE-DQ)	Data output delay time	No wait			45	ns
		Wait 1		18		ns
		Wait 0		50		ns
t _w (WE)	WE pulse width	No wait		130		ns
		Wait 1				
		Wait 0				
t _{pxz} (RDE-DZ)	Floating start delay time	No wait			5	ns
		Wait 1		20		ns
		Wait 0		48		ns
t _w (RDE)	RDE pulse width	No wait		128		ns
		Wait 1				
		Wait 0				
t _d (RSMP-WE) t _d (RSMP-RDE)	RSMP output delay time	No wait		10		ns
		Wait 1		0		ns
		Wait 0				
t _h (φ ₁ -RSMP)	RSMP hold time	No wait		0		ns
		Wait 1		0	18	ns
		Wait 0				
t _d (WE-φ ₁) t _d (RDE-φ ₁)	φ ₁ output delay time	No wait			50	ns
		Wait 1				
		Wait 0				
t _d (φ ₁ -HLDA)	HLDA output delay time	No wait				
		Wait 1				
		Wait 0				

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

[External bus mode B]

Memory expansion mode and microprocessor mode

Bus timing data formulas ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Max., Note1), unless otherwise noted)

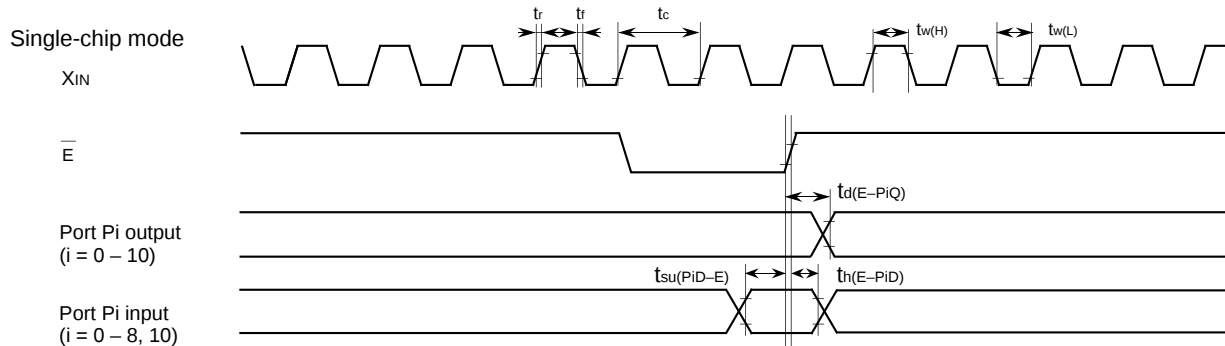
Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time		4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1	9		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$		ns
$t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$	ALE output delay time	No wait Wait 1	4		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{d(WE-DQ)}$	Data output delay time			45	ns
$t_{h(WE-DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_{w(WE)}$	$\overline{WEL}/\overline{WEH}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time			5	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		ns
$t_{w(RDE)}$	RDE pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 32$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 32$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$	RSMP output delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{h(\phi_1-RSMP)}$	RSMP hold time		0		ns
$t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$	ϕ_1 output delay time		0	18	ns

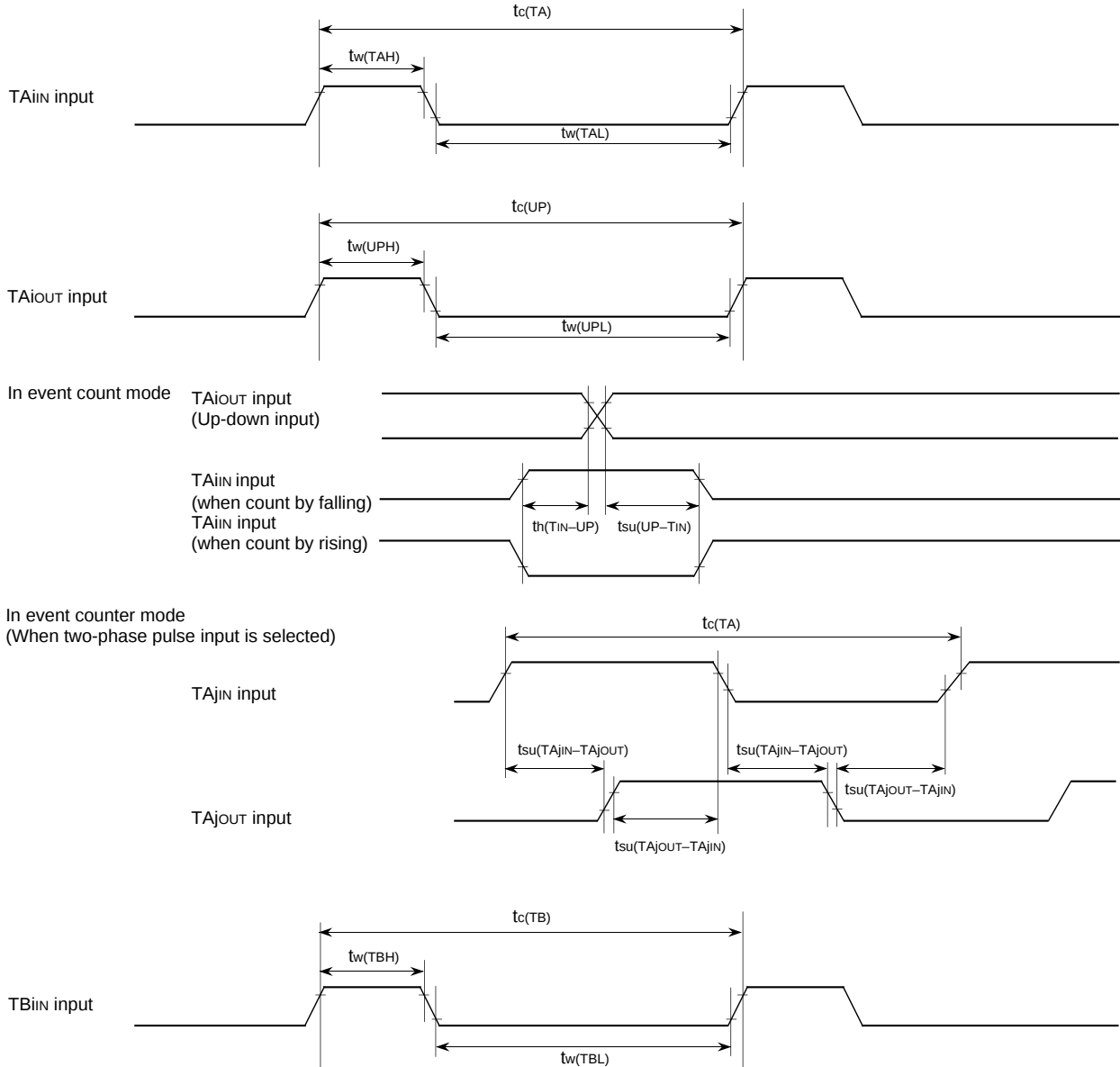
Notes 1. This applies when the main-clock division selection bit = "0".

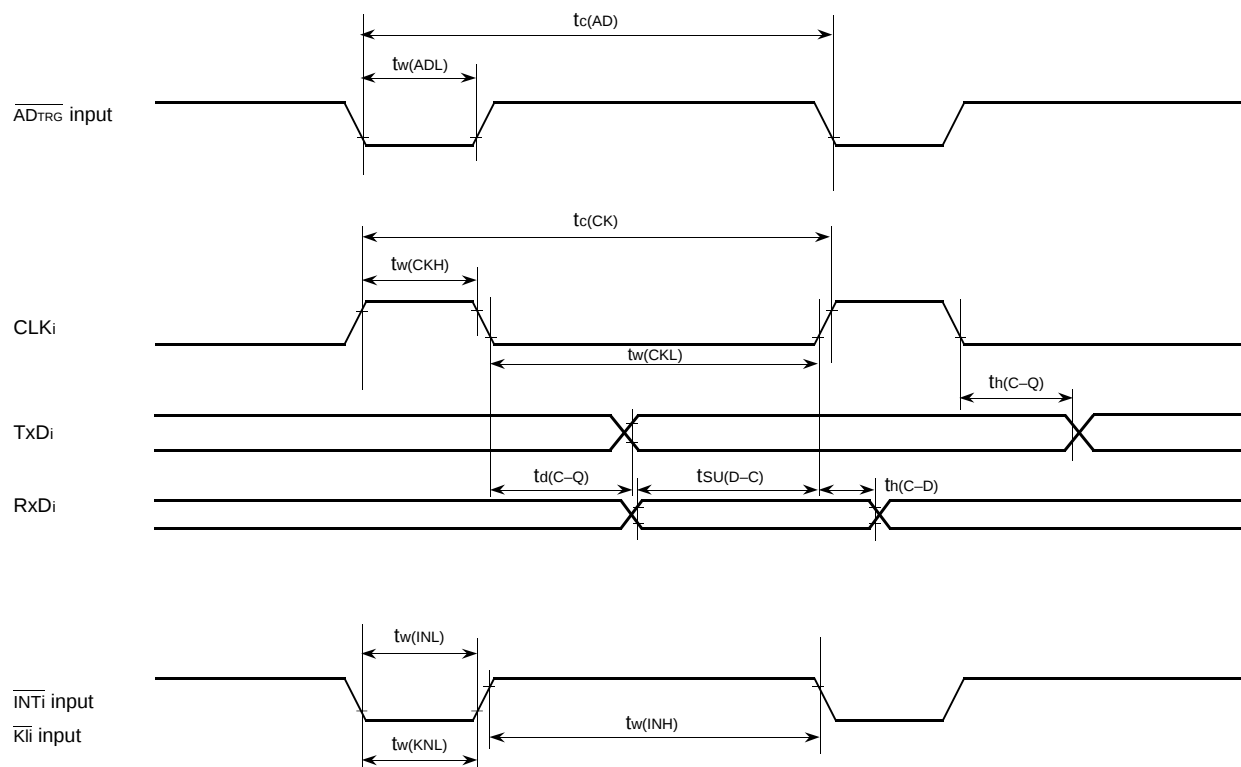
2. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet " M37736MHBXXXXGP ".

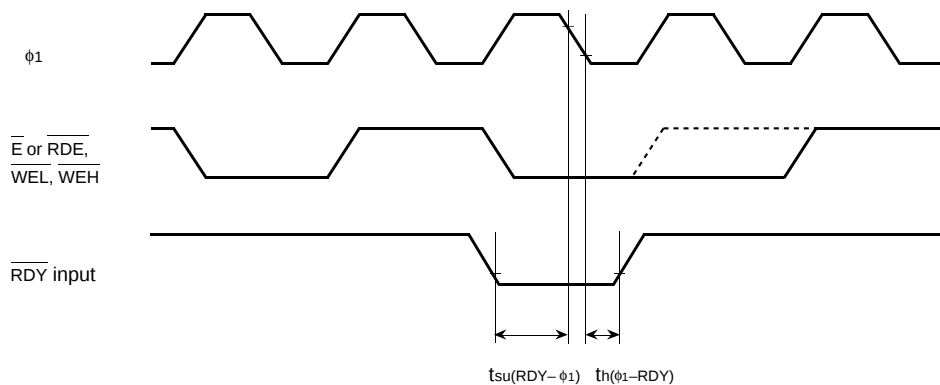
TIMING DIAGRAM



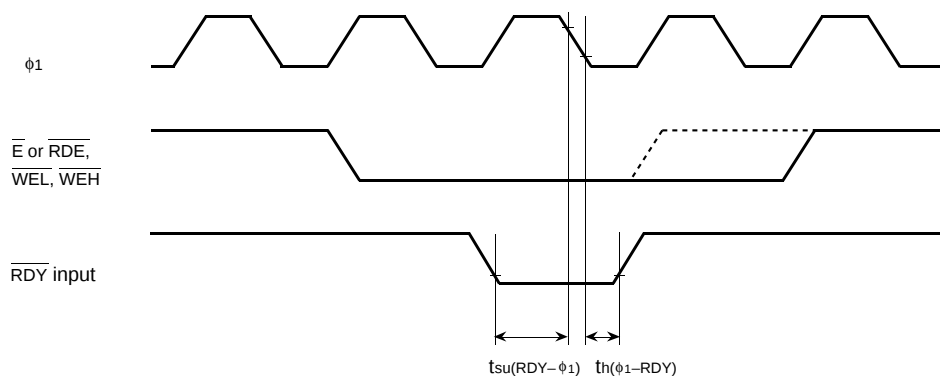




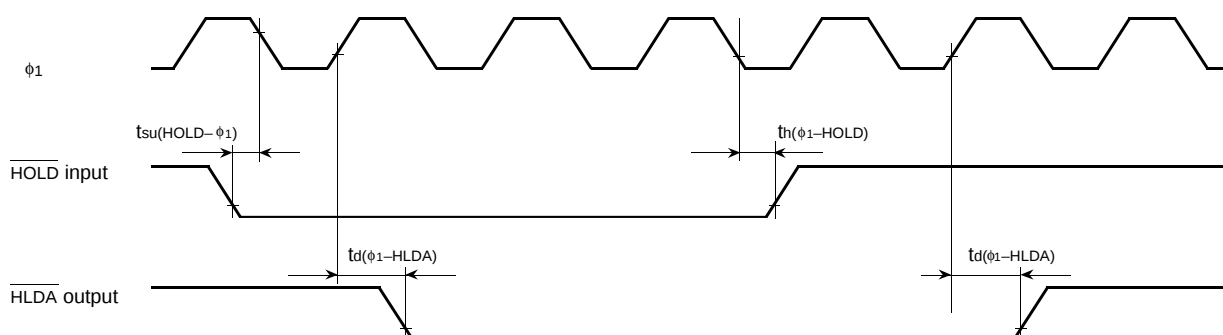
Memory expansion mode and microprocessor mode
 (When wait bit = "1")



(When wait bit = "0")



(When wait bit = "1" or "0" in common)



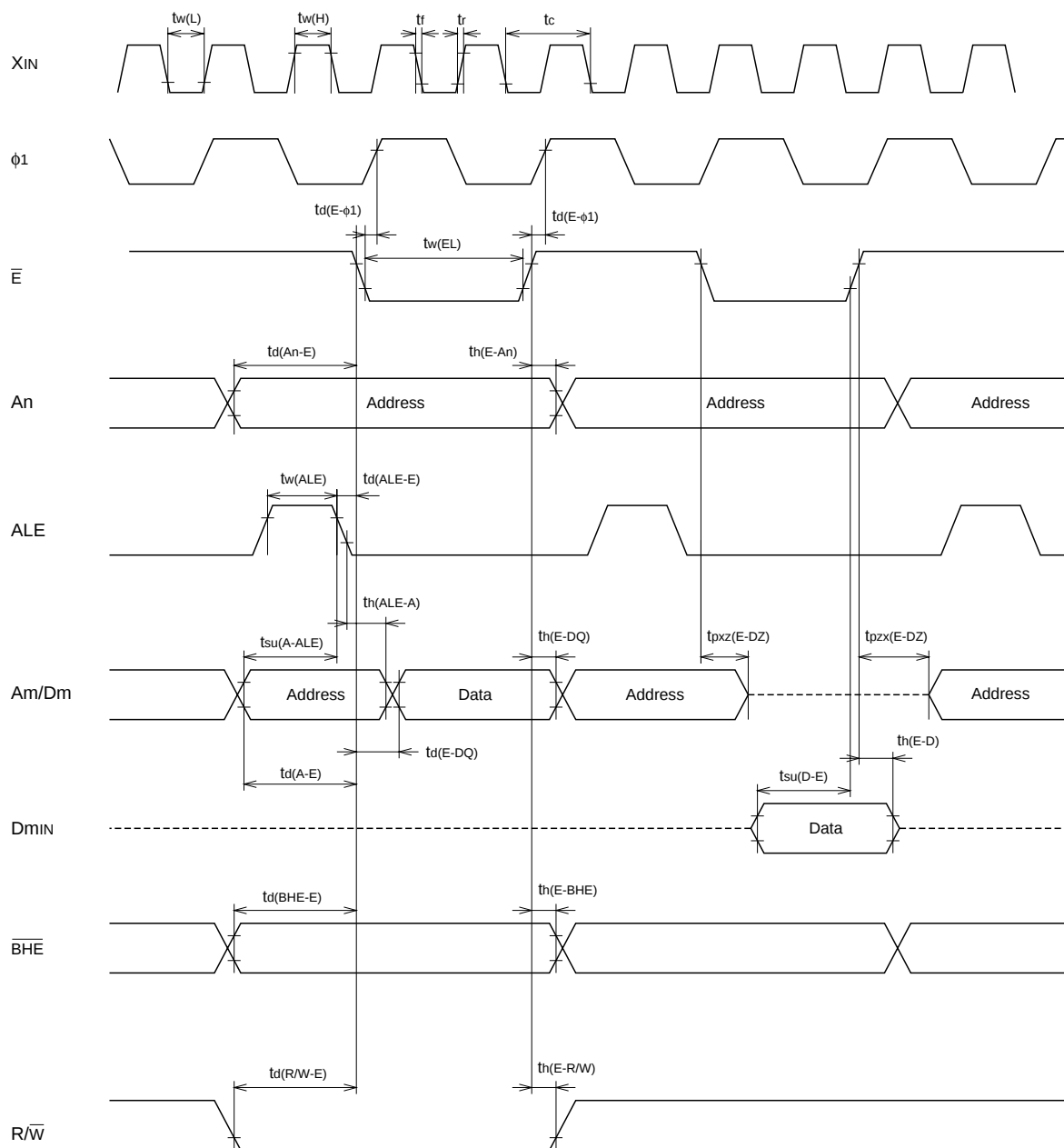
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$

[External bus mode A]

Memory expansion mode and microprocessor mode

(No wait : When wait bit = "1")



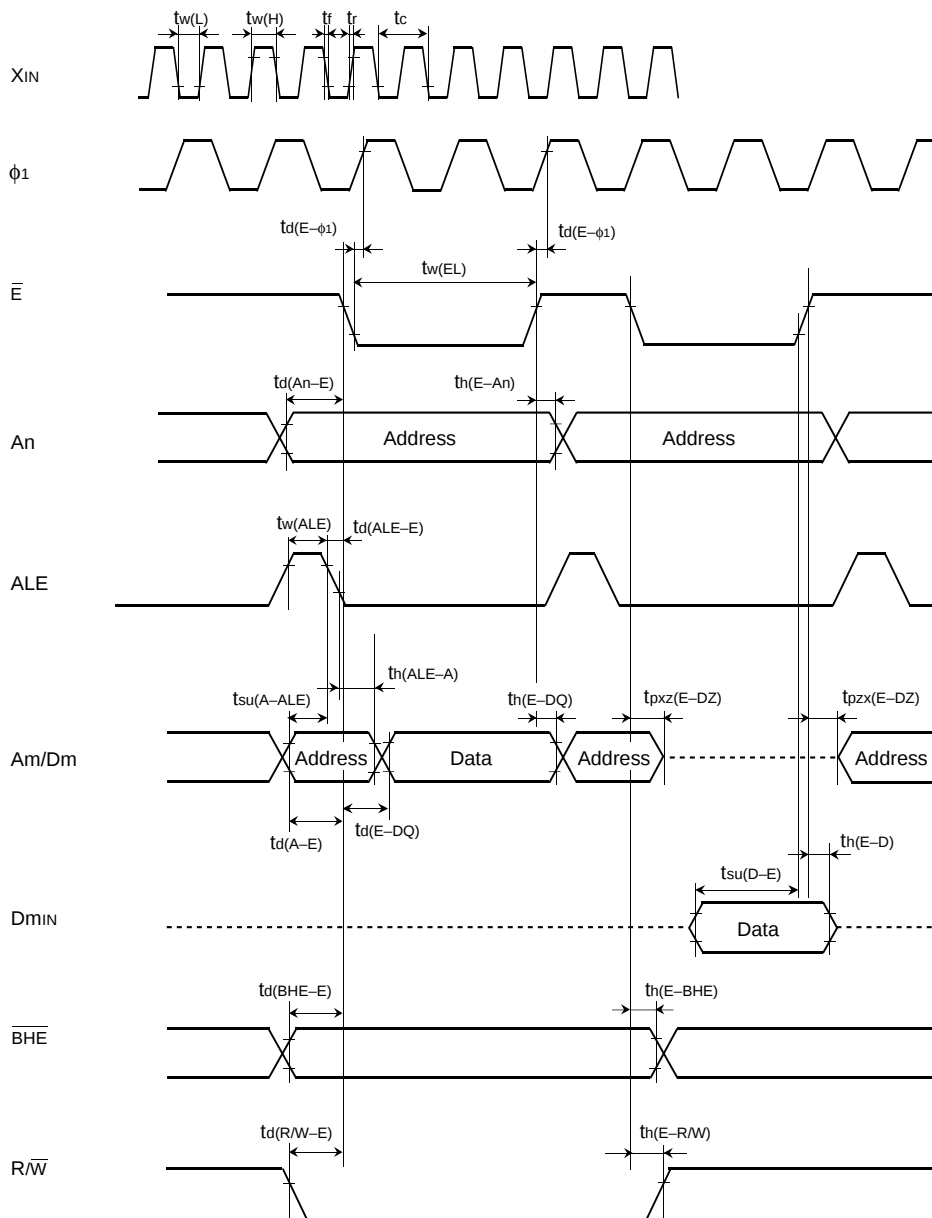
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

[External bus mode A]

Memory expansion mode and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection = "1".)



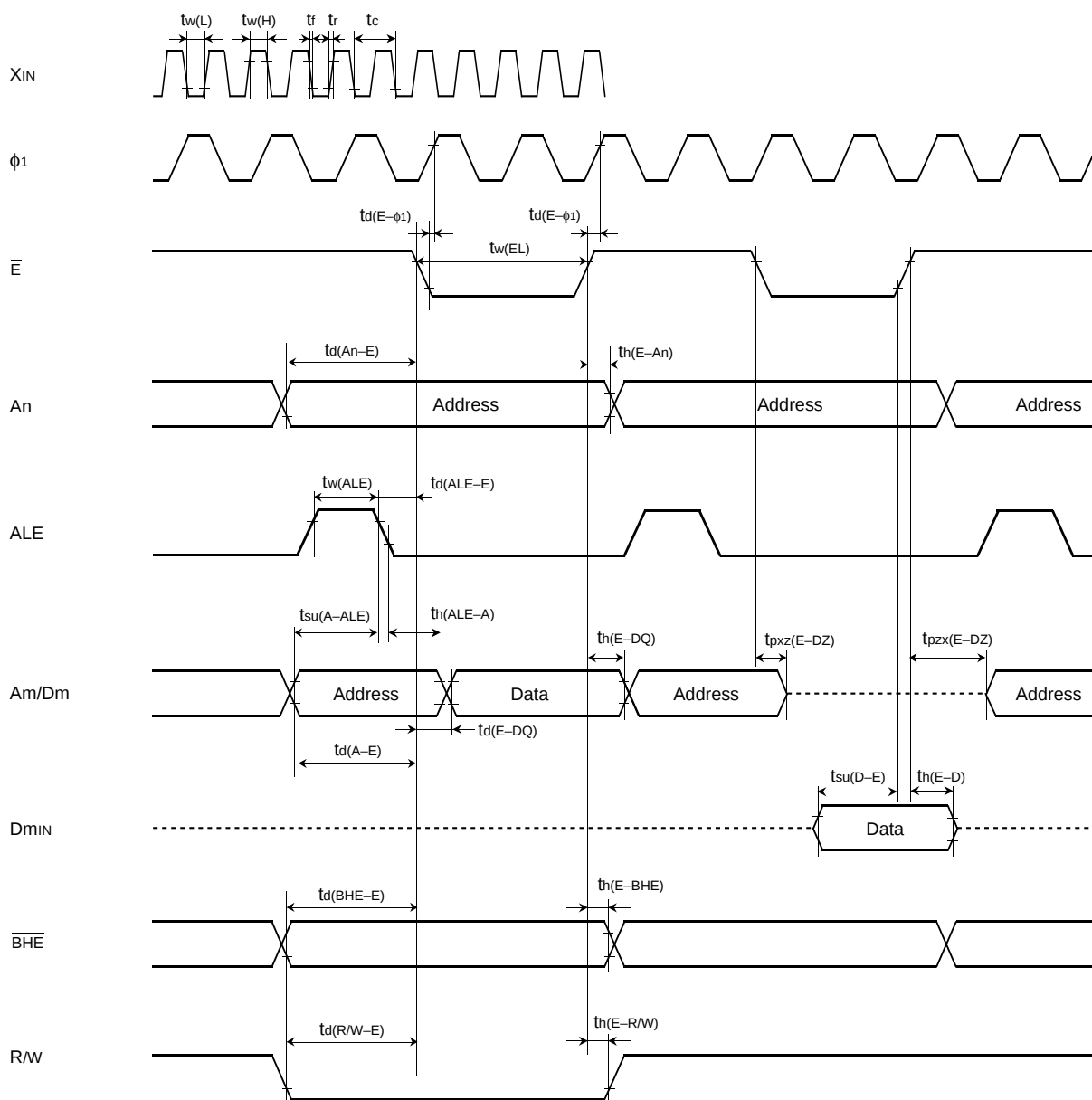
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

[External bus mode A]

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



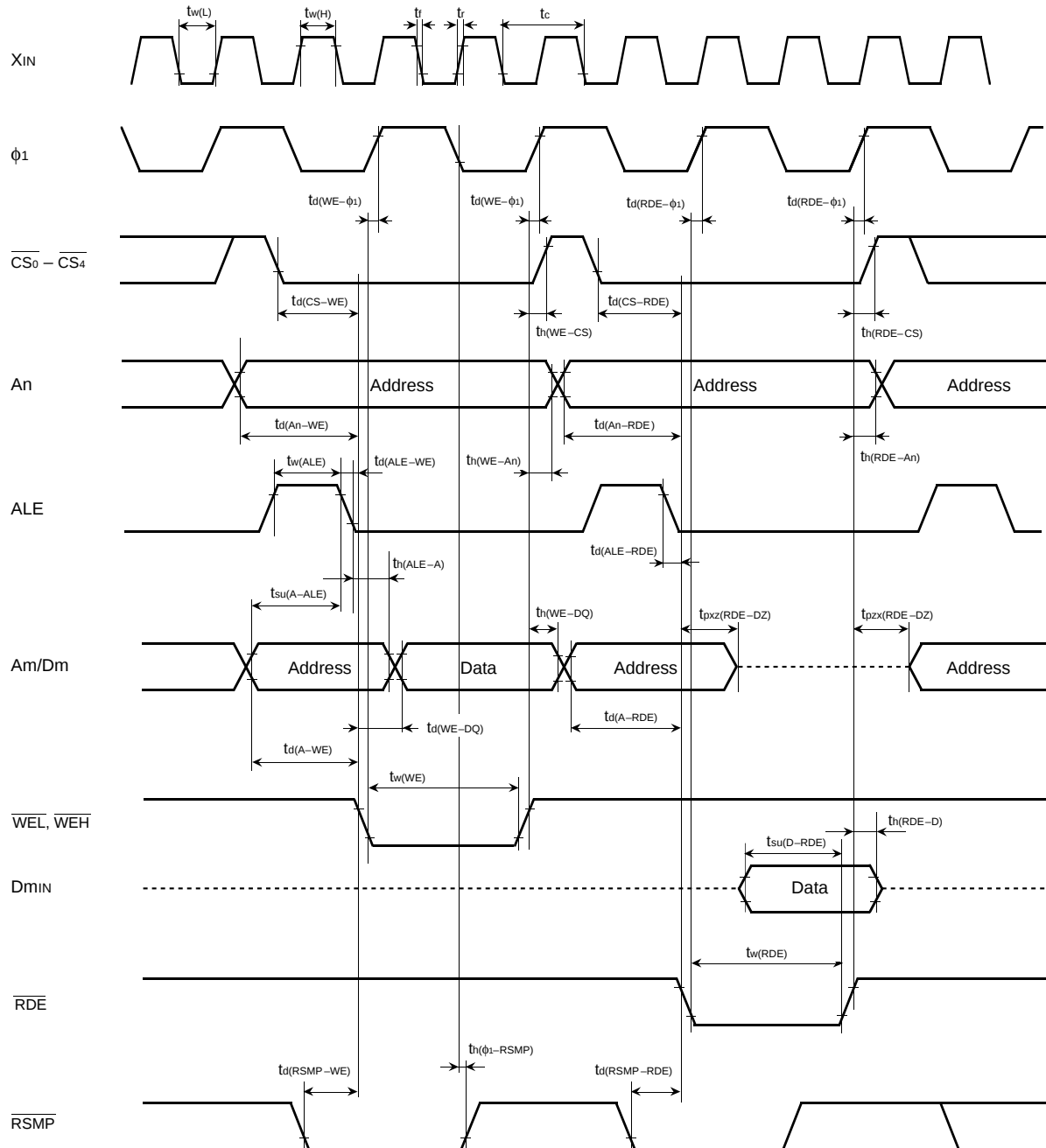
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{MIN} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

[External bus mode B]

Memory expansion mode and microprocessor mode

(No wait : When wait bit = "1")



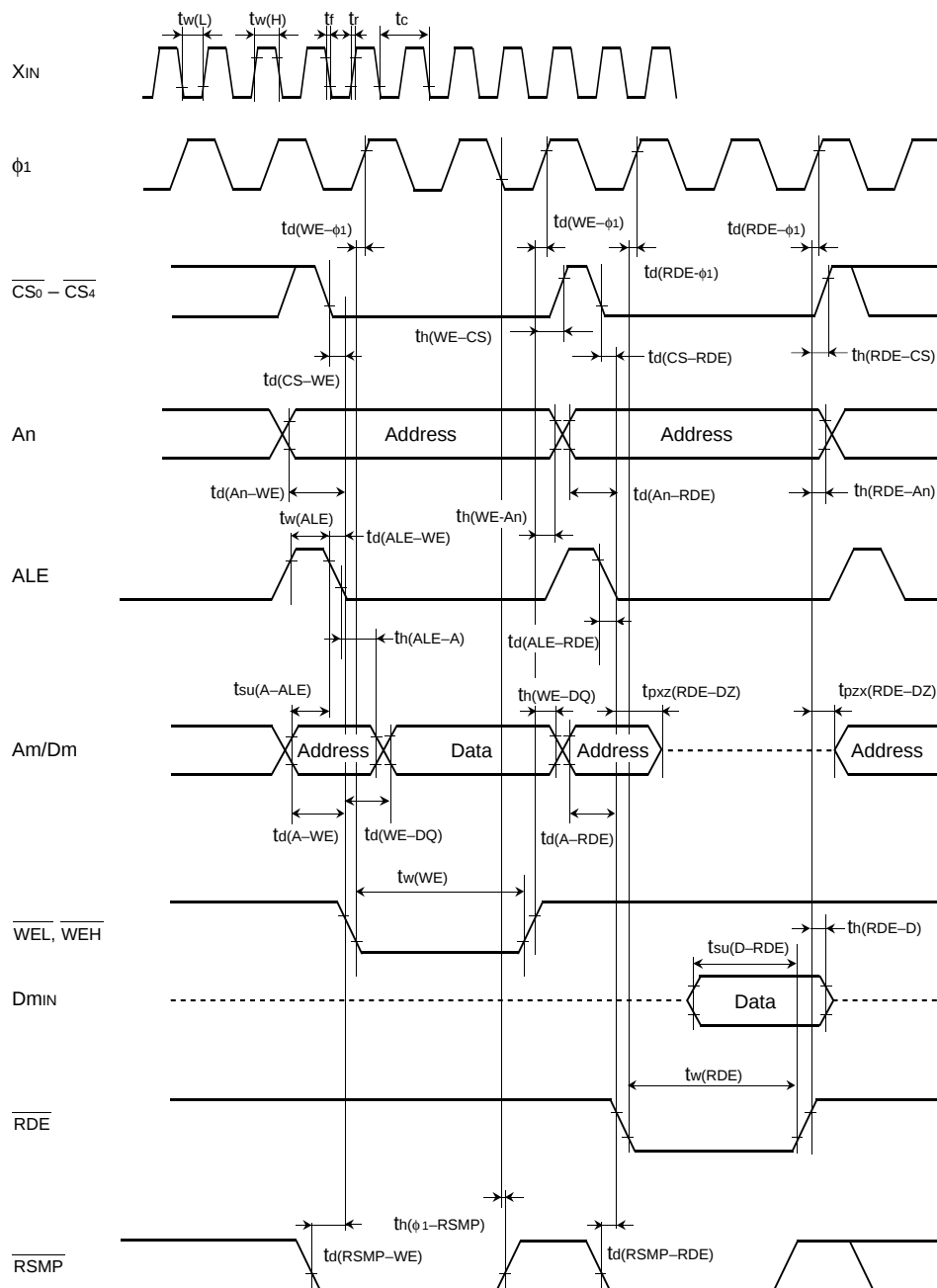
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

[External bus mode B]

Memory expansion mode and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)



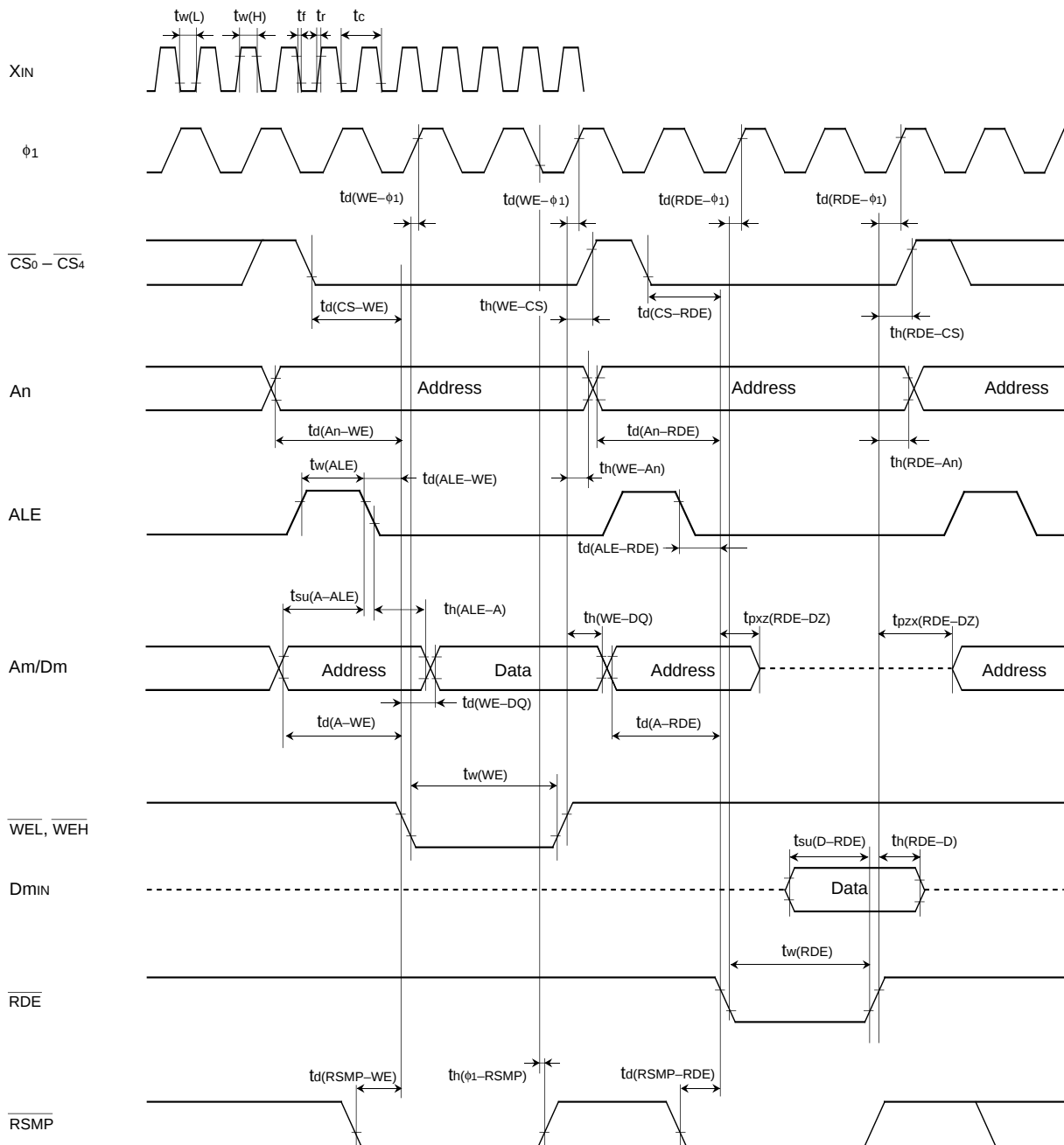
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

[External bus mode B]

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

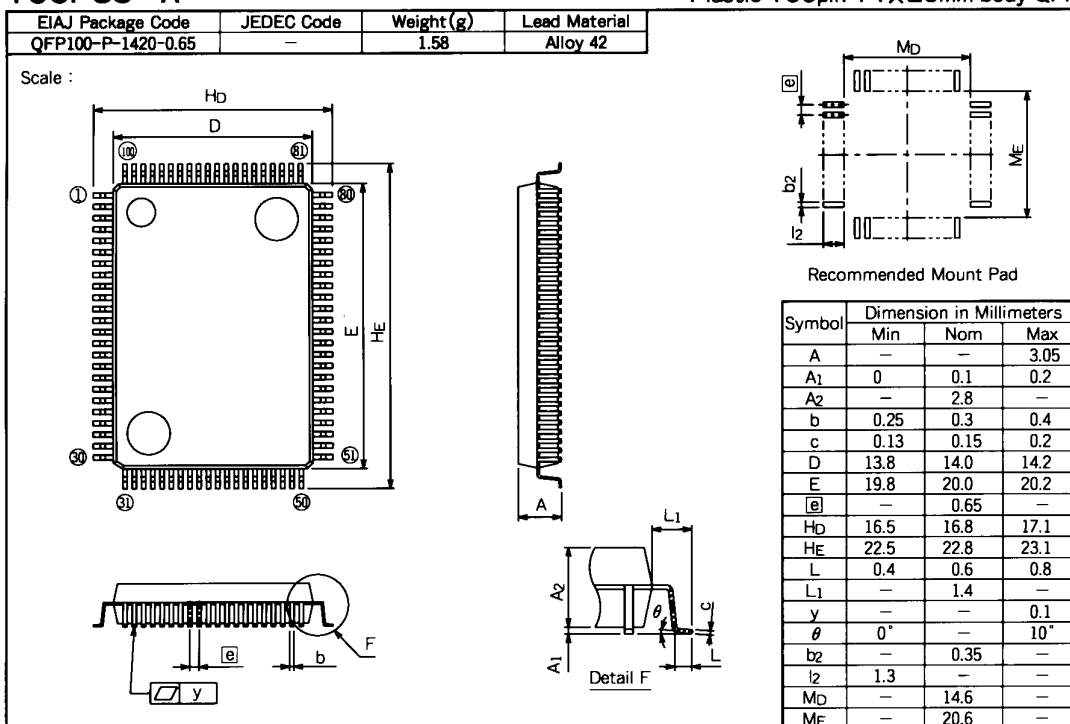
M37736EBHXXXGP
M37736EBHGS

PROM VERSION OF M37736MHBXXXGP

PACKAGE OUTLINE

100P6S-A

Plastic 100pin 14x20mm body QFP



Renesas Technology Corp.

Nippon Bldg., 6-2, Otemachi 2-chome, Chiyoda-ku, Tokyo, 100-0004 Japan

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REVISION DESCRIPTION LIST

M37736EBBXXXGP, M37736EBBGS Datasheet

Rev. No.	Revision Description		Rev. date
1.00	First Edition		970611
2.00	The following are revised:		980731
	Page	Previous Version	Revised Version
	P9 Right column Line 2	The M37736EBBXXXGP has 28 powerful addressing modes. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for the details of each addressing mode. MACHINE INSTRUCTION LIST The M37736EBBXXXGP has 103 machine instructions. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for details.	The M37736EBBXXXGP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details. MACHINE INSTRUCTION LIST The M37736EBBXXXGP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.
	Line 10	(2) <u>80P6N</u> mark specification form	(2) <u>100P6S</u> mark specification form