

FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Pinout Optimizes DDR2 DIMM PCB Layout
- Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer
- Chip-Select Inputs Gate Data Outputs From Changing State and Minimize System Power Consumption
- Output Edge-Control Circuitry Minimizes Switching Noise in Unterminated Line
- Supports SSTL_18 Data Inputs

- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVC MOS Switching Levels on Control and $\overline{\text{RESET}}$ Inputs
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 5000-V Human-Body Model (A114-A)
 - 150-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{CC} operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL_18, except the LVC MOS reset ($\overline{\text{RESET}}$) and LVC MOS control (Cn) inputs. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL_18 specifications.

The SN74SSTU32864D operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and should not be used.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared and the data outputs are driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time required to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SN74SSTU32864D must ensure that the outputs remain low, thus ensuring no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKE	Tape and reel	SN74SSTU32864DGKER	SU864D
	LFBGA – ZKE	Tape and reel	SN74SSTU32864DZKER	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+ is a trademark of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

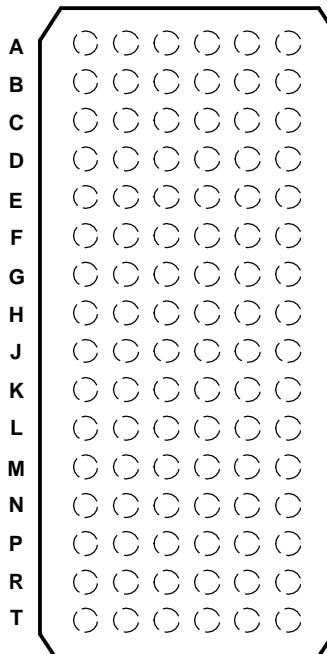
The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low. The LVCMS $\overline{\text{RESET}}$ and C_n inputs always must be held at a valid logic high or logic low level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS}}$ and $\overline{\text{CSR}}$) inputs and will gate the Q_n outputs from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. If either $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ input is low, the Q_n outputs function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control and forces the output low. If the $\overline{\text{DCS}}$ control functionality is not desired, the $\overline{\text{CSR}}$ input can be hard-wired to ground, in which case the setup-time requirement for $\overline{\text{DCS}}$ is the same as for the other D data inputs.

The two V_{REF} pins (A3 and T3) are connected together internally by approximately $150\ \Omega$. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

GKE PACKAGE
(TOP VIEW)

1 2 3 4 5 6



TERMINAL ASSIGNMENTS FOR 1:1 REGISTER (C0 = 0, C1 = 0)⁽¹⁾⁽²⁾⁽³⁾

	1	2	3	4	5	6
A	D1 (DCKE)	NC	V _{REF}	V _{CC}	Q1 (QCKE)	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V _{CC}	V _{CC}	Q3	Q16
D	D4 (DODT)	NC	GND	GND	Q4 (QODT)	DNU
E	D5	D17	V _{CC}	V _{CC}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	RESET	V _{CC}	V _{CC}	C1	C0
H	CLK	D7 (DCS)	GND	GND	Q7 (QCS)	DNU
J	CLK	CSR	V _{CC}	V _{CC}	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V _{CC}	V _{CC}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V _{CC}	V _{CC}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{CC}	V _{CC}	Q13	Q24
T	D14	D25	V _{REF}	V _{CC}	Q14	Q25

(1) Each pin name in parentheses indicates the DDR2 DIMM signal name.

(2) NC - No internal connection

(3) DNU - Do not use

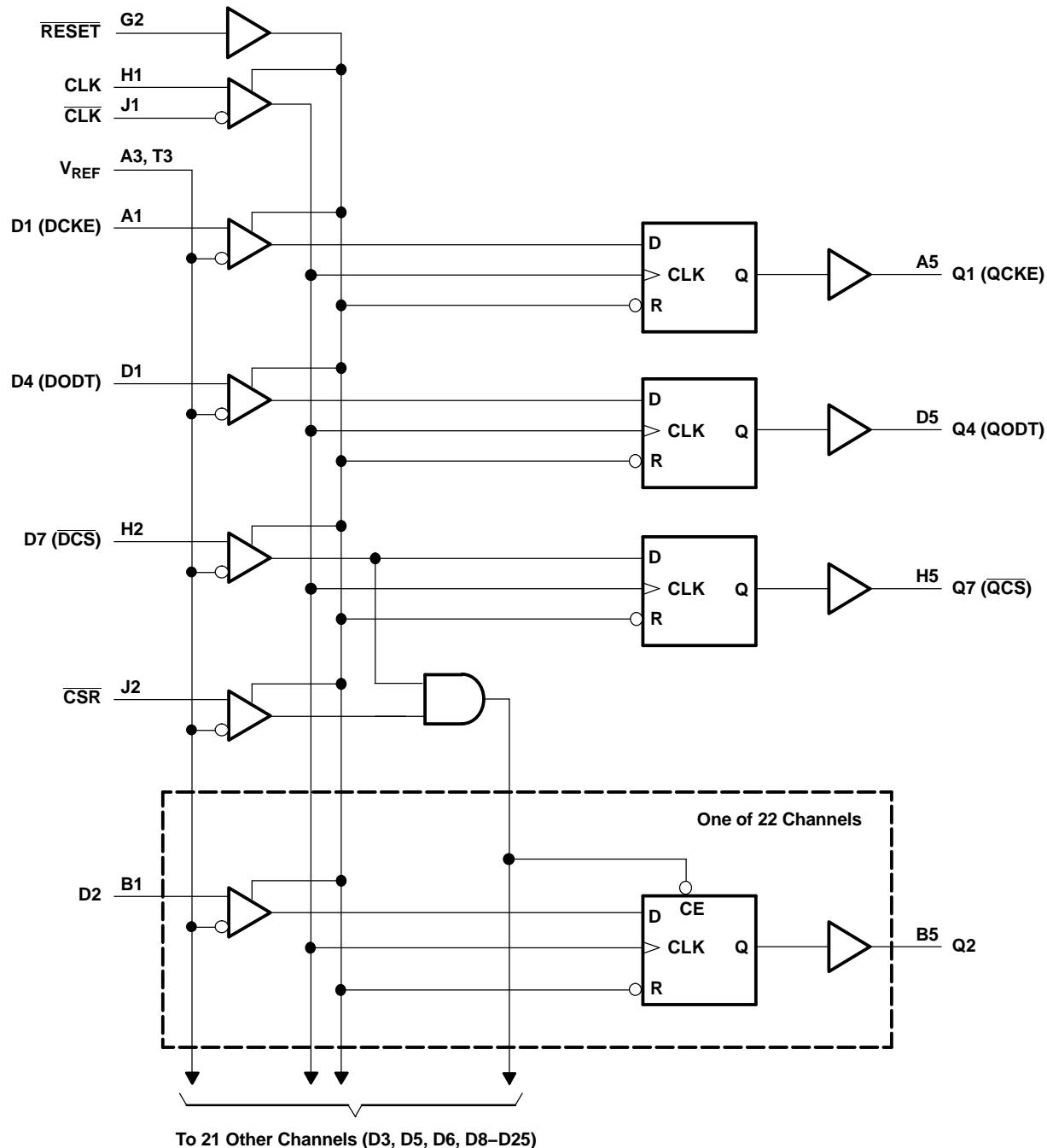
SN74SSTU32864D

25-BIT CONFIGURABLE REGISTERED BUFFER WITH SSTL_18 INPUTS AND OUTPUTS

SCES623A–FEBRUARY 2005–REVISED APRIL 2005

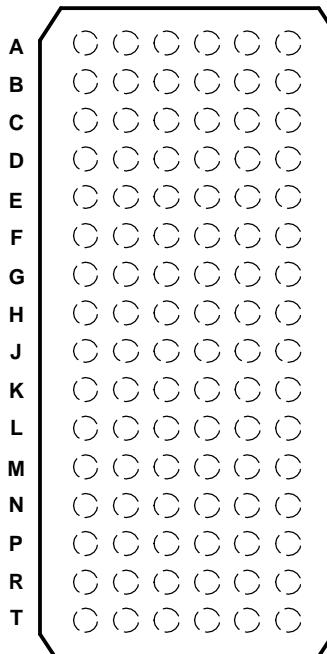
 **TEXAS
INSTRUMENTS**
www.ti.com

LOGIC DIAGRAM FOR 1:1 REGISTER CONFIGURATION (POSITIVE LOGIC)



GKE PACKAGE
 (TOP VIEW)

1 2 3 4 5 6


 TERMINAL ASSIGNMENTS FOR 1:2 REGISTER A (C0 = 0, C1 = 1)⁽¹⁾⁽²⁾⁽³⁾

	1	2	3	4	5	6
A	D1 (DCKE)	NC	V _{REF}	V _{CC}	Q1A (QCKEA)	Q1B (QCKEB)
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{CC}	V _{CC}	Q3A	Q3B
D	D4 (DODT)	NC	GND	GND	Q4A (QODTA)	Q4B (QODTB)
E	D5	DNU	V _{CC}	V _{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	RESET	V _{CC}	V _{CC}	C1	C0
H	CLK	D7 (DCS)	GND	GND	Q7A (QCSA)	Q7B (QCSB)
J	CLK	CSR	V _{CC}	V _{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{CC}	V _{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V _{CC}	V _{CC}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{CC}	V _{CC}	Q13A	Q13B
T	D14	DNU	V _{REF}	V _{CC}	Q14A	Q14B

(1) Each pin name in parentheses indicates the DDR2 DIMM signal name.

(2) NC - No internal connection

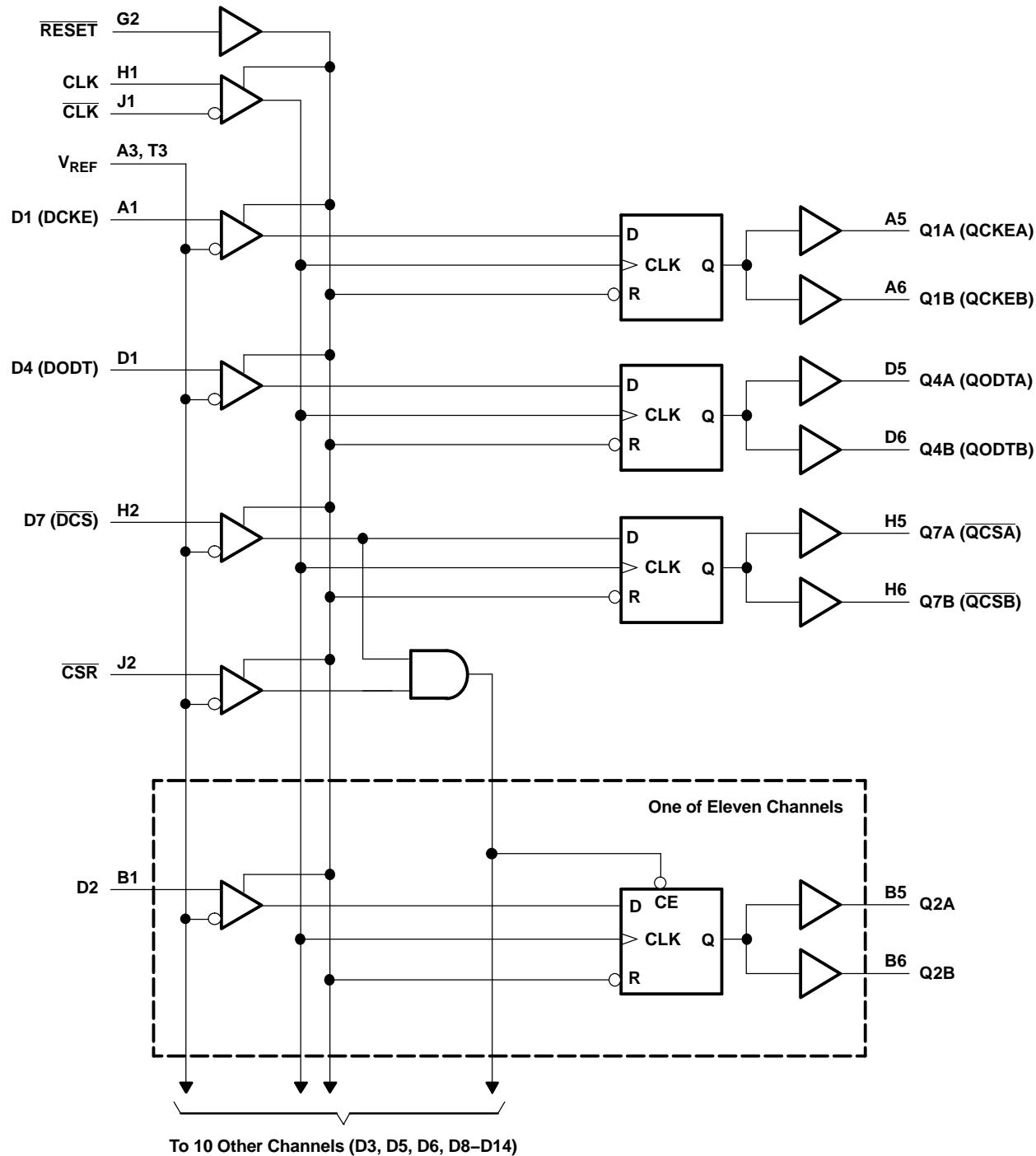
(3) DNU - Do not use

SN74SSTU32864D
25-BIT CONFIGURABLE REGISTERED BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

SCES623A—FEBRUARY 2005—REVISED APRIL 2005

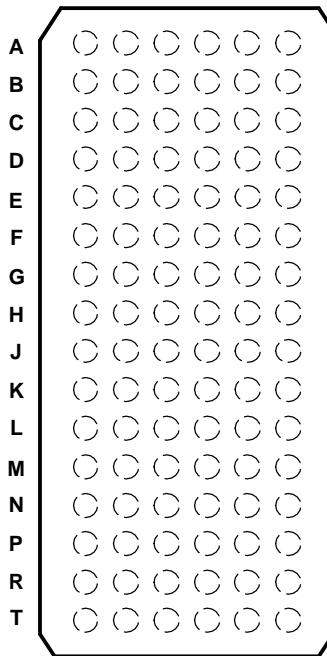
TEXAS
 INSTRUMENTS
www.ti.com

LOGIC DIAGRAM 1:2 REGISTER-A CONFIGURATION (POSITIVE LOGIC)



GKE PACKAGE
(TOP VIEW)

1 2 3 4 5 6



TERMINAL ASSIGNMENTS FOR 1:2 REGISTER B (C0 = 1, C1 = 1)⁽¹⁾⁽²⁾⁽³⁾

	1	2	3	4	5	6
A	D1	NC	V _{REF}	V _{CC}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{CC}	V _{CC}	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	V _{CC}	V _{CC}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	RESET	V _{CC}	V _{CC}	C1	C0
H	CLK	D7 (DCS)	GND	GND	Q7A (QCSA)	Q7B (QCSB)
J	CLK	CSR	V _{CC}	V _{CC}	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{CC}	V _{CC}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11 (DODT)	DNU	V _{CC}	V _{CC}	Q11A (QODTA)	Q11B (QODTB)
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{CC}	V _{CC}	Q13A	Q13B
T	D14 (DCKE)	DNU	V _{REF}	V _{CC}	Q14A (QCKEA)	Q14B (QCKEB)

(1) Each pin name in parentheses indicates the DDR2 DIMM signal name.

(2) NC - No internal connection

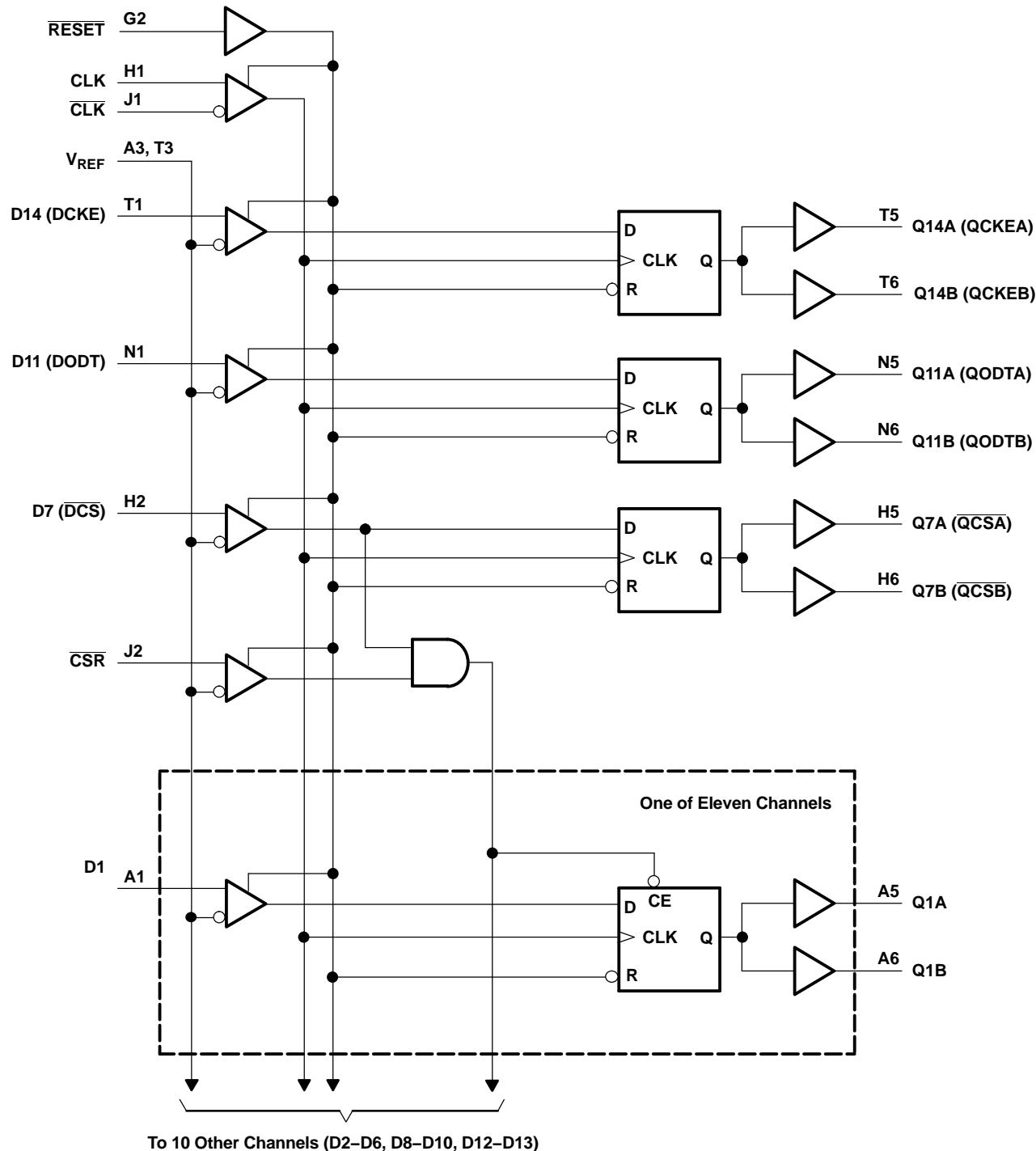
(3) DNU - Do not use

SN74SSTU32864D
25-BIT CONFIGURABLE REGISTER-BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

SCES623A—FEBRUARY 2005—REVISED APRIL 2005

TEXAS
 INSTRUMENTS
www.ti.com

LOGIC DIAGRAM 1:2 REGISTER-B CONFIGURATION (POSITIVE LOGIC)



TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V _{CC}	Power-supply voltage	1.8 V nominal
V _{REF}	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
CLK	Negative master clock input	Differential input
C0, C1	Configuration control inputs – Register A, Register B, 1:1, 1:2 select	LVCMOS inputs
RESET	Asynchronous reset input – resets registers and disables V _{REF} data and clock differential-input receivers. When RESET is low, all Q outputs are forced low.	LVCMOS input
D1–D25	Data inputs – clocked in on the crossing of the rising edge of CLK and the falling edge of CLK	SSTL_18 inputs
CSR, DCS	Chip select inputs – disables register clocking ⁽¹⁾ when both inputs are high	SSTL_18 inputs
DODT	The outputs of this register bit will not be suspended by the DCS and CSR control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the DCS and CSR control.	SSTL_18 input
Q1–Q25 ⁽²⁾	Data outputs that are suspended by the DCS and CSR control	1.8-V CMOS outputs
QCS	Data output that will not be suspended by the DCS and CSR control	1.8-V CMOS output
QODT	Data output that will not be suspended by the DCS and CSR control	1.8-V CMOS output
QCKE	Data output that will not be suspended by the DCS and CSR control	1.8-V CMOS output
NC	No internal connection	
DNU	Do not use – inputs are in standby-equivalent mode, and outputs are driven low.	

(1) Data inputs = D2, D3, D5, D6, D8–D25 when C0 = 0 and C1 = 0
 Data inputs = D2, D3 D5, D6, D8–D14 when C0 = 0 and C1 = 1
 Data inputs = D1–D6, D8–D10, D12, D13 when C0 = 1 and C1 = 0
 (2) Data outputs = Q2, Q3, Q5, Q6, Q8–Q25 when C0 = 0 and C1 = 0
 Data outputs = Q2, Q3 Q5, Q6, Q8–Q14 when C0 = 0 and C1 = 1
 Data outputs = Q1–Q6, Q8–Q10, Q12, Q13 when C0 = 1 and C1 = 1

FUNCTION TABLES

RESET	DCS	CSR	INPUTS			OUTPUT Q _n
			CLK	CLK	D _n	
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q ₀
H	X	X	L or H	L or H	X	Q ₀
L	X or floating	L				

RESET	CLK	CLK	INPUTS		OUTPUTS
			DCKE,	DCS,	
H	↑	↓	H		H
H	↑	↓	L		L
H	L or H	L or H	X		Q ₀
L	X or floating	X or floating	X or floating		L

SN74SSTU32864D

25-BIT CONFIGURABLE REGISTERED BUFFER WITH SSTL_18 INPUTS AND OUTPUTS

SCES623A—FEBRUARY 2005—REVISED APRIL 2005



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	2.5	V
V_I	Input voltage range ⁽²⁾⁽³⁾		-0.5	2.5	V
V_O	Output voltage range ⁽²⁾⁽³⁾		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		± 50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		± 50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		± 50	mA
	Continuous current through each V_{CC} or GND			± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾			36	°C/W
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 2.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	1.7		1.9	V
V_{REF}	Reference voltage	$0.49 \times V_{CC}$	$0.5 \times V_{CC}$	$0.51 \times V_{CC}$	V
V_I	Input voltage	0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs, \overline{CSR}	$V_{REF} + 250$ mV		V
V_{IL}	AC low-level input voltage	Data inputs, \overline{CSR}		$V_{REF} - 250$ mV	V
V_{IH}	DC high-level input voltage	Data inputs, \overline{CSR}	$V_{REF} + 125$ mV		V
V_{IL}	DC low-level input voltage	Data inputs, \overline{CSR}		$V_{REF} - 125$ mV	V
V_{IH}	High-level input voltage	\overline{RESET} , Cn	$0.65 \times V_{CC}$		V
V_{IL}	Low-level input voltage	\overline{RESET} , Cn		$0.35 \times V_{CC}$	V
V_{ICR}	Common-mode input voltage range	CLK, \overline{CLK}	0.675	1.125	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, \overline{CLK}	600		mV
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

- (1) The \overline{RESET} and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless \overline{RESET} is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{OH}		I _{OH} = -100 μ A	1.7 V to 1.9 V	V _{CC} - 0.2		1.3	V	
		I _{OH} = -6 mA	1.7 V					
V _{OL}		I _{OL} = 100 μ A	1.7 V to 1.9 V			0.2	V	
		I _{OL} = 6 mA	1.7 V			0.4		
I _I	All inputs ⁽²⁾	V _I = V _{CC} or GND	1.9 V			\pm 5	μ A	
I _{CC}	Static standby	RESET = GND	I _O = 0	1.9 V		100	μ A	
	Static operating	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)}				40	mA	
I _{CCD}	Dynamic operating – clock only	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle	I _O = 0	1.8 V		33	μ A/MHz	
	Dynamic operating – per each data input, 1:1 configuration	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				19	μ A/clock MHz/D input	
	Dynamic operating – per each data input, 1:2 configuration					35		
I _{CCDLP}	Chip-select-enabled low-power active mode, clock only	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle	I _O = 0	1.8 V		34	μ A/MHz	
	Chip-select-enabled low-power active mode, 1:1 configuration	RESET = V _{CC} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle				2	μ A/clock MHz/D input	
	Chip-select-enabled low-power active mode, 1:2 configuration					2		
C _i	Data inputs, $\overline{\text{CSR}}$	V _I = V _{REF} \pm 250 mV	1.8 V		2.5	3	3.5	pF
	CLK, $\overline{\text{CLK}}$	V _{ICR} = 0.9 V, V _{I(PP)} = 600 mV			2		3	
	RESET	V _I = V _{CC} or GND				2.5		

(1) All typical values are at V_{CC} = 1.8 V, T_A = 25°C.

(2) Each V_{REF} pin (A3 or T3) should be tested independently, with the other (untested) pin open. Since the two V_{REF} pins are connected internally, the total maximum input current on the V_{REF} input is doubled (\pm 10 μ A).

Timing Requirements⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

			MIN	MAX	UNIT
f _{clock}	Clock frequency			500	MHz
t _w	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low			1	ns
t _{act}	Differential inputs active time ⁽²⁾			10	ns
t _{inact}	Differential inputs inactive time ⁽³⁾			15	ns
t _{su}	Setup time	DCS before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow , $\overline{\text{CSR}}$ high; $\overline{\text{CSR}}$ before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow , DCS high	0.6	ns	
		DCS before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow , $\overline{\text{CSR}}$ low	0.5		
		DODT, DCKE, and Data before CLK \uparrow , $\overline{\text{CLK}}$ \downarrow	0.5		
t _h	Hold time	DCS, DODT, DCKE, and Data after CLK \uparrow , $\overline{\text{CLK}}$ \downarrow	0.5		ns

(1) All input slew rates are 1 V/ns \pm 20%.

(2) V_{REF} must be held at a valid input level, and data inputs must be held low for a minimum time of t_{act} max after RESET is taken high.

(3) V_{REF} data and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max after RESET is taken low.

SN74SSTU32864D
25-BIT CONFIGURABLE REGISTERED BUFFER
WITH SSTL_18 INPUTS AND OUTPUTS

SCES623A—FEBRUARY 2005—REVISED APRIL 2005



Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.1 \text{ V}$		UNIT
			MIN	MAX	
f_{max}			500		MHz
$t_{pdm}^{(1)}$	CLK and \bar{CLK}	Q	1.41	2.15	ns
$t_{pdmss}^{(1)}$	CLK and \bar{CLK}	Q		2.35	ns
$t_{RPHL}^{(1)}$	RESET	Q		3	ns

(1) Includes 350-ps test-load transmission-line delay

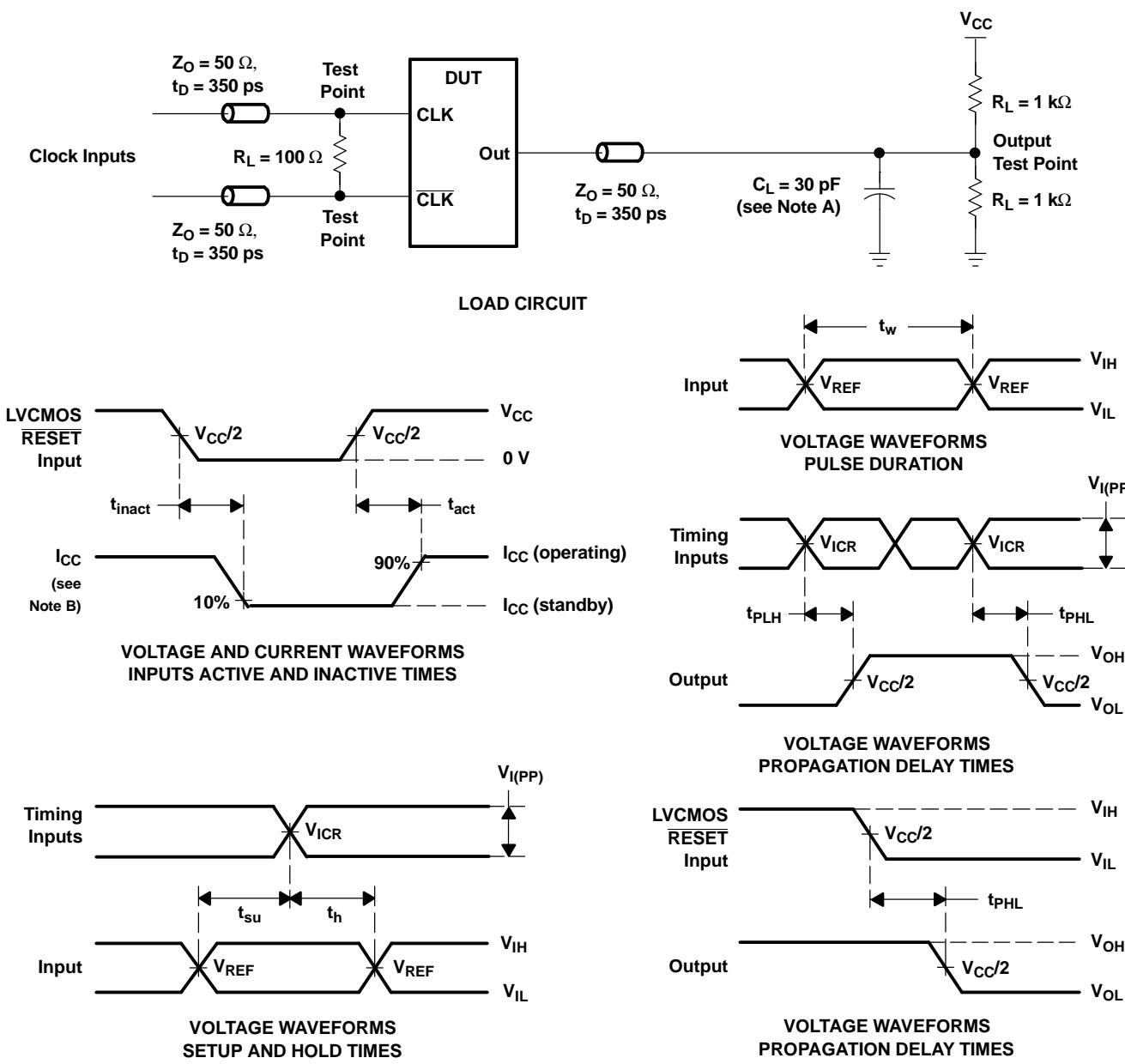
Output Slew Rates

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM	TO	$V_{CC} = 1.8 \text{ V} \pm 0.1 \text{ V}$		UNIT
			MIN	MAX	
dV/dt_r	20%	80%	1	4	V/ns
dV/dt_f	80%	20%	1	4	V/ns
$dV/dt_{\Delta}^{(1)}$	20% or 80%	80% or 20%		1	V/ns

(1) Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

PARAMETER MEASUREMENT INFORMATION

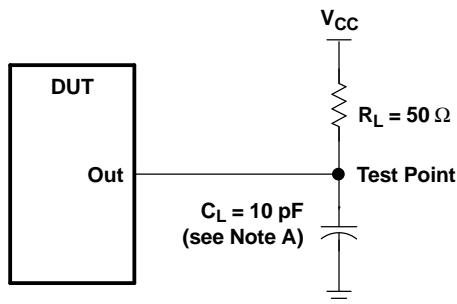


NOTES:

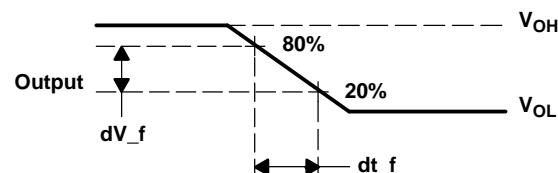
- C_L includes probe and jig capacitance.
- I_{cc} tested with clock and data inputs held at V_{CC} or GND, and $I_{O} = 0 \text{ mA}$.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, input slew rate = $1 \text{ V/ns} \pm 20\%$ (unless otherwise noted).
- The outputs are measured one at a time, with one transition per measurement.
- $V_{REF} = V_{CC}/2$
- $V_{IH} = V_{REF} + 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMS input.
- $V_{IL} = V_{REF} - 250 \text{ mV}$ (ac voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVCMS input.
- $V_{I(PP)} = 600 \text{ mV}$
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

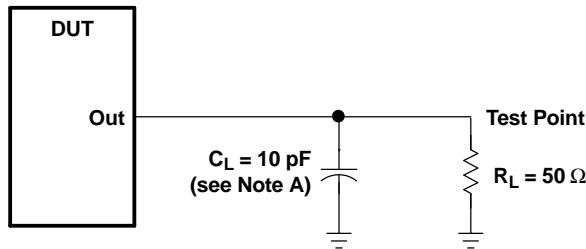
PARAMETER MEASUREMENT INFORMATION



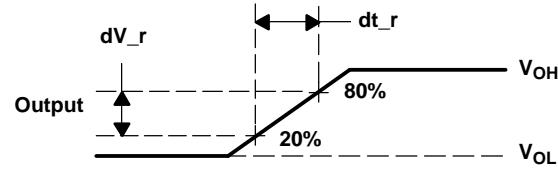
LOAD CIRCUIT
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT
LOW-TO-HIGH SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS
LOW-TO-HIGH SLEW-RATE MEASUREMENT

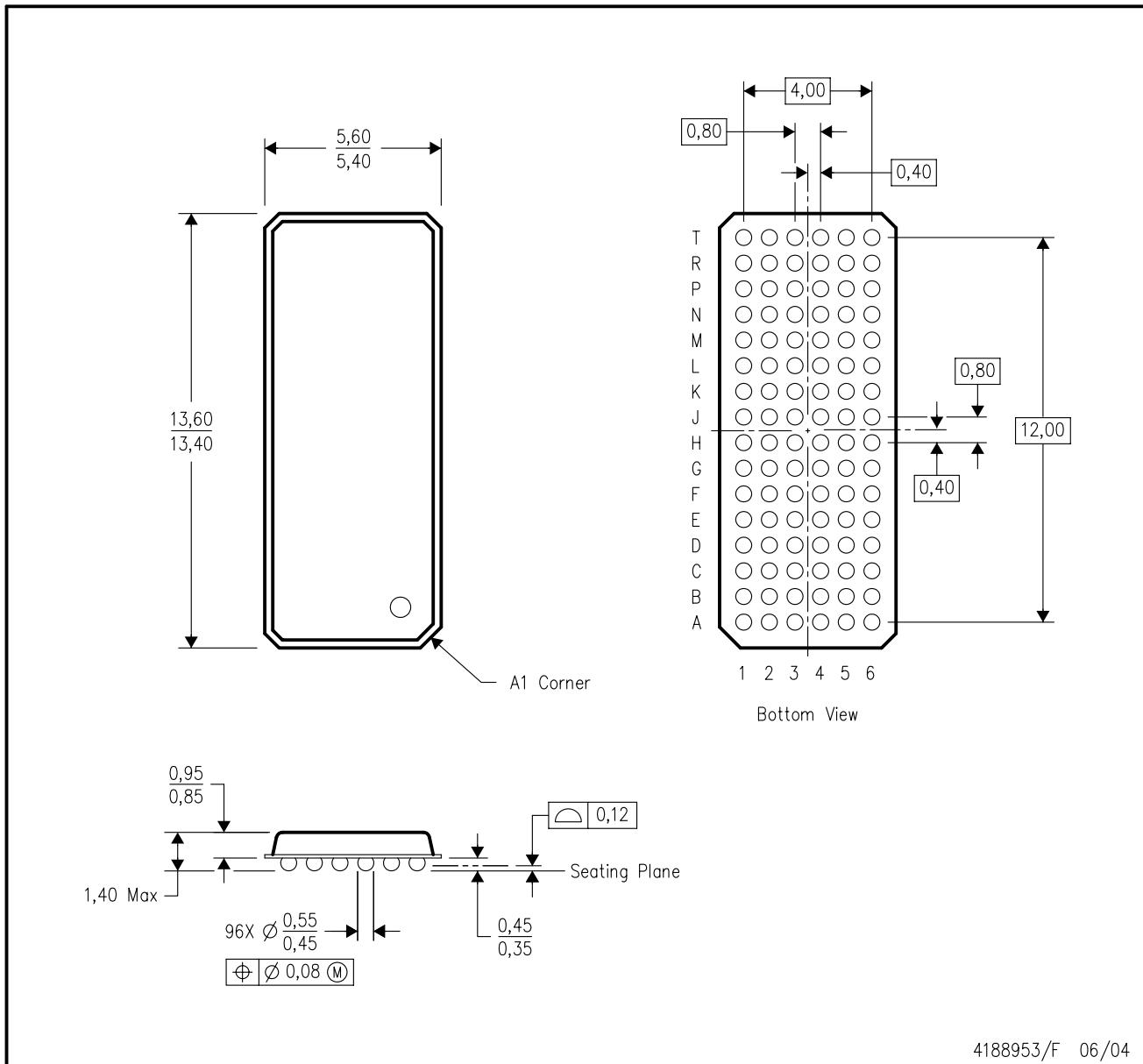
NOTES:

- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, input slew rate = $1 \text{ V/ns} \pm 20\%$ (unless otherwise specified).

Figure 2. Output Slew-Rate Measurement Information

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY

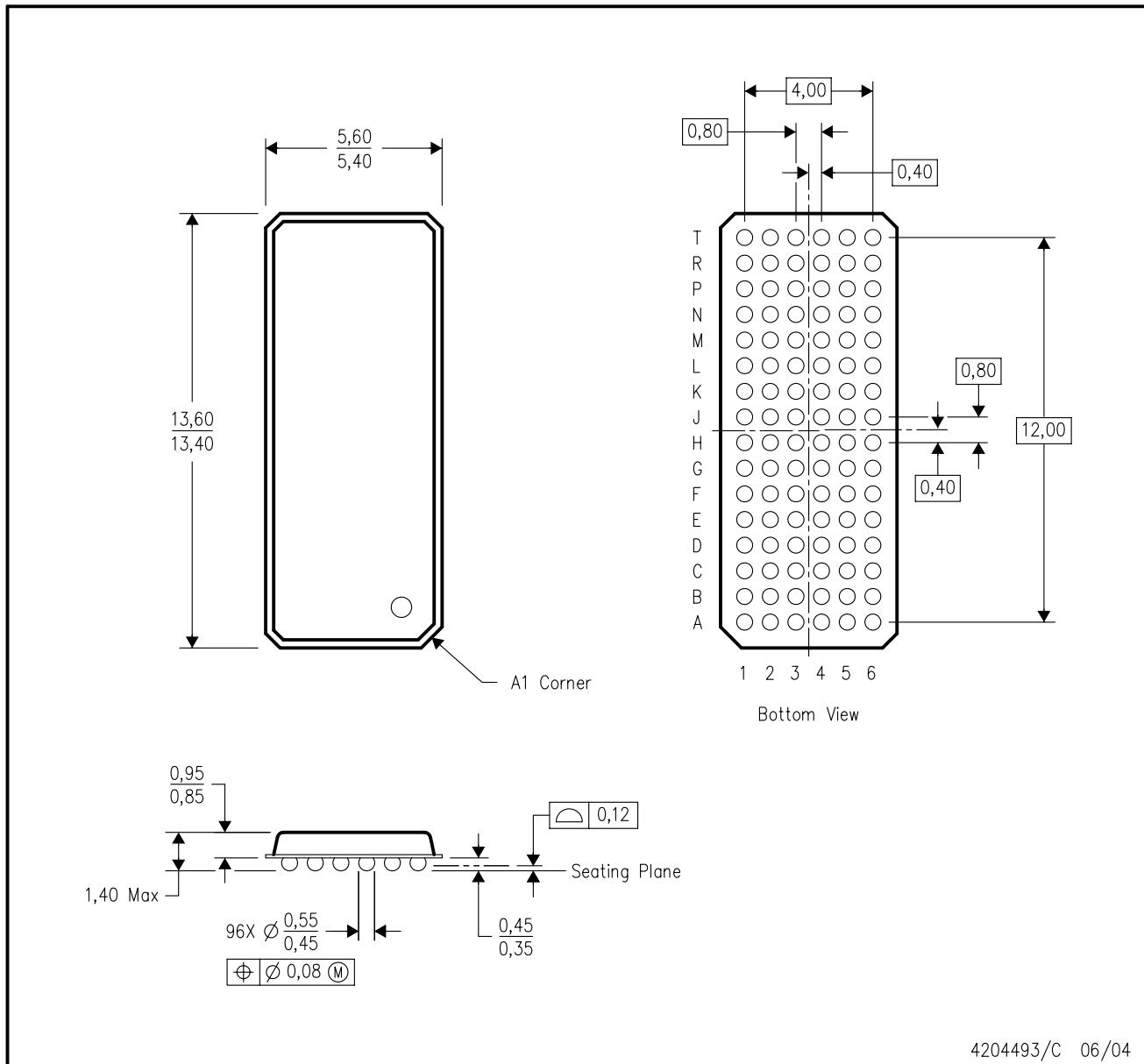


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-205 variation CC.
- This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-205 variation CC.
- This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated