DAC-HK Series
12-Bit Hybrid DAC's with Input Register

FEATURES

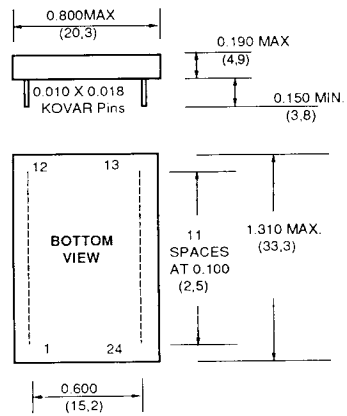
- **12-Bit resolution**
- **20 ppm/°C Tempco**
- **Input register**
- **2 Coding options**
- **Fast settling time**

GENERAL DESCRIPTION

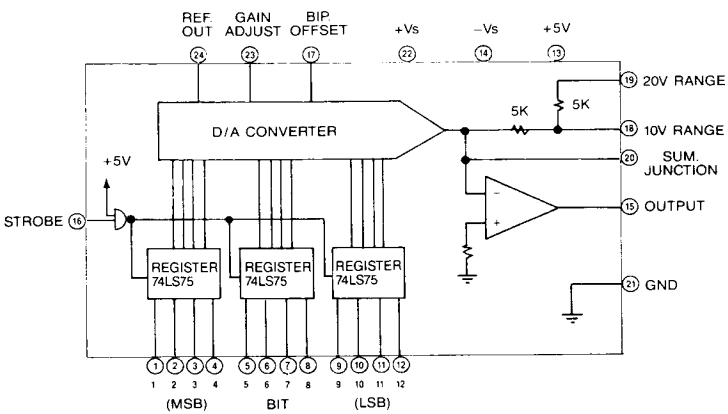
The DAC-HK Series hybrid D/A converters are high performance 12-bit devices with a fast settling voltage output. They incorporate a level controlled input storage register and are specifically designed for systems applications such as data bus interfacing with computers. When the "load" input is high, data in the storage register is held and when the load input is low, date is transferred through to the DAC. There are two basic models available by coding option: binary, and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +2.5V, 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V.

The DAC-HK Series contains a precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node a determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of 2 ppm/°C maximum. The temperature coefficient of gain is 20 ppm/°C maximum and tempco of zero is ±3 ppm/°C maximum.

MECHANICAL DIMENSIONS
INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	+5 VDC
2	BIT 2 IN	14	−15 VDC
3	BIT 3 IN	15	OUTPUT
4	BIT 4 IN	16	LOAD
5	BIT 5 IN	17	BIPOLAR OFF
6	BIT 6 IN	18	10 V RANGE
7	BIT 7 IN	19	20 V RANGE
8	BIT 8 IN	20	SUM JUNCTION
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15 VDC
11	BIT 11 IN	23	GAIN ADJ
12	BIT 12 IN (LSB)	24	REF OUT

ABSOLUTE MAXIMUM RATINGS	DAC-HK12B
Positive Supply, pin 22	+18V
Negative Supply, pin 14	−18V
Logic Supply, pin 13	+5.25V
Digital Input Voltage, pins 1-12 & 16	+5.5V
Output Current, pin 15	±20 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	
Resolution	12 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary Two's Complement[1]
Input Logic Level, bit ON ("1")	+2.0V to +5.5V
Input Logic Level, bit OFF ("0")	0V to +0.8V
Logic Loading	1 LSTTL load
Load Input[2]	High ("1") = hold data Low ("0") = transfer data
Load Input Loading	3 LSTTL loads

OUTPUT	
Output Voltage Ranges[3], unipolar	0 to +10V
Output Voltage Ranges[3], bipolar	±2.5V ±5V ±10V
Output Current	±5 mA min.
Output Impedance	0.05 ohm

PERFORMANCE[4]	
Linearity Error, max.	±½ LSB
Differential Linearity Error, max.	±¾ LSB
Gain Error, before trimming	±0.1%
Zero Error, before trimming	±0.05%
Gain Tempco, max.	±20 ppm/°C
Zero Tempco, unipolar, max.	±5 ppm/°C of FSR
Offset Tempco, bipolar, max.	±10 ppm/°C of FSR
Diff. Linearity Error Tempco, max.	±2 ppm/°C of FSR
Monotonicity	Guaranteed over oper. temp. range
Settling Time, 5V change	3 µsec.
Settling Time, 10V change	3 µsec.
Settling Time, 20V change	4 µsec.
Settling Time, 1 LSB change	800 nsec.
Slew Rate	20V/µsec.
Power Supply Rejection	±0.002% FSR/%

POWER REQUIREMENTS	
Power Supply Voltage	+15V dc ±0.5V dc at 10 mA −15V dc ±0.5V dc at 25 mA +5V dc ±0.25V dc at 35 mA ±12V dc, +5V operation[4]

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BGC, BMC) -55 °C to +125 °C (BMM/883B)
Storage Temperature Range	−65°C to +125°C
Package Type	24-pin Ceramic DIP
Pins	0.010 x 0.018 inch Kovar
Weight	0.2 ounces (6 grams)

FOOTNOTES:

1. For two's complement coding order the model described under ordering information.
2. Logic levels are the same as for data inputs.
3. By external pin connection.
4. For ±12V dc, +5V dc operation, contact factory.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1 µF (tantalum type) at the +15, −15, and +5V supply pins. The capacitors should be connected as close to the pins as possible. In high RFI noise environments these capacitors should be shunted with 0.01 µF ceramic capacitors.
2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 21 where they all must come together.
3. The "load" control pin is a level triggered input which causes the register to hold data with a high input and transfer data to the DAC with a low input.
4. A setup time of 50 nanoseconds minimum must be allowed for the input data. The DAC output voltage begins to change when the register output changes.
5. The external gain adjustment shown in the Connection Diagrams has a range of ±0.2% of full scale. If a wider range is desired the 18-Megohm resistor can be decreased slightly in value. The full-scale output is typically accurate within ±0.1% with no adjustment. The zero, or offset, adjustment has a range of ±0.35% of FS.
6. If the reference output terminal (pin 24) is used, an operational amplifier in non-inverting mode should be used as a buffer. Current drawn from pin 24 should be limited to ±10 µA in order not to affect the T.C. of the reference.

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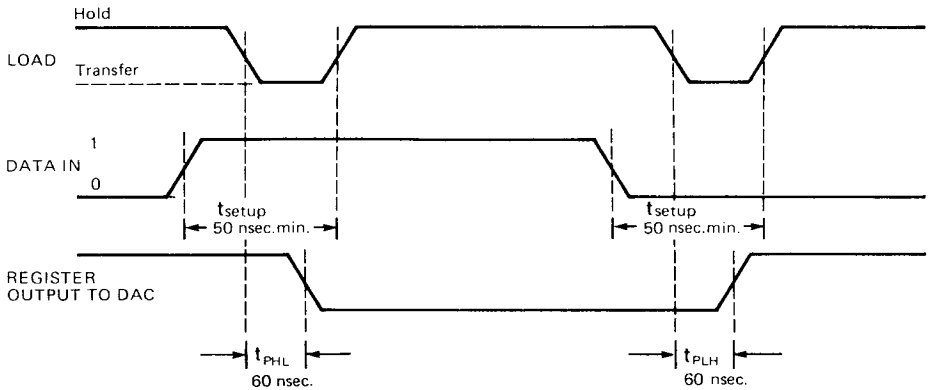
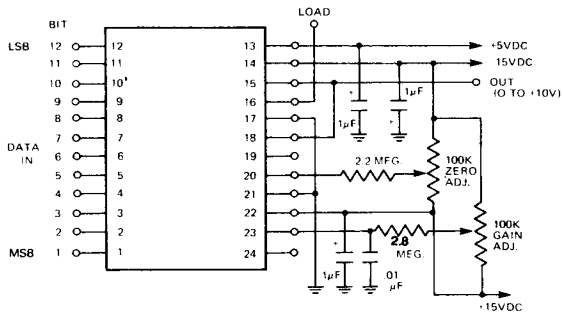
TIMING DIAGRAM



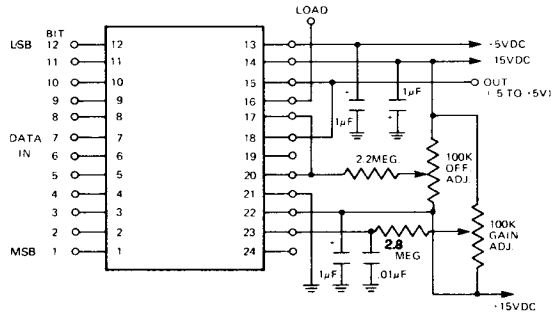
All rise and fall times ≤ 10 nsec.

CONNECTION DIAGRAMS

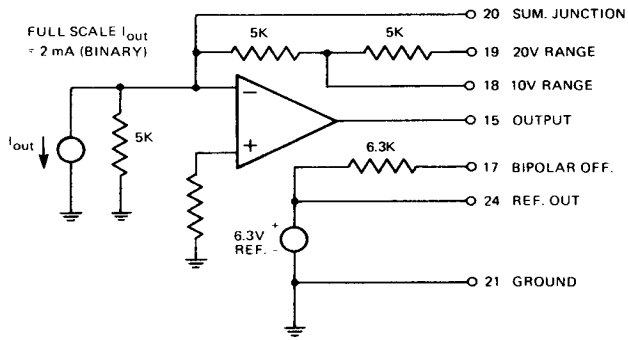
UNIPOLAR OPERATION (0 to +10V)



BIPOLAR OPERATION (±5 V)



OUTPUT CIRCUIT



OUTPUT RANGE SELECTION

RANGE	CONNECT THESE PINS TOGETHER		
±10 V	15 & 19	17 & 20	
±5 V	15 & 18	17 & 20	
±2.5 V	15 & 18	17 & 20	19 & 20
+10 V	15 & 18	17 & 21	
+5 V	15 & 18	17 & 21	19 & 20

CODING TABLES

UNIPOLAR OPERATION

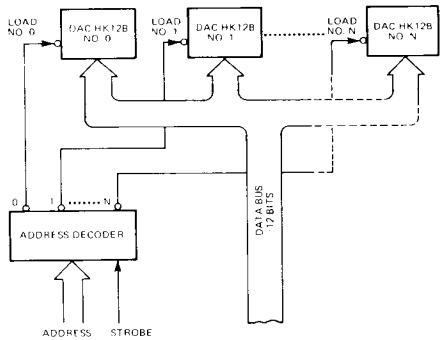
STRAIGHT BINARY MSB LSB	OUTPUT RANGES 0 to +10V	0 to +5V
1111 1111 1111	+9.9976	+4.9988
1100 0000 0000	+7.5000	+3.7500
1000 0000 0000	+5.0000	+2.5000
0100 0000 0000	+2.5000	+1.2500
0000 0000 0001	+0.0024	+0.0012
0000 0000 0000	0.0000	0.0000

BIPOLAR OPERATION

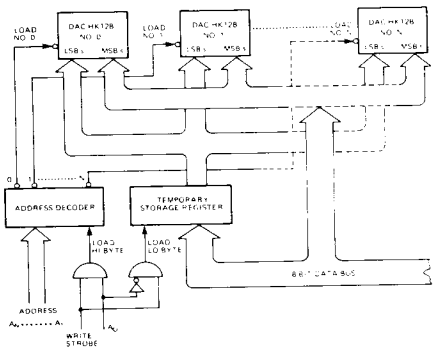
OFFSET BINARY MSB LSB	TWO's COMPLEMENT MSB LSB	OUTPUT RANGES ±10V	±5V	±2.5V
1111 1111 1111	0111 1111 1111	+9.9951	+4.9976	+2.4988
1100 0000 0000	0100 0000 0000	+5.0000	+2.5000	+1.2500
1000 0000 0000	0000 0000 0000	0.0000	0.0000	0.0000
0100 0000 0000	1100 0000 0000	−5.0000	−2.5000	−1.2500
0000 0000 0001	1000 0000 0001	−9.9951	−4.9976	−2.4988
0000 0000 0000	1000 0000 0000	−10.0000	−5.0000	−2.5000

APPLICATIONS

INTERFACING TO ≥ 12 BIT DATA BUS



INTERFACING TO 8 BIT DATA BUS



CALIBRATION PROCEDURE

Select the desired output voltage range and connect the converter up as shown in the Output Range Selection Table and the Connection Diagrams. Refer to the Coding Tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 0000 0000 0000 and adjust the ZERO ADJ. potentiometer to give 0.0000V output.
2. **Gain Adjustment.** Set the input digital code to 1111 1111 1111 (straight binary) and adjust the GAIN ADJ. potentiometer to give the full-scale output voltage shown in the Coding Table.

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the digital input code to 0000 0000 0000 (offset binary) or 1000 0000 0000 (two's complement) and adjust the OFFSET ADJ. potentiometer to give the negative full-scale output voltage shown in the Coding Table.
2. **Gain Adjustment.** Set the digital input code to 1111 1111 1111 (offset binary) or a 0111 1111 1111 (two's complement) and adjust the GAIN ADJ. potentiometer to give the positive full-scale output voltage shown in the Coding Table.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
Binary Coding		
DAC-HK12BGC	0 to +70 °C	Epoxy
DAC-HK12BMC	0 to +70 °C	Herm.
DAC-HK12BMM	-55 to +125 °C	Herm.
DAC-HKB/883B	-55 to +125 °C	Herm.
2's Complement Coding		
DAC-HK12BGC-2	0 to +70 °C	Epoxy
DAC-HK12BMC-2	0 to +70 °C	Herm.
DAC-HK12BMM-2	-55 to +125 °C	Herm.
DAC-HKB-2/883B	-55 to +125 °C	Herm.

The MIL-STD-883B units are available under DESC Drawing Number 5962-89528.

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