FAIRCHILD SEMICONDUCTOR™

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MM74HC148
8-3 Line Priority Encoder

General Description

The MM74HC148 priority encoder utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LB-TTL.

This priority encoder accepts 8 input request lines 0–7 and outputs 3 lines A0–A2. The priority encoding ensures that only the highest order data line is encoded. Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. All data inputs and outputs are active at the low logic level.

All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

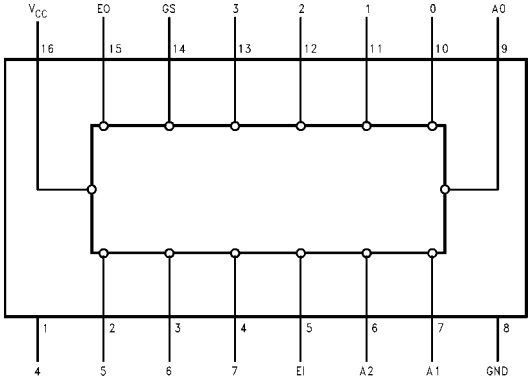
Features

- Typical propagation delay: 13 ns
- Wide supply voltage range: 2V–6V

Ordering Code:

Order Number	Package Number	Package Description
MM74HC148M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC148N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

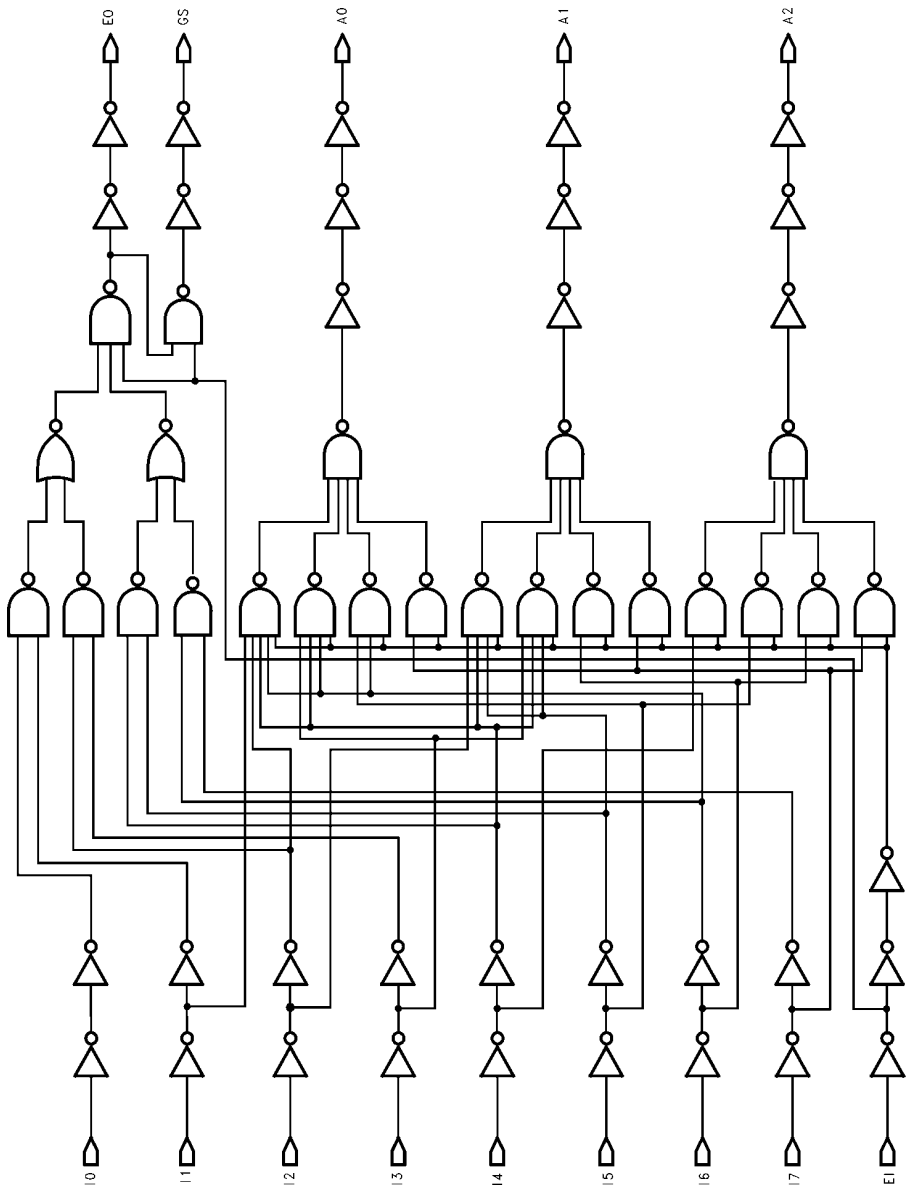


Truth Table

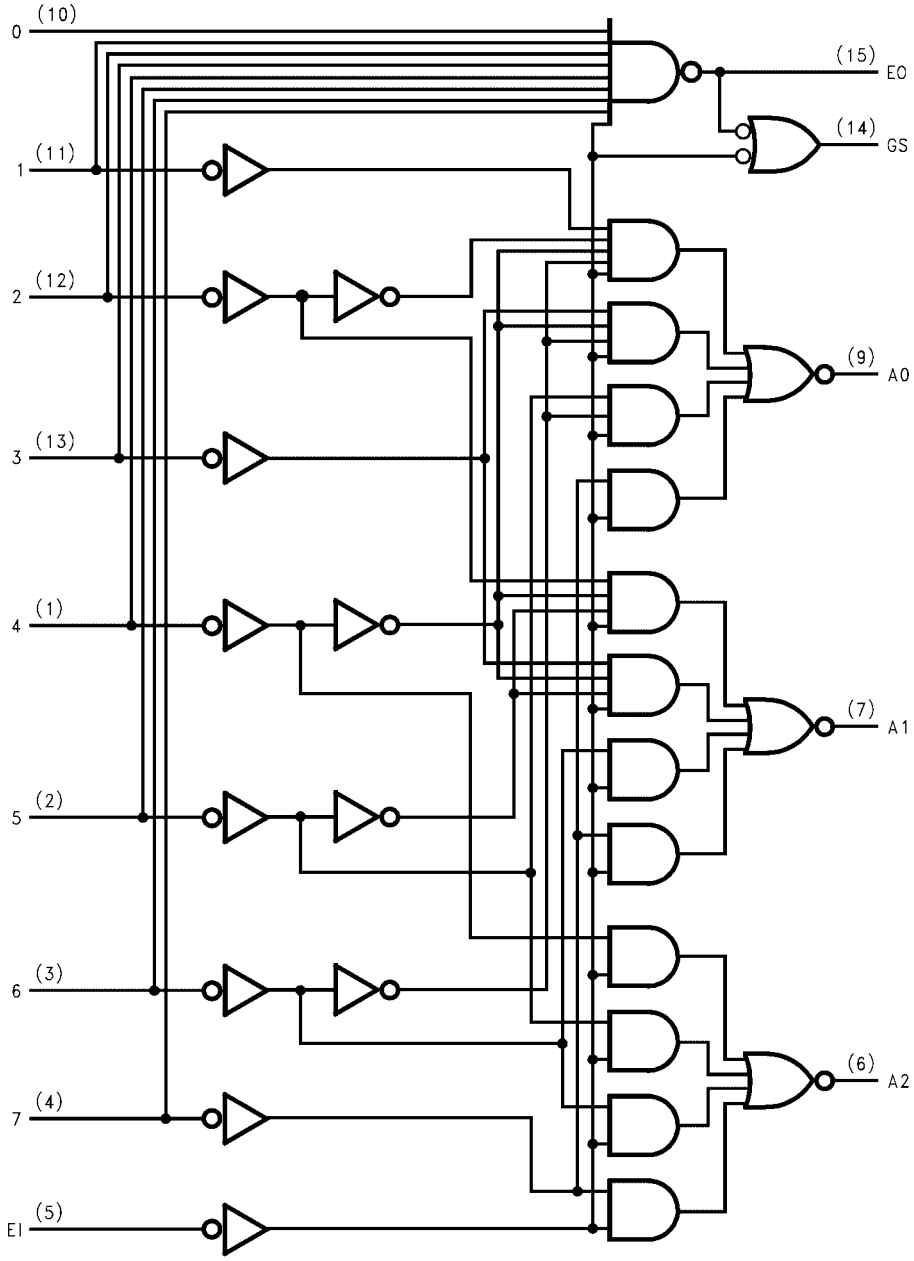
Inputs									Outputs				
EI	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**A2**	**A1**	**A0**	**GS**	**EO**
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = HIGH
L = LOW
X = Irrelevant

Schematic Diagram



Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 sec.)	260°C

Operation Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C		T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage (Note 5)		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level	V_{IN} = V_{IH} or V_{IL}						
	Output Voltage	$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.7	3.96	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level	V_{IN} = V_{IH} or V_{IL}						
	Output Voltage	$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent	V_{IN} = V_{CC} or GND	6.0V		8.0	80	160	μA
	Supply Current	I_{OUT} = 0 μA						

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Note 5: V_{IL} limits are currently tested at 20% of V_{CC}.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Input to Any Output		14		ns

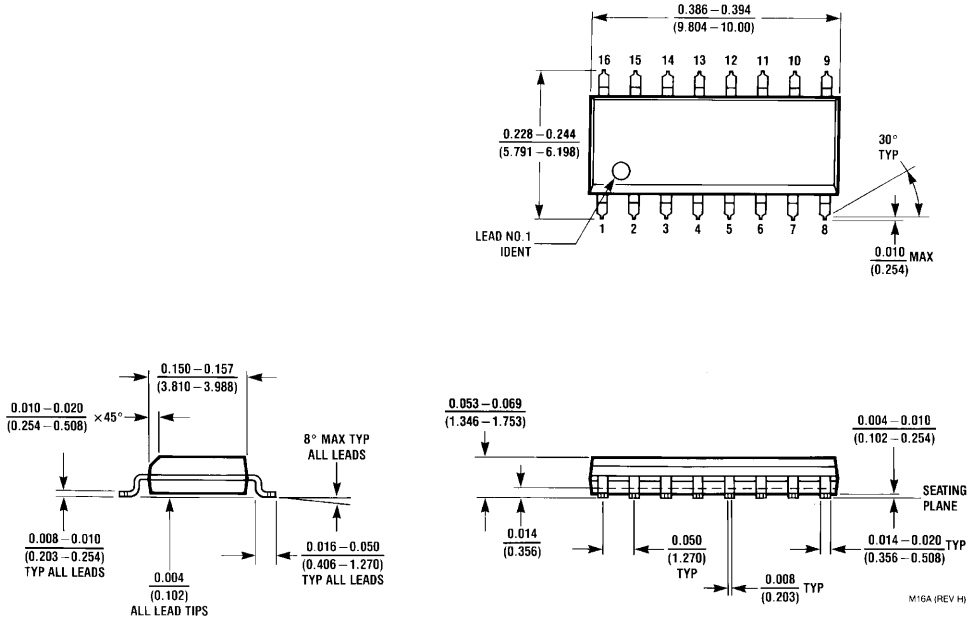
AC Electrical Characteristics

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	V_{CC}	T_A = 25°C	−40°C to +85°C	−55°C to +125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Inputs 0–7	2.0V		140	175	210	ns
	to Outputs	4.5V	14	28	35	42	ns
	A0, A1, A2	6.0V		24	30	36	ns
t_{PHL}, t_{PLH}	Inputs 0–7	2.0V		140	175	210	ns
	to	4.5V	15	28	35	42	ns
	Output EO	6.0V		24	30	36	ns
t_{PHL}, t_{PLH}	Inputs 0–7	2.0V		160	200	240	ns
	to	4.5V	17	32	40	48	ns
	Output GS	6.0V		27	34	41	ns
t_{PHL}, t_{PLH}	Input EI	2.0V		160	200	240	ns
	to Outputs	4.5V	17	32	40	48	ns
	A0, A1, A2	6.0V		27	34	41	ns
t_{PHL}, t_{PLH}	Input EI	2.0V		100	125	150	ns
	to	4.5V	12	20	25	30	ns
	Output GS	6.0V		17	21	26	ns
t_{PHL}, t_{PLH}	Input EI	2.0V		100	125	150	ns
	to	4.5V	12	20	25	30	ns
	Output EO	6.0V		17	21	26	ns
t_f, t_r	Maximum	2.0V		75	95	110	ns
	Output Rise	4.5V	7	15	19	22	ns
	and Fall Time	6.0V		13	16	19	ns
C_{pd}	Power Dissipation Capacitance (Note 6)		52				pF
C_{in}	Maximum Input Capacitance		5	10	10	10	pF

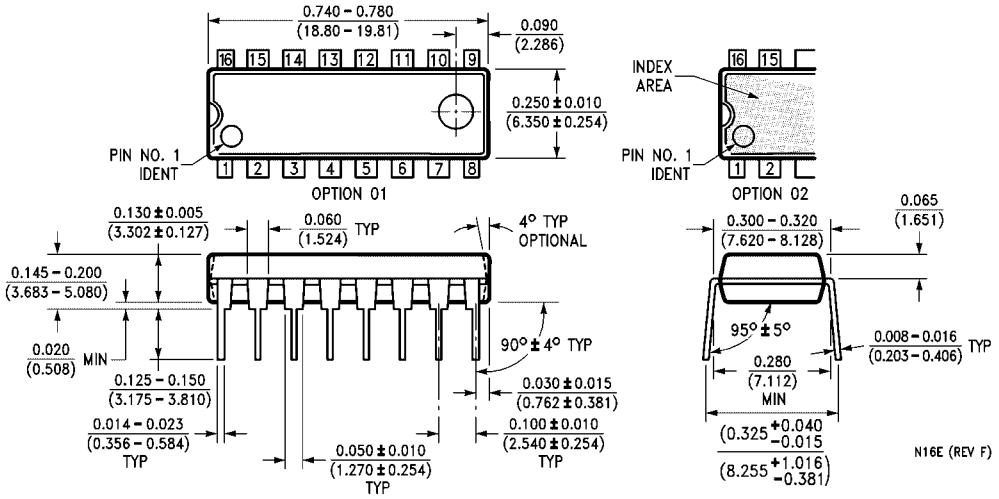
Note 6: C_{pd} determines the no load dynamic power consumption, and the no load dynamic current consumption.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E