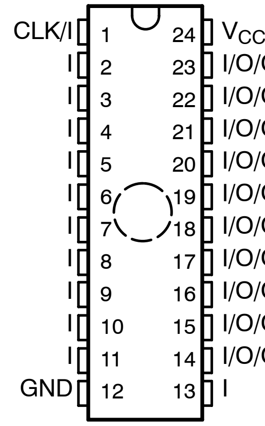
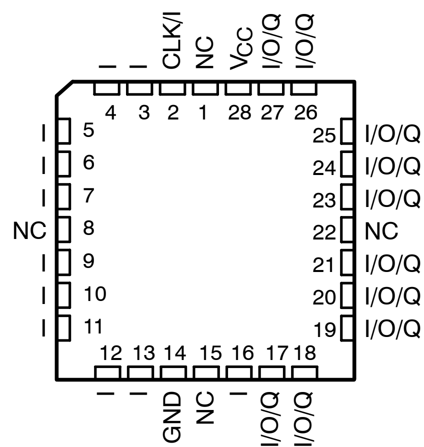
- **24-Pin Advanced CMOS PLD**
- **Virtually Zero Standby Power**
- **Propagation Delay Time:**
  I, I/O to I/O in the Turbo Mode
  -25C . . . 25 ns Max
  -30I . . . 30 ns Max
  I, I/O to I/O in the Zero-Power Mode
  -25C . . . 35 ns Max
  -30I . . . 40 ns Max
  CLK to Q
  -25C . . . 15 ns Max
  -30I . . . 20 ns Max
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User-Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Preload Capability on All Registered Outputs Allow for Improved Device Testing**
- **UV Light Erasable Cell Technology Allows for:**
  Reconfigurable Logic
  Reprogrammable Cells
  Full Factory Testing for High Programming Yield
- **Programmable Design Security Bit Prevents Copying of Logic Stored in Device**
- **Package Options Include Plastic Dual-In-Line and Clip Carrier [for One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Windowed Package**

JTL AND NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC − No internal connection
Pin assignments in operating mode

AVAILABLE OPTIONS

T_A RANGE	PACKAGE TYPE		
	CERAMIC WINDOWED DUAL-IN-LINE (JTL)	**PLASTIC DUAL-IN-LINE (NT)**	**PLASTIC CHIP CARRIER (FN)**
0°C to 75°C	TICPAL22V10Z-25CJTL	TICPAL22V10Z-25CNT	TICPAL22V10Z-25CFN
−40°C to 85°C	NA	TICPAL22V10Z-30INT	TICPAL22V10Z-30IFN

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description

The CMOS PLD devices feature variable product terms, flexible outputs, and virtually zero standby power. It combines TI's EPIC™ (Enhanced Processed Implanted CMOS) process with ultraviolet-light-erasable EPROM technology. Each output has an output logic macrocell (OLM) configuration allowing for user definition of the output type. This device provides reliable, low-power substitutes for numerous high-performance TTL PLDs with gate complexities between 300 and 800 gates.

The TICPAL22V10Z has 12 dedicated inputs and 10 user-definable outputs. Individual outputs can be programmed as registered or combinational and inverting or noninverting as shown in the OLM diagram. These ten outputs are enabled through the use of individual product terms

The variable product-term distribution on this device removes rigid limitation to a maximum of eight product terms per output. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. The variable allocation of product terms allows for far more complex functions to be implemented in this device than in previously available devices.

With features such as the programmable OLMs and the variable product-term distribution, the TICPAL22V10Z offers quick design and development of custom LSI functions. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs can be implemented with this device.

Design complexity is enhanced by the addition of synchronous set and asynchronous reset product terms. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0 independently of the clock. The output logic level after set or reset will depend on the polarity selected during programming.

Output registers of this device can be preloaded to any desired state during testing, thus allowing for full logical verification during product testing.

The TICPAL22V10Z has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.6. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

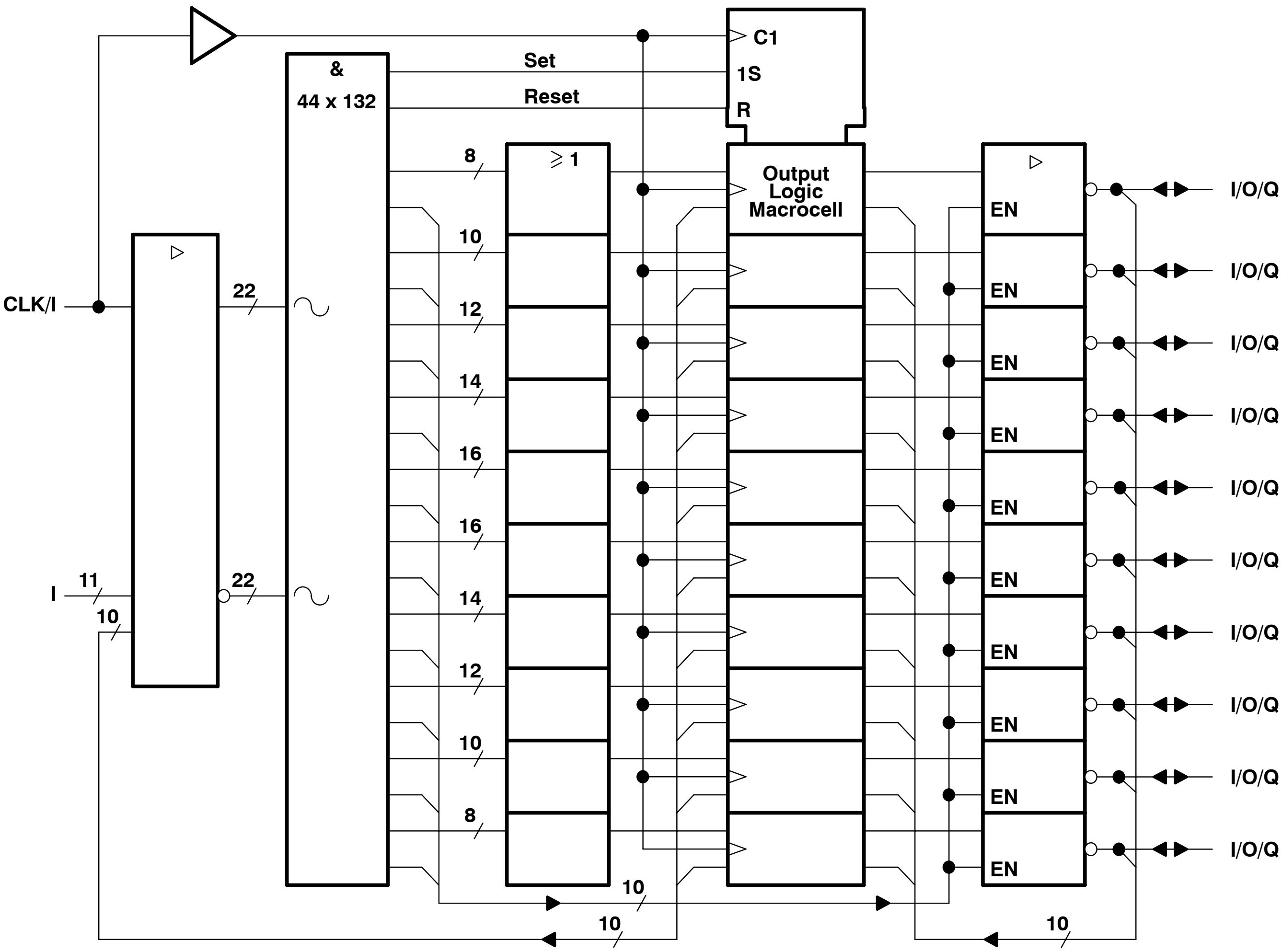
The floating-gate programmable cells allow the devices to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

The TICPAL22V10Z-25C is characterized for operation from 0°C to 75°C. The TICPAL22V10Z-30I is characterized for operation from −40°C to 85°C.

design security

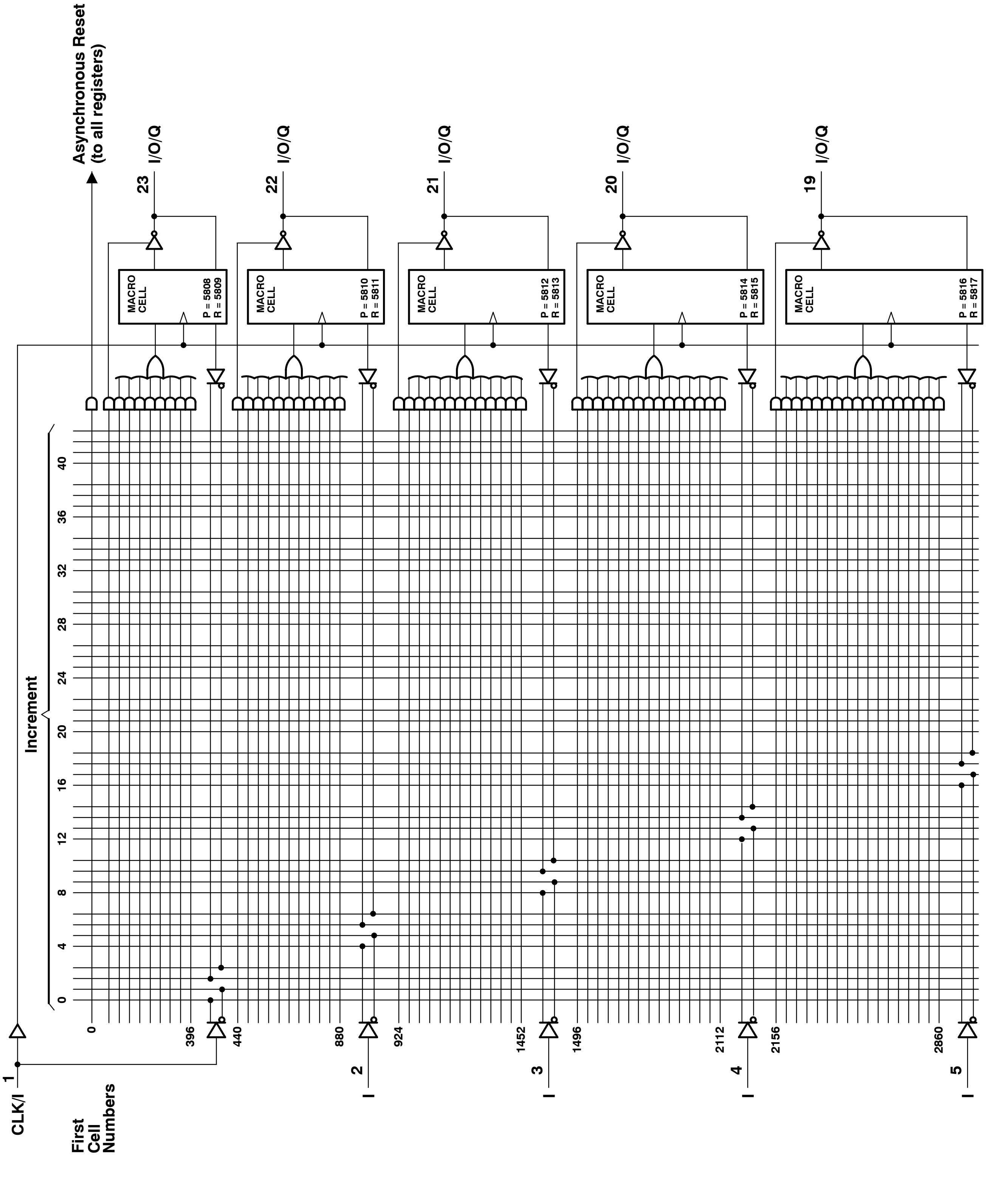
The 'PAL22V10Z contains a programmable design security cell. Programming this cell will disable the read verify and programming circuitry protecting the design from being copied. The security cell is usually programmed after the design is finalized and released to production. A secured device will verify as if every location in the device is programmed. Because programming is accomplished by storing an invisible charge instead of opening a metal link, the '22V10Z cannot be copied by visual inspection. Once a secured device is fully erased, it can be reprogrammed to any desired configuration.

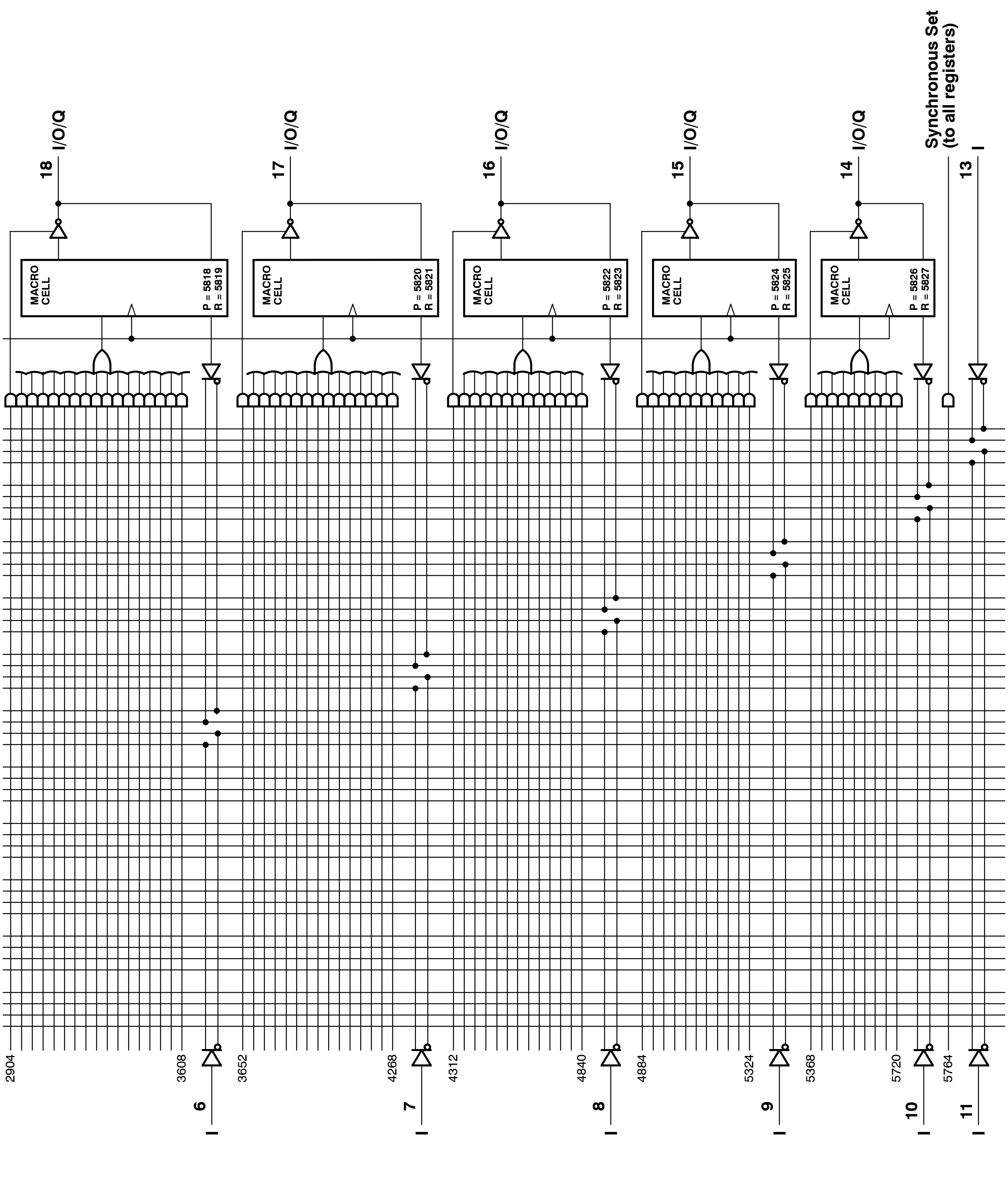
functional block diagram (positive logic)



∿ denotes programmable cell inputs

logic diagram (positive logic)





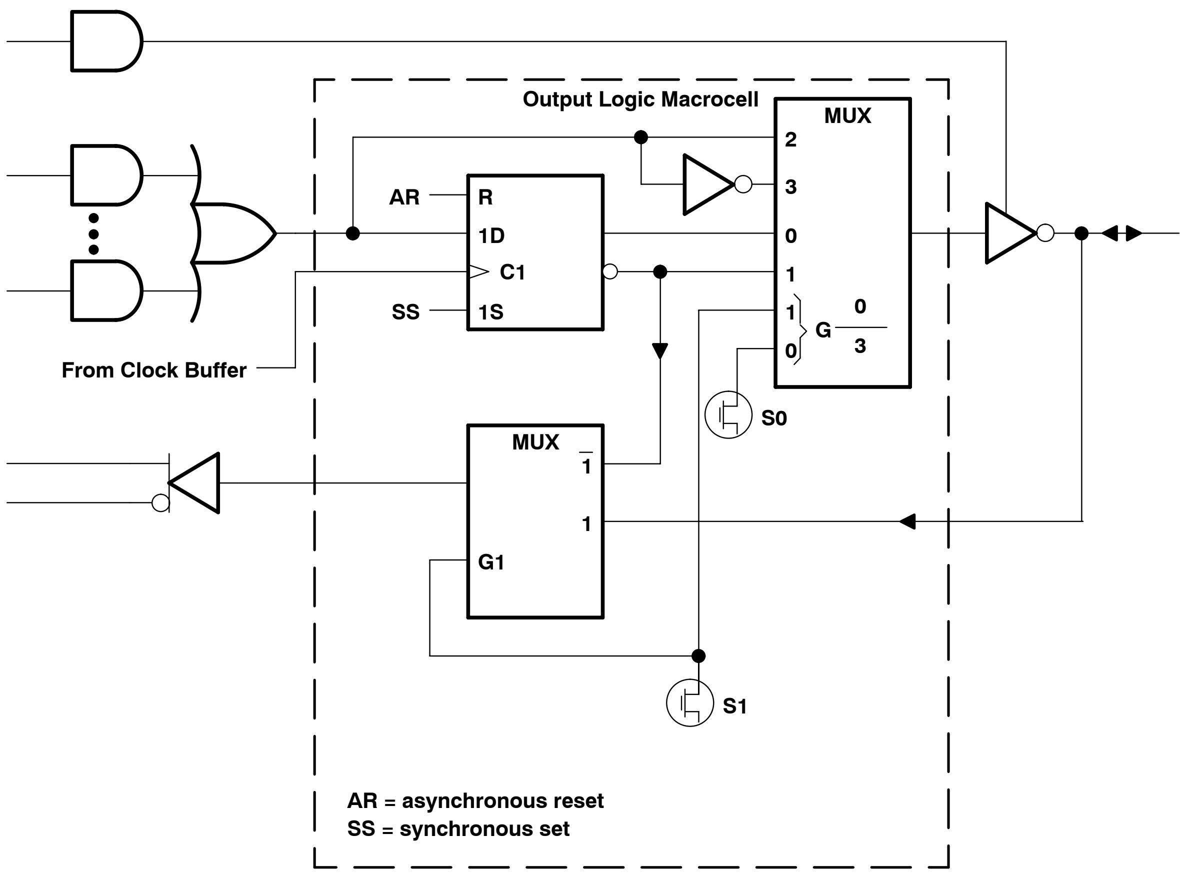
Programmable Cell Number = First Cell Number + Increment
Inside each MACROCELL the (P) cell is the polarity cell and the (R) cell is the register cell.

output logic macrocell (OLM) description

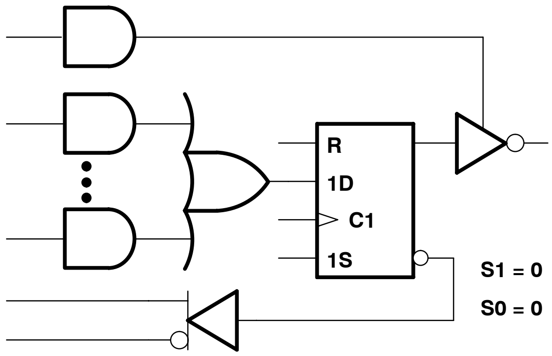
A great amount of architectural flexibility is provided by the user-configurable macrocell output options. The macrocell consists of a D-type flip-flop and two select multiplexers. The D-type flip-flop operates like a standard TTL D-type flip-flop. The input data is latched on the low-to-high transition of the clock input. The Q and $\overline{Q}$ outputs are made available to the output select multiplexer. The asynchronous reset and synchronous set controls are available in all flip-flops.

The select multiplexers are controlled by programmable cells. The combination of these programmable cells will determine which macrocell functions are implemented. It is this user control of the architectural structure that provides the generic flexibility of this device.

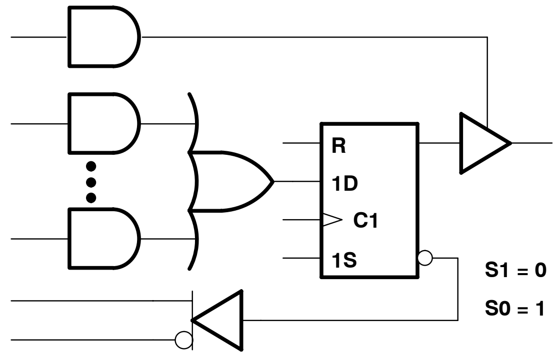
output logic macrocell diagram



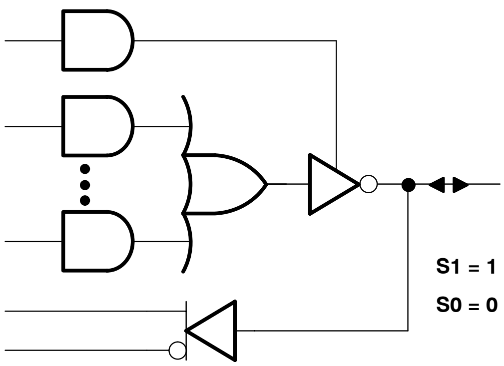
output logic macrocell options (see Figure 1)



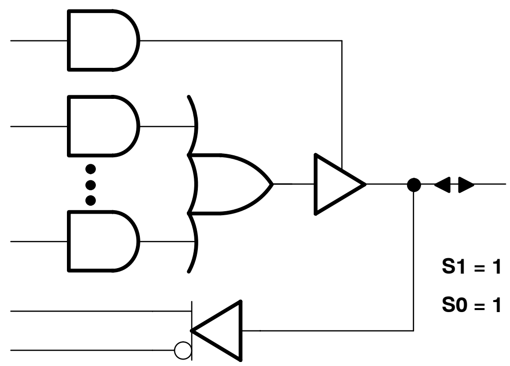
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

CELL SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = erased cell, 1 = programmed cell
S1 and S0 are select-function cells as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ± 40 mA
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FN or NT package .... 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: JTL package .... 300°C
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Driving TTL			–3.2	mA
		Driving CMOS			–4	
I_{OL}	Low-level output current	Driving TTL			16	mA
		Driving CMOS			4	
t_w	Pulse duration	Clock high	10			ns
		Clock low	10			
		Asynchronous reset	20			
t_{su}	Setup time, turbo mode	Input or feedback	17			ns
		Asynchronous reset inactive	20			
		Synchronous preset inactive	20			
t_{su}	Setup time, zero-power mode	Input or feedback	25			ns
		Asynchronous reset inactive	30			
		Synchronous preset inactive	30			
t_h	Hold time	Input or feedback	0			ns
T_A	Operating free-air temperature		0		75	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA for TTL	4	4.8		V
		V_{CC} = 4.75 V,	I_{OH} = −4 mA for CMOS	3.86	4.7		
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA for TTL		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 4 mA for CMOS		0.07	0.4	
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V		0.01	10	µA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.5 V		−0.01	−10	µA
I_{IH}		V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.5 V		−0.01	−10	µA
I_O‡		V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−45	−90	mA
I_{CC}§		V_{CC} = 5.25 V, Outputs open,	V_I = 0 or V_{CC}, Zero-power mode		10	100	µA
C_i	I	V_I = 2 V,	f = 1 MHz		6		pF
	I/O				10		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}¶	Without feedback			50	66		MHz
	With feedback			31.2	55		
t_{pd}	Turbo mode	I, I/O	O, I/O		16	25	ns
	Zero-power mode				21	35	
t_{pd}	Turbo mode	Asynchronous RESET	Q		18	30	ns
	Zero-power mode				23	40	
t_{pd}		CLK↑	Q		10	15	ns
t_{en}	Turbo mode	I, I/O	I, Q, I/O		15	25	ns
	Zero-power mode				20	35	
t_{dis}	Turbo mode	I, I/O	I, Q, I/O		15	25	ns
	Zero-power mode				17	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.
§ Disabled outputs are tied to GND or V_{CC}.
¶ f_{max} (with feedback) $= \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$; f_{max} (without feedback) $= \frac{1}{t_w(\text{high}) + t_w(\text{low})}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ± 20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ± 40 mA
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FN or NT package . . . . 260°C
Operating free-air temperature range . . . . −40°C to 85°C
Storage temperature range . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Driving TTL			−3.2	mA
		Driving CMOS			−4	
I_{OL}	Low-level output current	Driving TTL			16	mA
		Driving CMOS			4	
t_w	Pulse duration	Clock high	12			ns
		Clock low	12			
		Asynchronous reset	30			
t_{su}	Setup time, turbo mode	Input or feedback	22			ns
		Asynchronous reset inactive	25			
		Synchronous preset inactive	25			
t_{su}	Setup time, zero-power mode	Input or feedback	30			ns
		Asynchronous reset inactive	35			
		Synchronous preset inactive	35			
t_h	Hold time	Input or feedback	0			ns
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3.2 mA for TTL	4	4.8		V
		V_{CC} = 4.5 V,	I_{OH} = −4 mA for CMOS	3.86	4.7		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 16 mA for TTL		0.25	0.5	V
		V_{CC} = 4.5 V,	I_{OL} = 4 mA for CMOS		0.07	0.4	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V		0.01	10	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V		−0.01	−10	µA
I_{IH}		V_{CC} = 5.5 V,	V_I = 5.5 V		0.01	10	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.5 V		−0.01	−10	µA
I_O‡		V_{CC} = 5.5 V,	V_O = 0.5 V	−30	−45	−90	mA
I_{CC}§		V_{CC} = 5.5 V, Outputs open,	V_I = 0 or V_{CC}, Zero-power mode		10	100	µA
C_i	I	V_I = 2 V,	f = 1 MHz		6		pF
	I/O				10		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}¶	Without feedback			41.6	66		MHz
	With feedback			23.8	55		
t_{pd}	Turbo mode	I, I/O	O, I/O		16	30	ns
	Zero-power mode				21	40	
t_{pd}	Turbo mode	Asynchronous RESET	Q		18	35	ns
	Zero-power mode				23	45	
t_{pd}		CLK↑	Q		10	20	ns
t_{en}	Turbo mode	I, I/O	I, Q, I/O		15	30	ns
	Zero-power mode				20	40	
t_{dis}	Turbo mode	I, I/O	I, Q, I/O		15	30	ns
	Zero-power mode				17	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.
§ Disabled outputs are tied to GND or V_{CC}.
¶ f_{max} (with feedback) $= \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$; f_{max} (without feedback) $= \frac{1}{t_w(\text{high}) + t_w(\text{low})}$

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to setup through the entire state-machine sequence. Each register is preloaded individually by following the steps given below. The output level depends on the polarity selected during programming.

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 8 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 8 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

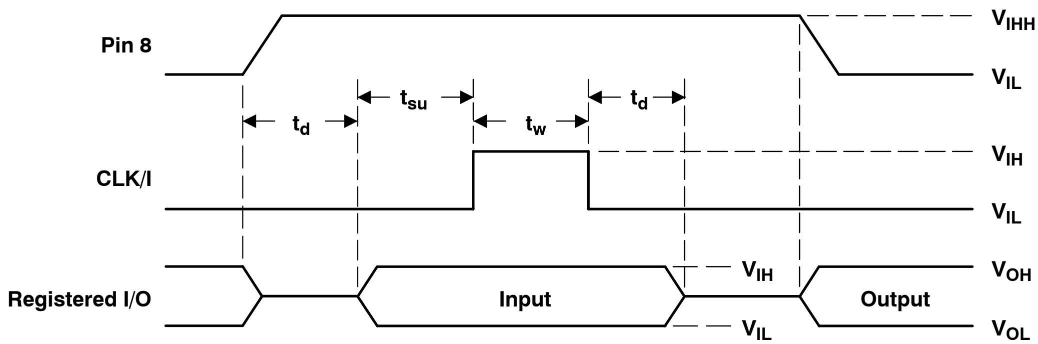


Figure 2. Preload Waveforms

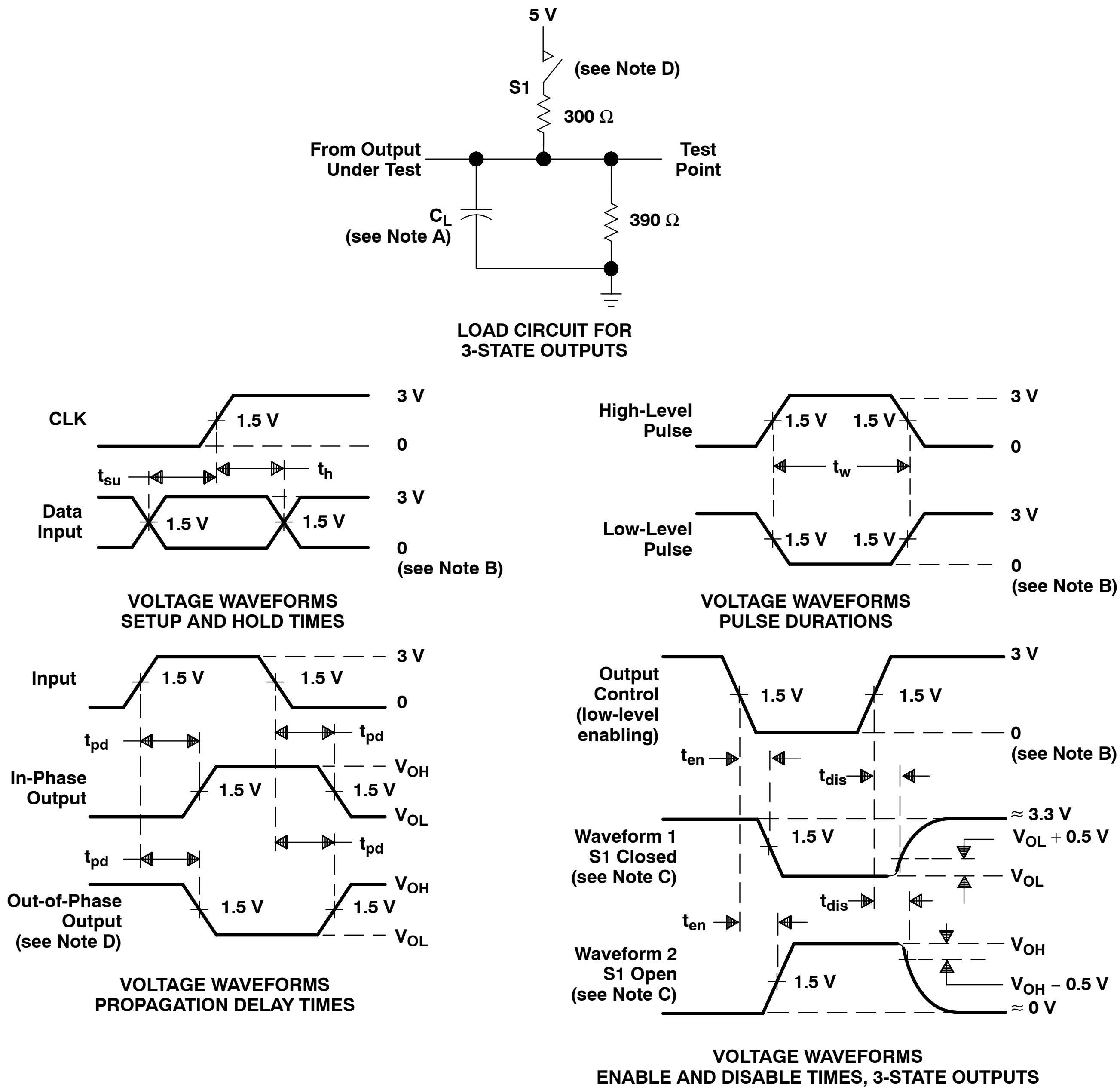
NOTES: 2. Pin numbers shown are for the JTL and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, $t_r = t_f$ = 2 ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

special design features

True CMOS Outputs: Each TICPAL22V10Z output is designed with a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail output switching. This provides direct interface to CMOS logic, memory, or ASIC devices without the need for a pull-up resistor. The CMOS output has 16-mA drive capability, which makes the TICPAL22V10Z an ideal substitute for bipolar PLDs. The electrical characteristics of this device show the output under both CMOS and TTL conditions.

Simultaneous Switching: High-performance CMOS devices often have output glitches on nonswitched outputs when a large number of outputs are switched simultaneously. This glitch is commonly referred to as ”ground bounce” and is most noticeable on outputs held at V_{OL} (low-level output voltage). Ground bounce is caused by the voltage drop across the inductance in the package lead when current is switched (dv α I x di/dt).

One solution is to restrict the number of outputs that can switch simultaneously. Another solution is to change the device pinout such that the ground is located on a low-inductance package pin. TI opted for a third option in order to maintain pinout compatibility and eliminate functional constraints. This option controls the output transistor turn-on characteristics and puts a limit on the instantaneous current available to the load, much like the I_{OS} resistor in a TTL circuit.

Wake-Up Features: The TICPAL22V10Z employs input signal transition detection techniques to power up the device from the standby-power mode. The transition detector monitors all inputs, I/Os, and feedback paths. Whenever a transition is sensed, the detector activates the power-up mode. The device will remain in the power-up mode until the detector senses that the inputs and outputs have been static for about 40 ns; thereafter, the device returns to the standby mode.

Turbo Mode or Zero-Power Mode: When the turbo cell is programmed, the device will be set to the power-up mode. Therefore, the delay associated with its transition detection and power up will be eliminated. This is how the faster propagation delays and shorter setup times are obtained in the turbo mode. The turbo mode and the associated speed increase can be effectively simulated with the turbo cell erased, if a series of adjacent input, I/O, or feedback edges occur with an interval of about 25 ns or less between these adjacent edges. Under these conditions, the TICPAL22V10Z will never have the opportunity to power down due to the frequency of the adjacent edges.

Power Up: The TICPAL22V10Z device configuration bits (power mode, and macrocell configuration) are read at the first input transition after a monotonic power up. When completed, the TICPAL22V10Z is in its designed configuration. The use of an initializing device reset is necessary in applications where registered feedback is used to ensure the TICPAL22V10Z is in a known state at the beginning of system operation.

Power Dissipation: Power dissipation of the TICPAL22V10Z is defined by three contributing factors, and the total power dissipation is the sum of all three.

Standby Power: The product of V_{CC} and the standby I_{CC}. The standby current is the reverse current through the diodes that are reversed biased. This current is very small, and for circuits that remain in static condition for a long time, this low amount of current can become a major performance advantage.

Dynamic Power: The product of V_{CC} and the dynamic current. This dynamic current flows through the device only when the transistors are switching from one logic level to the other. The total dynamic current for the TICPAL22V10Z is dependent upon the users’ configuration of the device and the operating frequency. Output loading can be a source of additional power dissipation.

Interface Power: The product of I_{CC} (interface) and V_{CC}. The total interface power is dependent on the number of inputs at the TTL V_{OH} level. The interface power can be eliminated by the addition of a pull-up resistor.

Even though power dissipation is a function of the user's device configuration and the operating frequency, the TICPAL22V10Z is a lower powered solution than either the quarter-powered or half-powered bipolar devices. The virtually zero standby power feature makes the TICPAL22V10Z the device of choice for low-duty-cycle applications.

programming and erasability

Programming of the TICPAL22V10Z is achieved through floating-gate avalanche injection techniques. The charge trapped on the floating gate remains after power has been removed, allowing for the nonvolatility of the programmed data. The charge can be removed by exposure to light with wavelengths of less than 400 nm (4000 Å). The recommended erasure wavelength is 253.7 nm (2537 Å), with erasure time of 60 to 90 minutes, using a light source with a power rating of 12000 $\mu W/cm^2$ placed within 2.5 cm (one inch) of the device.

The TICPAL22V10Z is designed for programming endurance of 1000 write/erase cycles with a data retention of ten years. To guarantee maximum data retention, the window on the device should be covered by an opaque label. The fluorescent light in a room can erase a unit in three years or, in the case of a direct sunlight, erasure can be complete in one week.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE

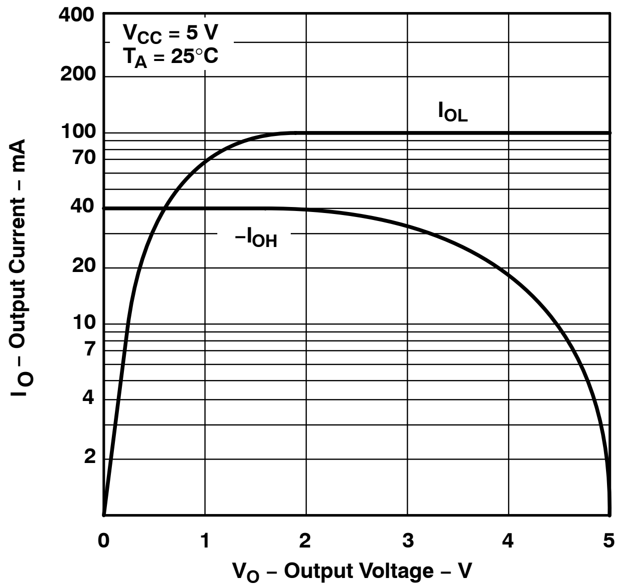


Figure 4

NORMALIZED SUPPLY CURRENT vs FREE-AIR TEMPERATURE (10-BIT COUNTER)

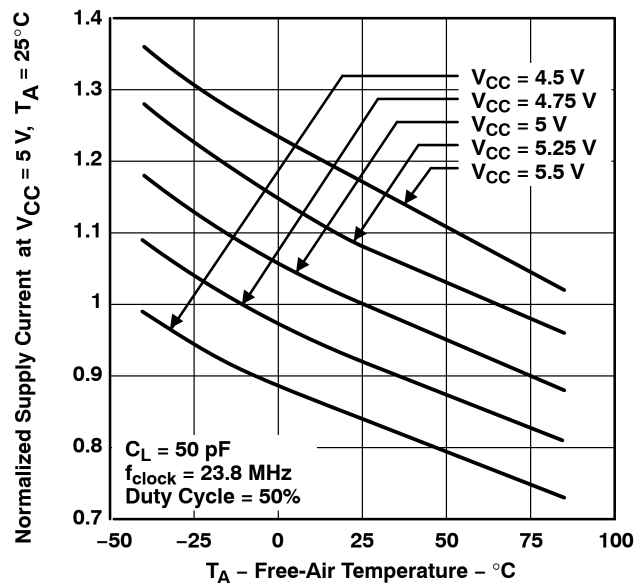


Figure 5

SUPPLY CURRENT vs CLOCK FREQUENCY (10-BIT COUNTER)

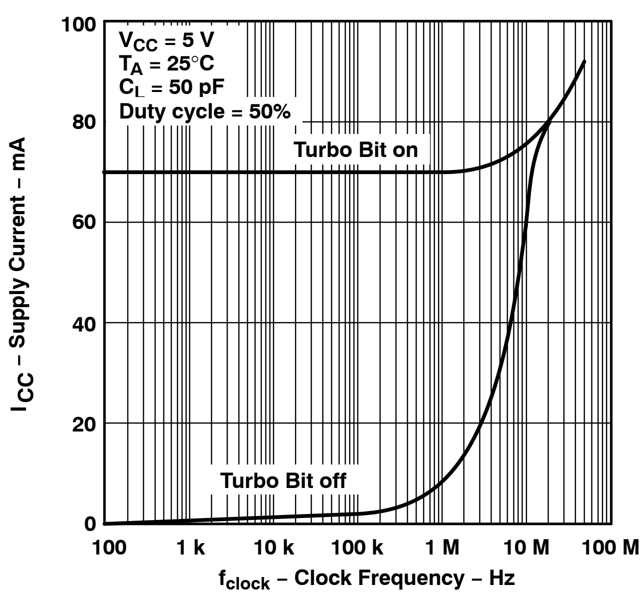


Figure 6

NORMALIZED PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

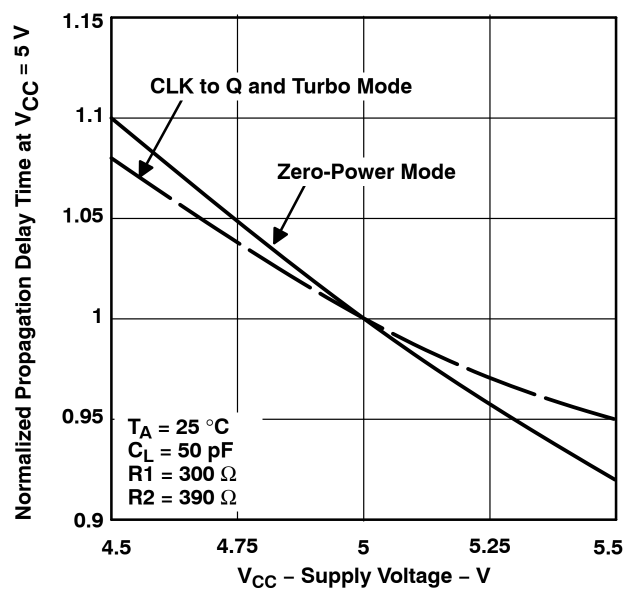


Figure 7

TYPICAL CHARACTERISTICS

NORMALIZED PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

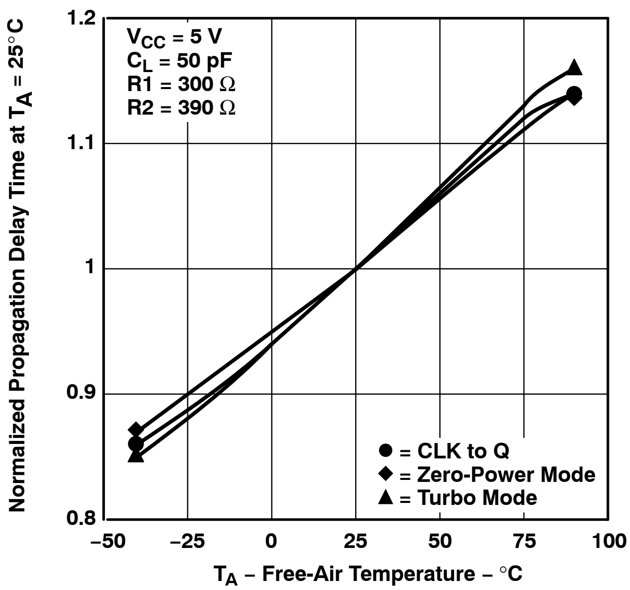


Figure 8

CHANGE IN PROPAGATION DELAY TIME vs LOAD CAPACITANCE

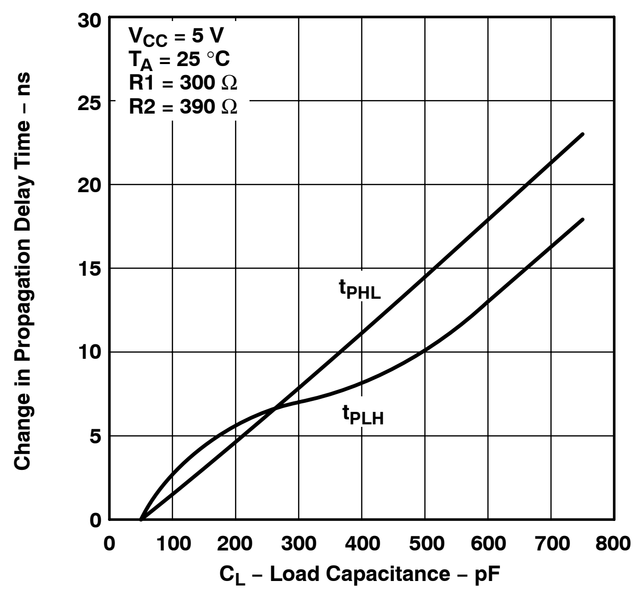


Figure 9

CHANGE IN PROPAGATION DELAY TIME vs NUMBER OF OUTOUTS SWITCHING

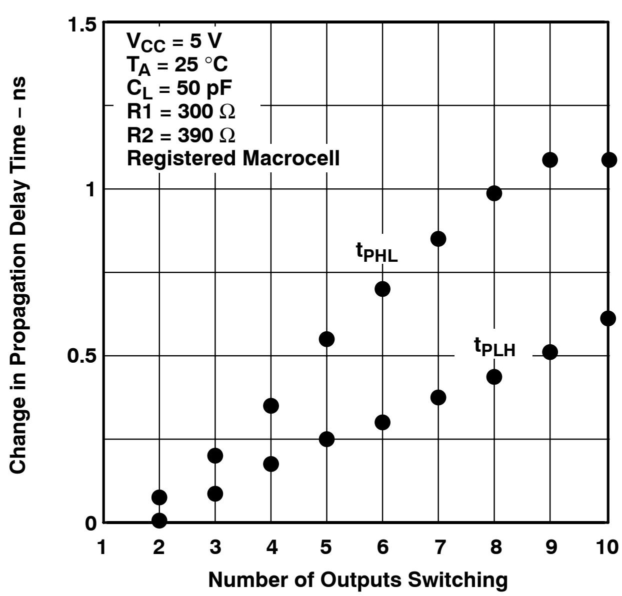


Figure 10

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D0892

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PAL22V10Z-25CJTL	ACTIVE	CDIP	JT	24	15	TBD	A42	N / A for Pkg Type	0 to 75	22V10Z -25CJTL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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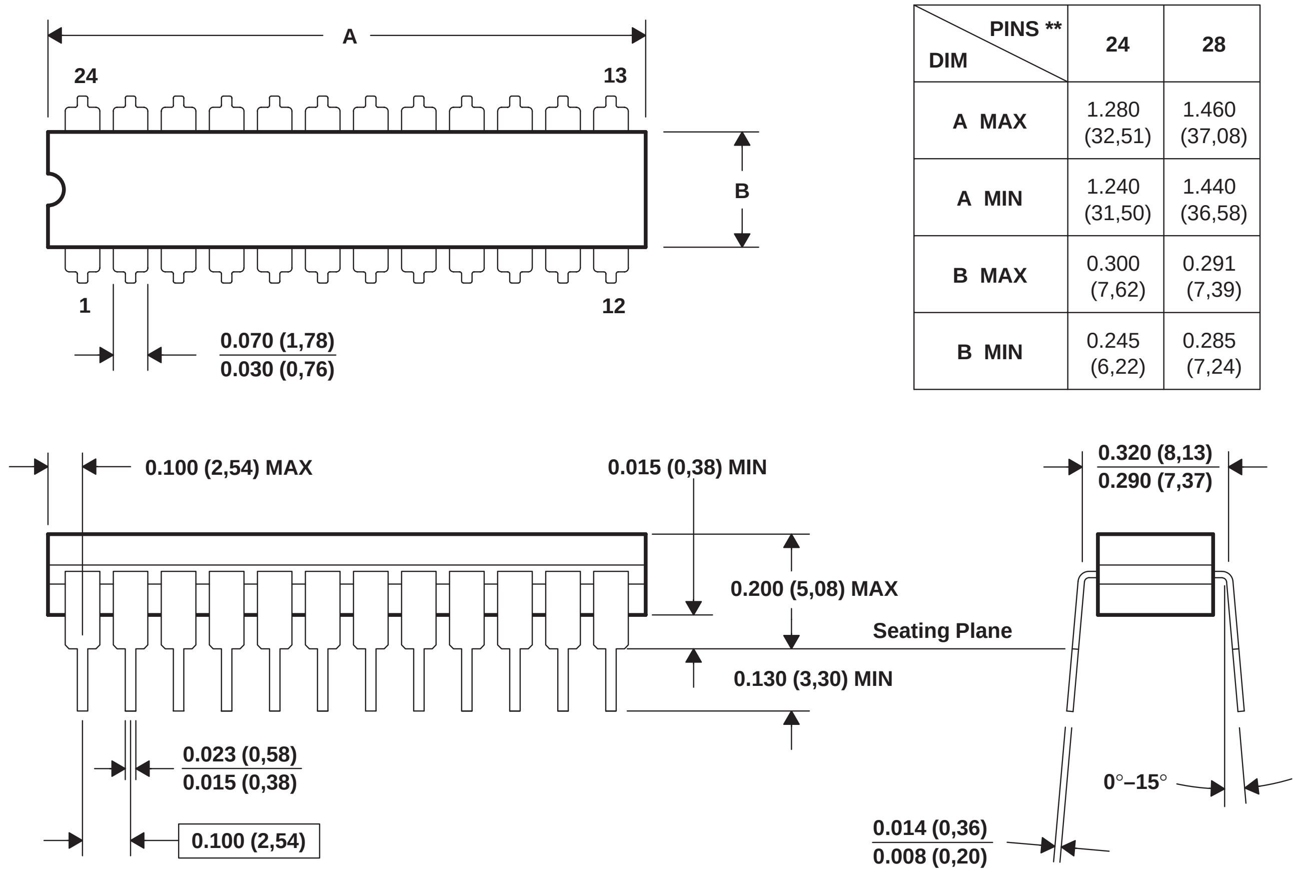
JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN



DIM \ PINS **	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

4040110/C 08/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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