PRODUCT PREVIEW

8XC151SA/SB HIGH-PERFORMANCE CHMOS MICROCONTROLLER

Commercial/Express

- **MCS® 51 Microcontroller Compatible Instruction Set**
- **Pin Compatible with 44-lead PLCC and 40-lead PDIP MCS 51 Sockets**
- **Fast Instruction Pipeline**
- **16-bit Internal Code Fetch**
- **8-bit, Min 2-clock External Code Fetch in Page Mode**
- **User-selectable Configurations:**
  - **— External Wait States (0-3 wait states)**
  - **— Page Mode**
- **64K External Code Memory Space**
- **64K External Data Memory Space**
- **ROM/OTPROM Options: 8 Kbytes (SA), 16 Kbytes (SB) or without ROM/OTPROM**
- **256 Bytes On-Chip RAM**
- **Power Management**
  - **— Idle Mode**
  - **— Powerdown Mode**
- **32 Programmable I/O Lines**
- **Seven Maskable Interrupt Sources with Four Programmable Priority Levels**
- **Three Flexible 16-bit Timer/counters**
- **Hardware Watchdog Timer**
- **Programmable Counter Array**
  - **— High-speed Output**
  - **— Compare/Capture Operation**
  - **— Pulse Width Modulator**
  - **— Watchdog Timer**
- **Programmable Serial I/O Port**
  - **— Framing Error Detection**
  - **— Automatic Address Recognition**
- **High-performance CHMOS Technology**
- **Static Standby to 16-MHz Operation**
- **Package Options (PDIP, PLCC)**

The 8XC151SA/SB has an MCS 51 microcontroller compatible instructon set. It is available in 40-pin PDIP and 44-lead PLCC compatible with the MCS 51 microcontroller. The 8XC151SA/SB has 256 bytes of on-chip RAM and is available in 8/16 Kbytes of on-chip ROM/OTPROM or without ROM/OTPROM. A variety of new features such as programmable wait states, page mode and extended ALE can be selected using the new user-programmable configuration.

March 1996 **Order Number: 272814-001**

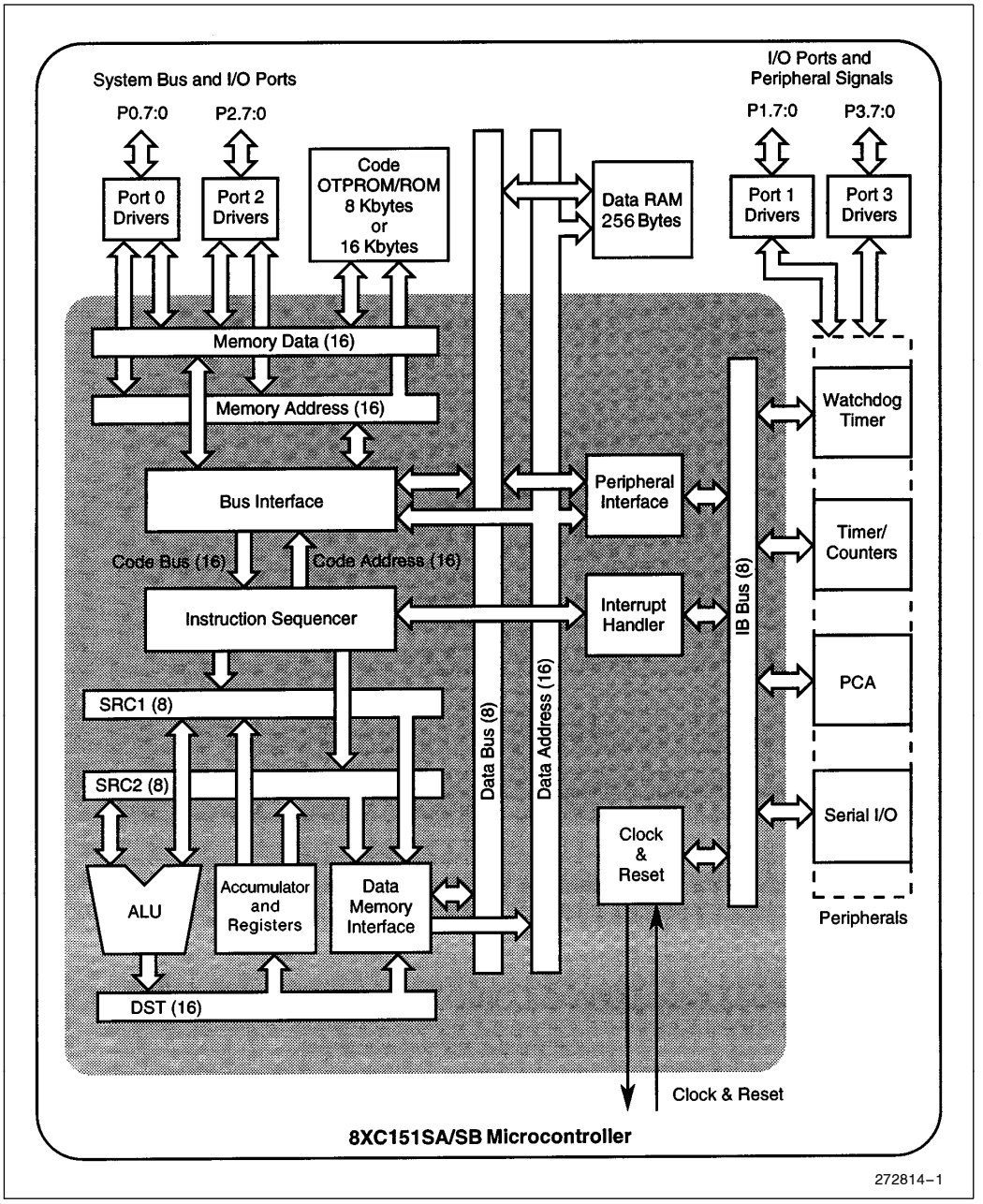


Figure 1. 8XC151SA/SB Block Diagram

TEMPERATURE RANGE

With the commercial (standard) temperature option, the device operates over the temperature range 0°C to +70°C. The express temperature option provides −40°C to +85°C device operation.

PROLIFERATION OPTIONS

Table 1 lists the proliferation options. See Figure 2 for the 8XC151SA/SB family nomenclature.

Table 1. Proliferation Options

8XC151SA/SB (0 MHz–16 MHz; 5V ±10%)	
80C151SB	CPU-only
83C151SA	8K ROM
83C151SB	16K ROM
87C151SA	8K OTPROM
87C151SB	16K OTPROM

PROCESS INFORMATION

This device is manufactured on a complimentary high-performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 2. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
44-Lead PLCC	46°C/W	16°C/W
40-Pin PDIP	45°C/W	16°C/W

PACKAGE OPTIONS

Table 3 lists the 8XC151SA/SB packages.

Table 3. Package Information

Pkg.	Definition	Temperature
N	44-Lead PLCC	0°C to +70°C
P	40-Pin Plastic DIP	0°C to +70°C
TN	44-Lead PLCC	−40°C to +85°C
TP	40-Pin Plastic DIP	−40°C to +85°C

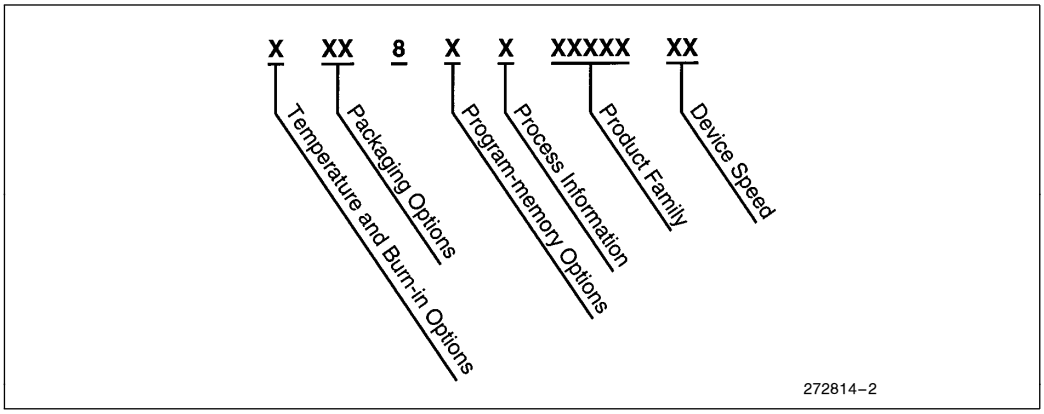


Figure 2. The 8XC151SA/SB Family Nomenclature

Table 4. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
	T	Express operating temperature range (−40°C to 85°C) with Intel standard burn-in.
Packaging Options	N	44-lead Plastic Leaded Chip Carrier (PLCC)
	P	40-pin Plastic Dual In-line Package (PDIP)
Program Memory Options	0	Without ROM/OTPROM
	3	ROM
	7	User programmable OTPROM
Process Information	C	CHMOS
Product Family	151	8-bit controller architecture
Device Memory Options	SA/SB	256 bytes RAM/8/16 Kbyte ROM/OTPROM or without ROM/OTPROM
Device Speed	16	External clock frequency

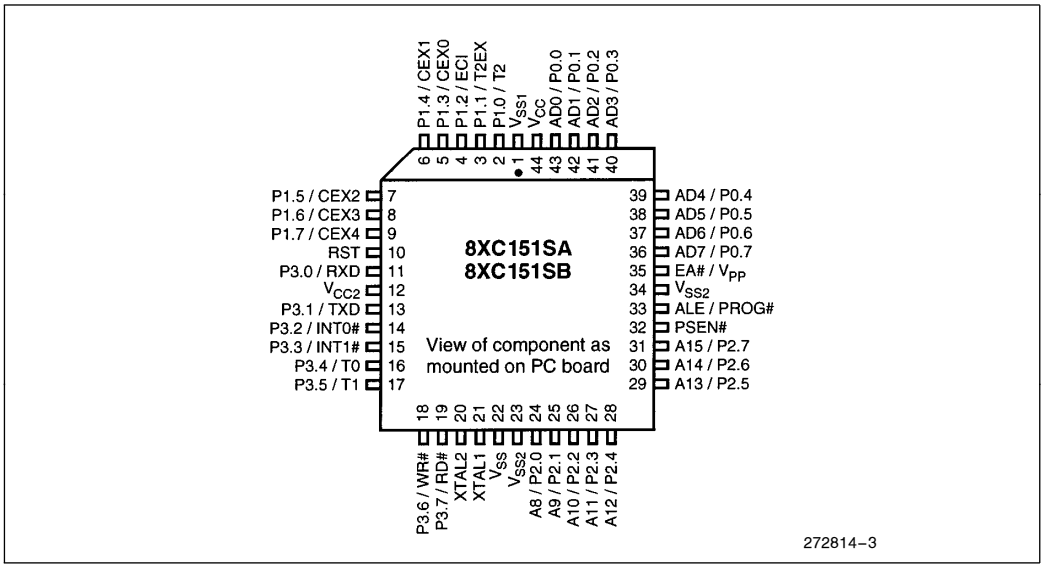


Figure 3. 8XC151SA/SB 44-Lead PLCC Package

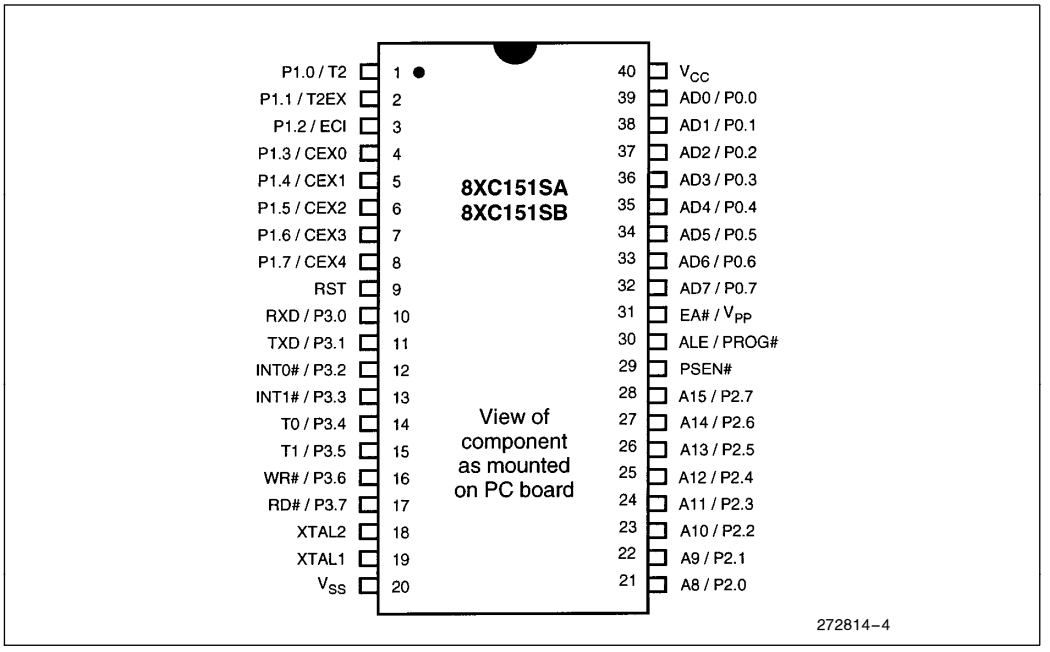


Figure 4. 8XC151SA/SB 40-Pin PDIP and Ceramic DIP Packages

Table 5. PLCC/DIP Signal Assignment Arranged by Functional Categories

Address & Data		
Name	**PLCC**	**DIP**
AD0/P0.0	43	39
AD1/P0.1	42	38
AD2/P0.2	41	37
AD3/P0.3	40	36
AD4/P0.4	39	35
AD5/P0.5	38	34
AD6/P0.6	37	33
AD7/P0.7	36	32
A8/P2.0	24	21
A9/P2.1	25	22
A10/P2.2	26	23
A11/P2.3	27	24
A12/P2.4	28	25
A13/P2.5	29	26
A14/P2.6	30	27
A15/P2.7	31	28

Processsor Control		
Name	**PLCC**	**DIP**
P3.2/INT0#	14	12
P3.3/INT1#	15	13
EA#/V_{PP}	35	31
RST	10	9
XTAL1	21	18
XTAL2	20	19

Input/Output		
Name	**PLCC**	**DIP**
P1.0/T2	2	1
P1.1/T2EX	3	2
P1.2/ECI	4	3
P1.3/CEX0	5	4
P1.4/CEX1	6	5
P1.5/CEX2	7	6
P1.6/CEX3	8	7
P1.7/CEX4	9	8
P3.0/RXD	11	10
P3.1/TXD	13	11
P3.4/T0	16	14
P3.5/T1	17	15

Power & Ground		
Name	**PLCC**	**DIP**
V_{CC}	44	40
V_{CC2}	12	—
V_{SS}	22	20
V_{SS1}	1	—
V_{SS2}	23, 34	—
EA#/V_{PP}	35	31

Bus Control & Status		
Name	**PLCC**	**DIP**
P3.6/WR#	18	16
P3.7/RD#	19	17
ALE/PROG#	33	30
PSEN#	32	29

Table 6. Signal Assignments Arranged by Package Number

PLCC	DIP	Name
1	—	V_{SS1}
2	1	P1.0/T2
3	2	P1.1/T2EX
4	3	P1.2/ECI
5	4	P1.3/CEX0
6	5	P1.4/CEX1
7	6	P1.5/CEX2
8	7	P1.6/CEX3
9	8	P1.7/CEX4
10	9	RST
11	10	P3.0/RXD
12	—	V_{CC2}
13	11	P3.1/TXD
14	12	P3.2/INT0#
15	13	P3.3/INT1#
16	14	P3.4/T0
17	15	P3.5/T1
18	16	P3.6/WR#
19	17	P3.7/RD#
20	18	XTAL2
21	19	XTAL1
22	20	V_{SS}

PLCC	DIP	Name
23	—	V_{SS2}
24	21	A8/P2.0
25	22	A9/P2.1
26	23	A10/P2.2
27	24	A11/P2.3
28	25	A12/P2.4
29	26	A13/P2.5
30	27	A14/P2.6
31	28	A15/P2.7
32	29	PSEN#
33	30	ALE/PROG#
34	—	V_{SS2}
35	31	EA#/V_{pp}
36	32	AD7/P0.7
37	33	AD6/P0.6
38	34	AD5/P0.5
39	35	AD4/P0.4
40	36	AD3/P0.3
41	37	AD2/P0.2
42	38	AD1/P0.1
43	39	AD0/P0.0
44	40	V_{CC}

SIGNAL DESCRIPTIONS

Table 7. Signal Descriptions

Signal Name	Type	Description	Multiplexed With
A15:8†	O	**Address Lines.** Upper address lines for the external bus.	P2.7:0
AD7:0†	I/O	**Address/Data Lines.** Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable.** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	PROG#
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Pins.** These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.6:3 P1.7
EA#	I	**External Access.** Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is to on-chip ROM/OTPROM if the address is within the range of the on-chip ROM/OTPROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM/OTPROM, EA# must be strapped to ground.	V_{PP}
ECI	I	**PCA External Clock Input.** External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1.** These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
PROG#	I	**Programming Pulse.** The programming pulse is applied to this pin for programming the on-chip OTPROM.	ALE
P0.7:0	I/O	**Port 0.** This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1.** This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI CEX3:0 CEX4
P2.7:0	I/O	**Port 2.** This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3.** This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#
PSEN#	O	**Program Store Enable.** Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte UCONFIG0.	—
RD#	O	**Read.** Read signal output to external data memory.	P3.7
RST	I	**Reset.** Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this pin and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data.** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
T1:0	I	**Timer 1:0 External Clock Inputs.** When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output.** For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input.** In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data.** TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
V_{CC}	PWR	**Supply Voltage.** Connect this pin to the +5V supply voltage.	—
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this pin to the +5V supply voltage is recommended. However, when using the 8XC151SA/SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—
V_{PP}	I	**Programming Supply Voltage.** The programming supply voltage is applied to this pin for programming the on-chip OTPROM.	EA#

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
V_{SS}	GND	**Circuit Ground.** Connect this pin to ground.	—
V_{SS1}	GND	**Secondary Ground.** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC151SA/SB as a pin-for-pin replacement for the 8XC51BH, V_{SS1} can be unconnected without loss of compatibility. (Not available on DIP)	
V_{SS2}	GND	**Secondary Ground 2.** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC151SA/SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	
WR#	O	**Write.** Write signal output to external memory.	P3.6
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier.** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier.** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	—

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

ELECTRICAL CHARACTERISTICS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias:
- Commercial . . . . . 0°C to +70°C
- Express . . . . . −40°C to +85°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on EA#/V_{PP} Pin to V_{SS} . . . . . 0V to +13.0V

Voltage on Any other Pin to V_{SS} . . . −0.5V to +6.5V

I_{OL} per I/O Pin . . . . . 15 mA

Power Dissipation 1.5W

NOTE:

Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias):
- Commercial . . . . . 0°C to +70°C
- Express . . . . . −40°C to +85°C

V_{CC} (Digital Supply Voltage) . . . . . 4.5V to 5.5V

V_{SS} 0V

DC CHARACTERISTICS

Parameter values apply to all devices unless otherwise indicated.

Table 8. DC Characteristics at V_{CC} = 4.5V − 5.5V

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	−0.5		$0.2V_{CC} - 0.1$	V	
V_{IL1}	Input Low Voltage (EA#)	0		$0.2V_{CC} - 0.3$	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 μA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (Note 1, Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (Note 1, Note 2)
V_{OH}	Output High Voltage (Port 1, 2, 3, ALE, PSEN#)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	I_{OH} = −10 μA I_{OH} = −30 μA I_{OH} = −60 μA (Note 3)

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   port 0 26 mA
   ports 1–3 15 mA
   Maximum Total I_{OL} for
   all output pins 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.

Table 8. DC Characteristics at V_{CC} = 4.5V − 5.5V (Continued)

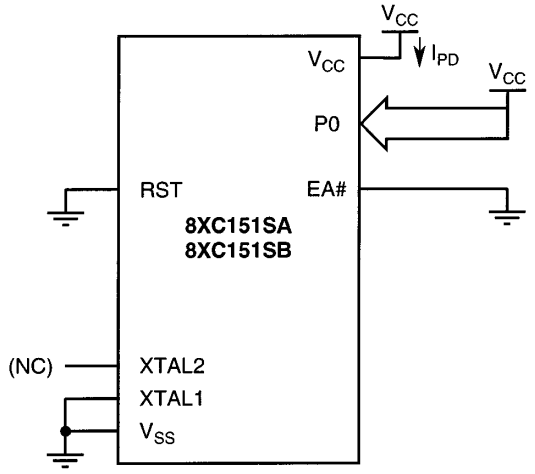
Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7.0 mA
V_{OH2}	Output High Voltage (Port 2 in External Address during Page Mode)	V_{CC} −0.3 V_{CC} − 0.7 V_{CC} − 1.5			V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45< V_{IN} < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Port 1, 2, 3)			−650	μA	V_{IN} = 2.0V
R_{RST}	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10 (Note 4)		pF	F_{OSC} = 16 MHz T_A = 25°C
I_{PD}	Powerdown Current		10 (Note 4)	< 20	μA	
I_{DL}	Idle Mode Current		13 (Note 4)	20	mA	F_{OSC} = 16 MHz
I_{CC}	Operating Current		71 (Note 4)	85	mA	F_{OSC} = 16 MHz

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   port 0 26 mA
   ports 1–3 15 mA
   Maximum Total I_{OL} for all output pins 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.



All other 8XC151SA/SB pins are unconnected.

Figure 5. I_{PD} Test Condition, Powerdown Mode, V_{CC} = 2.0V − 5.5V

AC Characteristics

Table 8 lists AC timing parameters for the 8XC151SA/SB with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and/or by extending ALE. In the table, Notes 3 and 5 mark parameters affected by an ALE wait state, and Notes 4 and 5 mark parameters affected by a PSEN#/RD#/WR# wait state.

Figures 5–11 show the bus cycles with the timing parameters.

Table 9. AC Characteristics (Capacitive Loading = 50 pF)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
F_{OSC}	XTAL1 Frequency	N/A	N/A	0	16	MHz
T_{OSC}	$1/F_{OSC}$ @ 12 MHz @ 16 MHz	N/A	N/A	 83.3 62.5		ns
T_{LHLL}	ALE Pulse Width @ 12 MHz @ 16 MHz	 68.3 47.5		 (1 + 2M) T_{OSC} − 15		ns (3)
T_{AVLL}	Address Valid to ALE Low @ 12 MHz @ 16 MHz	 58.3 37.5		 (1 + 2M) T_{OSC} − 25		ns (3)
T_{LLAX}	Address Hold after ALE Low @ 12 MHz @ 16 MHz	 10 10		 10		ns
T_{RLRH} (2)	RD# or PSEN# Pulse Width @ 12 MHz @ 16 MHz	 151.6 110		 2(1 + N) T_{OSC} − 15		ns (4)
T_{WLWH}	WR# Pulse Width @ 12 MHz @ 16 MHz	 151.6 110		 2(1 + N) T_{OSC} − 15		ns (4)
T_{LLRL} (2)	ALE Low to RD# or PSEN# Low @ 12 MHz @ 16 MHz	 58.3 37.5		 Tosc − 25		ns
T_{LHAX}	ALE High to Address Hold @ 12 MHz @ 16 MHz	 83.3 62.5		 (1 + 2M) T_{OSC}		ns (3)

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M = Number of wait states (0 or 1) for ALE.
4. In the formula, N = Number of wait states (0, 1, 2, or 3) for RD#/PSEN#/WR#.
5. ''Typical'' specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
T_{RLDV} (2)	RD#/PSEN# Low to valid Data/Instruction In @ 12 MHz @ 16 MHz		 111.6 70		 2(1 + N) T_{OSC} − 55	ns (4)
T_{RHDX} (2)	RD#/PSEN# Data/Instruction Hold after RD# and PSEN# High	0		0		ns
T_{RLAZ} (2)	RD#/PSEN# Low to Address Float	Typ. = 0 (5)	2	Typ. = 0 (5)	2	ns
T_{RHDZ1}	Instruction Float after RD#/PSEN# High @ 12 MHz @ 16 MHz		 0 0		 0	ns
T_{RHDZ2}	Data Float after RD#/PSEN# High @ 12 MHz @ 16 MHz		 151.6 110		 $2T_{OSC}$ −15	ns
T_{RHLH1}	RD#/PSEN# High to ALE High (Instruction) @ 12 MHz @ 16 MHz	 0 0		 0		ns
T_{RHLH2}	RD#/PSEN# High to ALE High (Data) @ 12 MHz @ 16 MHz	 156.6 115		 $2T_{OSC}$ − 10		ns
T_{WHLH}	WR# High to ALE High @ 12 MHz @ 16 MHz	 166.6 125		 $2T_{OSC}$		ns
T_{AVDV1}	Address (P0) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 253.2 170		 4(1 + M/2) T_{OSC} − 80	ns (3)
T_{AVDV2}	Address (P2) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 268.2 185		 4(1 + M/2) T_{OSC} − 65	ns (3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In @ 12 MHz @ 16 MHz		 116.6 75		 $2T_{OSC}$ −50	ns

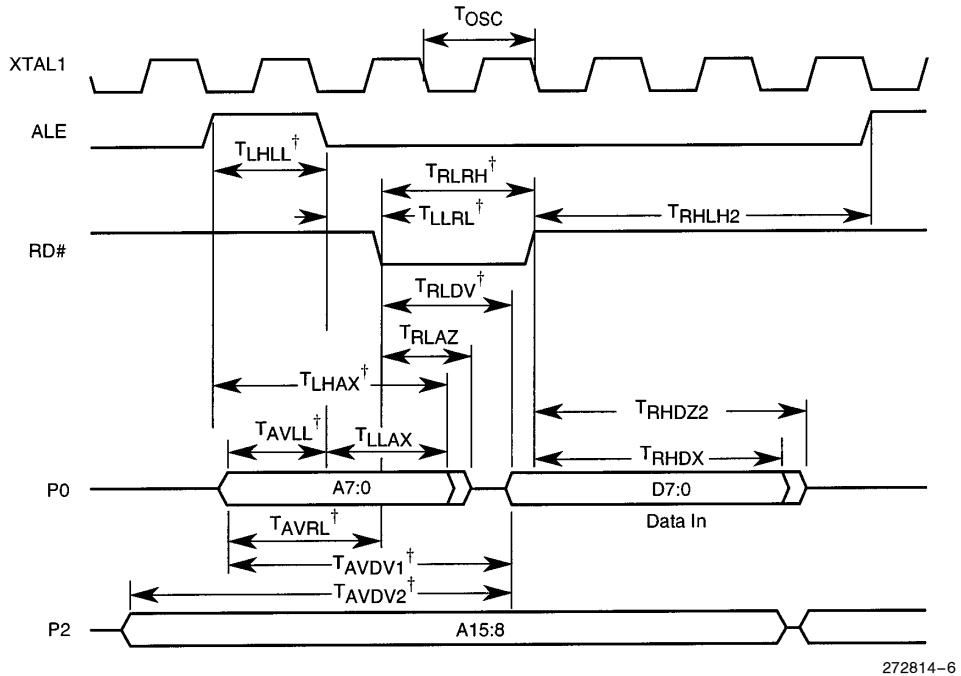
NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M = Number of wait states (0 or 1) for ALE.
4. In the formula, N = Number of wait states (0, 1, 2, or 3) for RD#/PSEN#/WR#.
5. ''Typical'' specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
T_{AVRL} (2)	Address Valid to RD#/PSEN# Low @ 12 MHz @ 16 MHz	 126.6 85		 2(1+M) T_{OSC} − 40		ns (3)
T_{AVWL1}	Address (P0) Valid to WR# Low @ 12 MHz @ 16 MHz	 126.6 85		 2(1+M) T_{OSC} − 40		ns (3)
T_{AVWL2}	Address (P2) Valid to WR# Low @ 12 MHz @ 16 MHz	 141.6 100		 2(1+M) T_{OSC} −25		ns (3)
T_{WHQX}	Data Hold after WR# High @ 12 MHz @ 16 MHz	 58.3 37.5		 T_{OSC} − 25		ns
T_{QVWH}	Data Valid to WR# High @ 12 MHz @ 16 MHz	 146.6 105		 2(1+N) T_{OSC} − 20		ns (4)
T_{WHAX}	WR# High to Address Hold @ 12 MHz @ 16 MHz	 146.6 105		 $2T_{OSC}$ − 20		ns

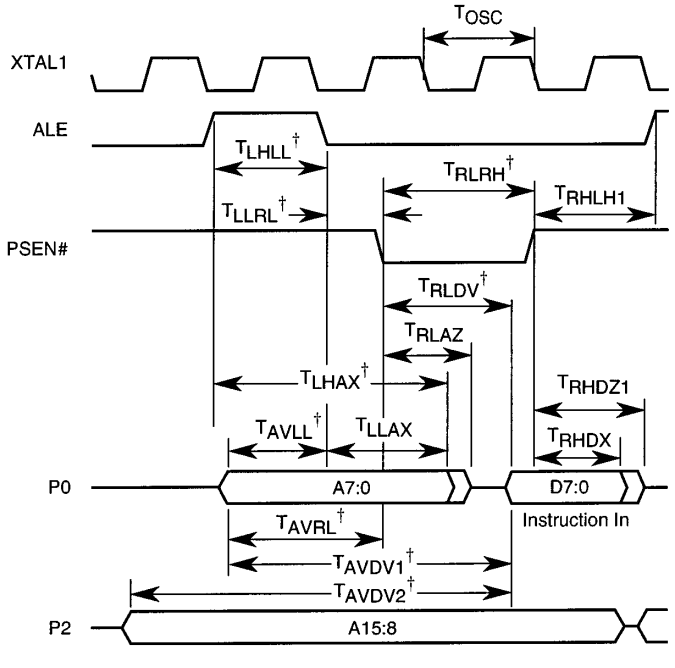
NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M = Number of wait states (0 or 1) for ALE.
4. In the formula, N = Number of wait states (0, 1, 2, or 3) for RD#/PSEN#/WR#.
5. ''Typical'' specifications are untested and not guaranteed.

SYSTEM BUS TIMINGS



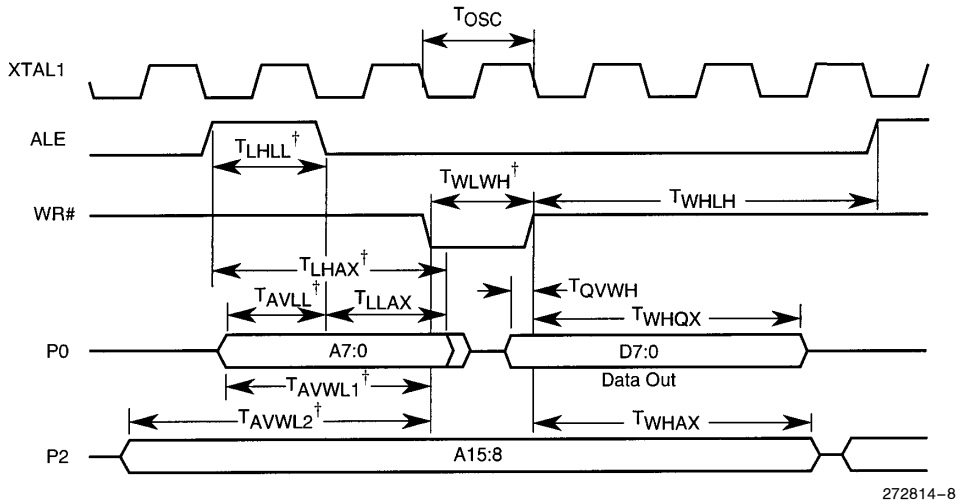
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 6. External Read Data Bus Cycle in Nonpage Mode



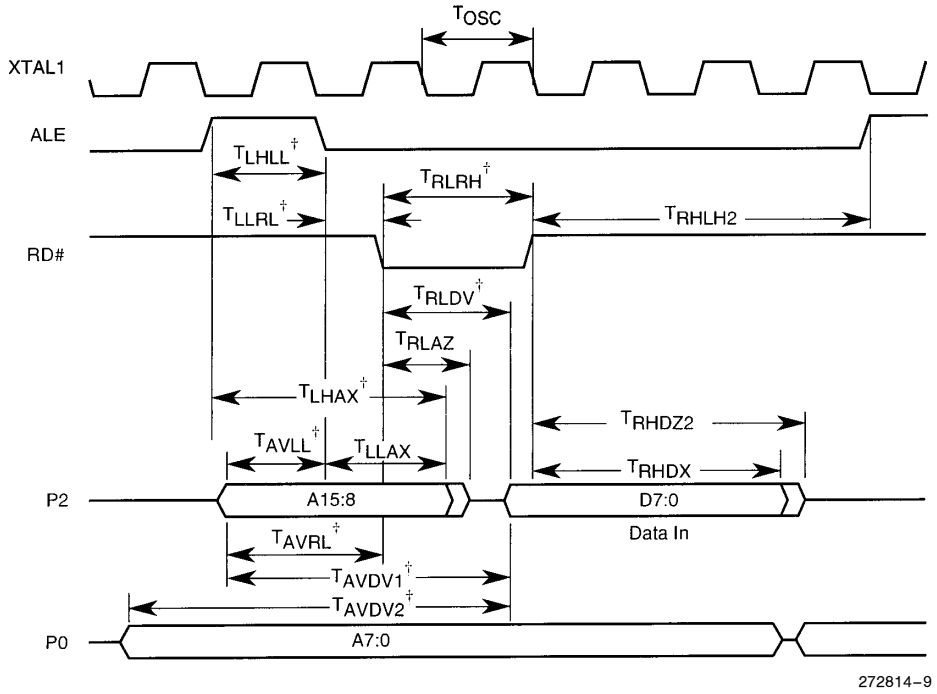
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 7. External Instruction Bus Cycle in Nonpage Mode



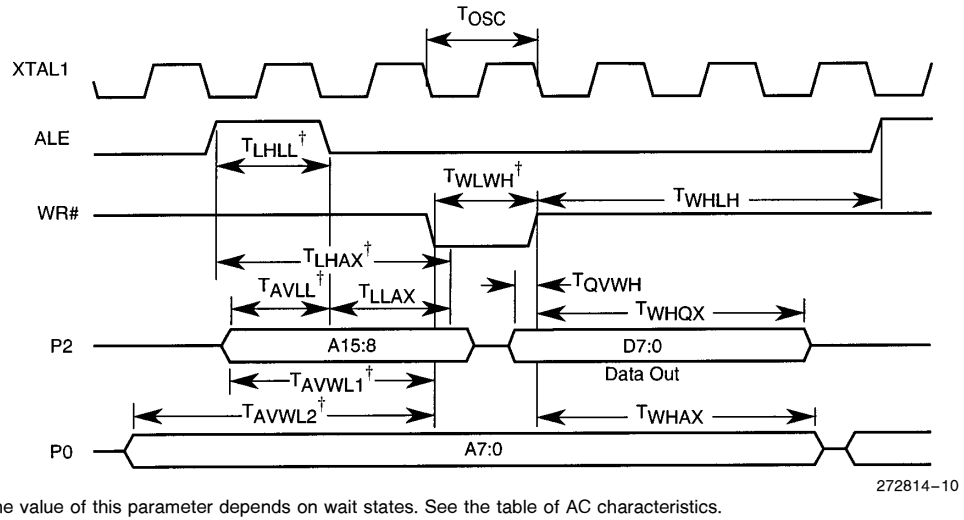
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 8. External Write Data Bus Cycle in Nonpage Mode



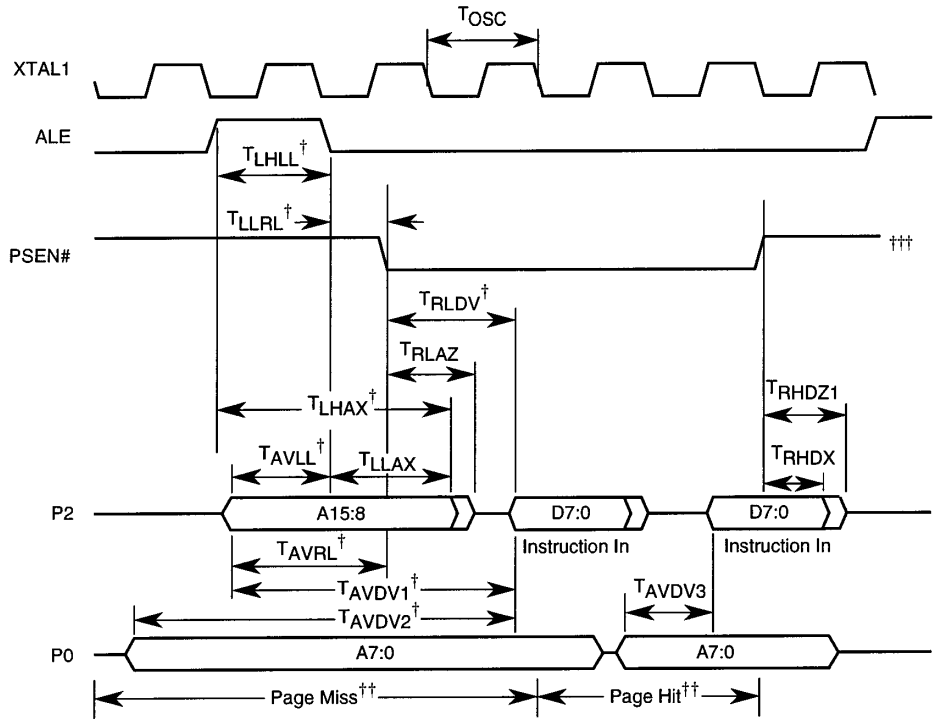
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 9. External Read Data Bus Cycle in Page Mode



†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 10. External Write Data Bus Cycle in Page Mode



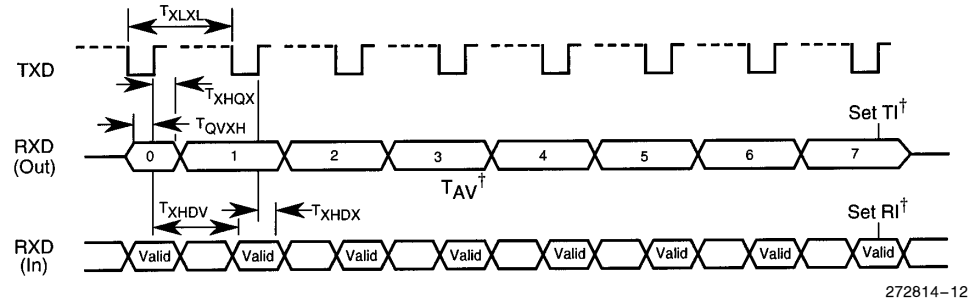
† The value of this parameter depends on wait states. See the table of AC characteristics.
†† A page hit (i.e., a code fetch to the same 256-byte ''page'' as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).
††† During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

Figure 11. External Instruction Bus Cycle in Page Mode

AC Characteristics—Serial Port, Shift Register Mode

Table 10. Serial Port Timing Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns



† TI and RI are set during S1P1 of the peripheral cycle following the shift of the eighth bit.

Figure 12. Serial Port Waveform —Shift Register Mode

External Clock Drive

Table 11. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency (F_{OSC})		16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

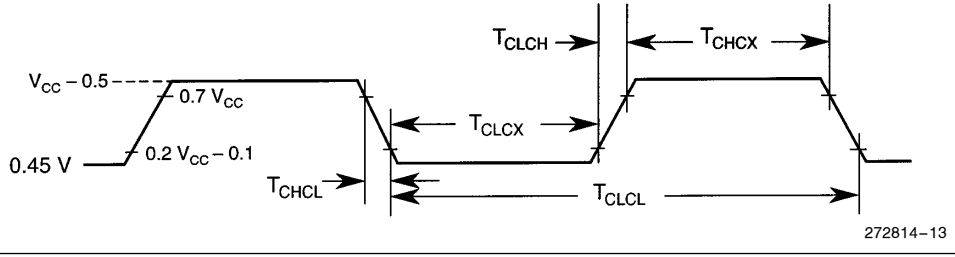
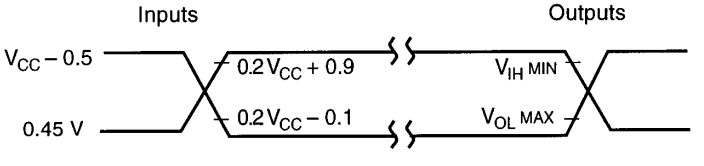
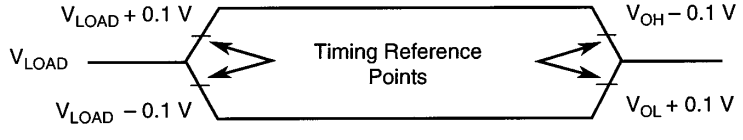


Figure 13. External Clock Drive Waveforms



AC inputs during testing are driven at V_{CC} – 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at a min of V_{IH} for logic 1 and V_{OL} for a logic 0.

Figure 14. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

Figure 15. Float Waveforms

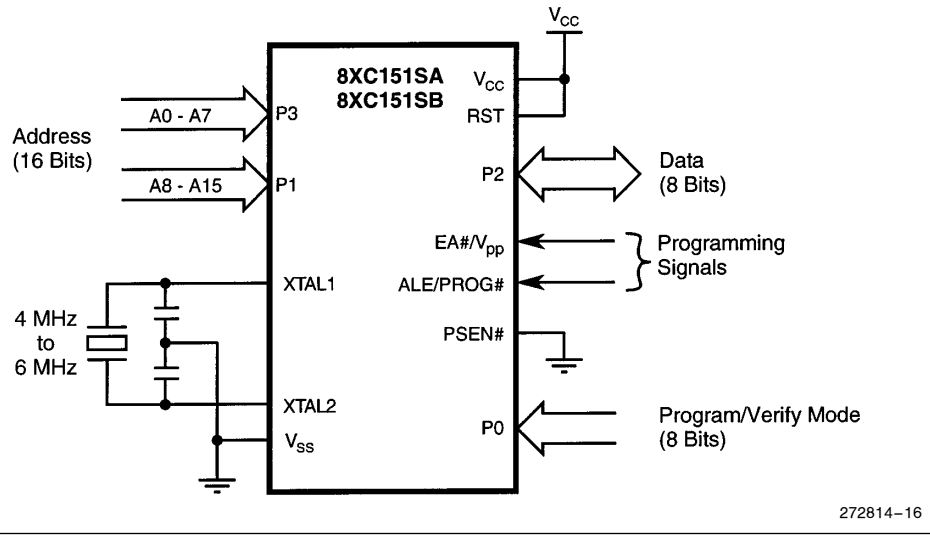


Figure 16. Setup for Programming and Verifying Nonvolatile Memory

PROGRAMMING AND VERIFYING NONVOLATILE MEMORY

The 87C151SA/SB has several areas of nonvolatile memory that can be programmed and/or verified: on-chip code memory (8/16 Kbytes), lock bits (3 bits), encryption array (128 bytes), and signature bytes (3 bytes).

Figure 16 shows the setup for programming and/or verifying the nonvolatile memory. Table 11 lists the programming and verification operations and indicates which operations apply to the different versions of the 87C151SA/SB. It also specifies the signals on the programming input (PROG#) and the ports. The ROM/OTPROM mode (port 0) specifies the operation (program or verify) and the base address of the memory area. The addresses (ports 1 and 3) are relative to the base address. (On-chip memory for a 16-Kbyte ROM/OTPROM device is located at address range 0000H–3FFFH. The other areas of the ROM/OTPROM are outside the memory address space and are accessible only during programming and verification.)

Information in Figures 17 and 18 define the configuration bits. Figure 19 shows the waveforms for the programming and verification cycles, and Table 12 lists the timing specifications. The signature bytes of the 83C151SA/SB ROM versions and the 87C151SA/SB OTPROM versions are factory programmed. Table 13 lists the addresses and the contents of the signature bytes.

Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.

NOTE:

The V_{PP} source in Figure 16 must be well regulated and free of glitches. The voltage on the V_{PP} pin must not exceed the specified maximum, even under transient conditions.

Table 12. Programming and Verification Modes Mode

Mode	8XC151SA/SB		PROG#	P0	P2	Addresses P1 (high), P3 (low)	Notes
	X = 7	X = 3					
Program On-Chip Code Memory	Y		5 Pulses	68H	Data	0000H–3FFFH (16K) 0000H–1FFFH (8K)	1
Verify On-Chip Code Memory	Y	Y	High	28H	Data	0000H–3FFFH (16K) 0000H–1FFFH (8K)	
Program Configuration Bytes							2
Verify Configuration Bytes							2
Program Lock Bits	Y		25 Pulses	6BH	XX	0001H–0003H	1, 3
Verify Lock Bits	Y	Y	High	2BH	Data	0000H	4
Program Encryption Array	Y		25 Pulses	6CH	Data	0000H–007FH	1
Verify Signature Bytes	Y	Y	High	29H	Data	0030H, 0031H, 0060H	

NOTES:
1. The PROG# pulse waveform is shown in Figure 19.
2. Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.
3. When programming the lock bits, the data bits on port 2 are don't care. Identify the lock bits with the address as follows: LB3 - 0003H, LB2 - 0002H, LB1 - 0001H.
4. The three lock bits are verified in a single operation. The states of the lock bits appear simultaneously at port 2 as follows: LB3 - P2.3, LB2 - P2.2. LB1 - P2.1. High = programmed.

UCONFIG0 Address FFF8H

7							0
—	WSA1#	WSA0#	XALE#	—	—	PAGE#	—

Bit Number	Bit Mnemonic	Function
7	—	Reserved
6:5	WSA1# WSA0# (see Note)	Wait State Select for external code WSA1# WSA0# Description 1 1 No wait states 1 0 Insert 1 wait state 0 1 Insert 2 wait states 0 0 Insert 3 wait states
4	XALE#	Extend Ale: If this bit is set, the time of the ALE pulse is T_{OSC}. Clearing this bit extends the time of the ALE pulse from T_{OSC} to $3T_{OSC}$, which adds one external wait state.
1	PAGE#	Page Mode Select: Clear this bit for page-mode (A15:8/D7:0 on P2, and A7:0 on P0). Set this bit for nonpage-mode (A15:8 on P2, and A7:0/D7:0 on P0 (compatible with MCS 51 microcontrollers)).

NOTE:
Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.

Figure 17. Configuration Byte 0

UCONFIG1 Address FFF9H

7							0
—	—	—	—	—	WSB1#	WSB0#	—

Bit Number	Bit Mnemonic	Function
7:5	—	Reserved; set these bits when writing to UCONFIG1.
2:1	WSB1#, WSB0#	Wait States for external data

WSB1#	WSB0#	Description
1	1	No wait states
1	0	Insert 1 wait state
0	1	Insert 2 wait states
0	0	Insert 3 wait states

NOTE:
Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.

Figure 18. Configuration Byte 1

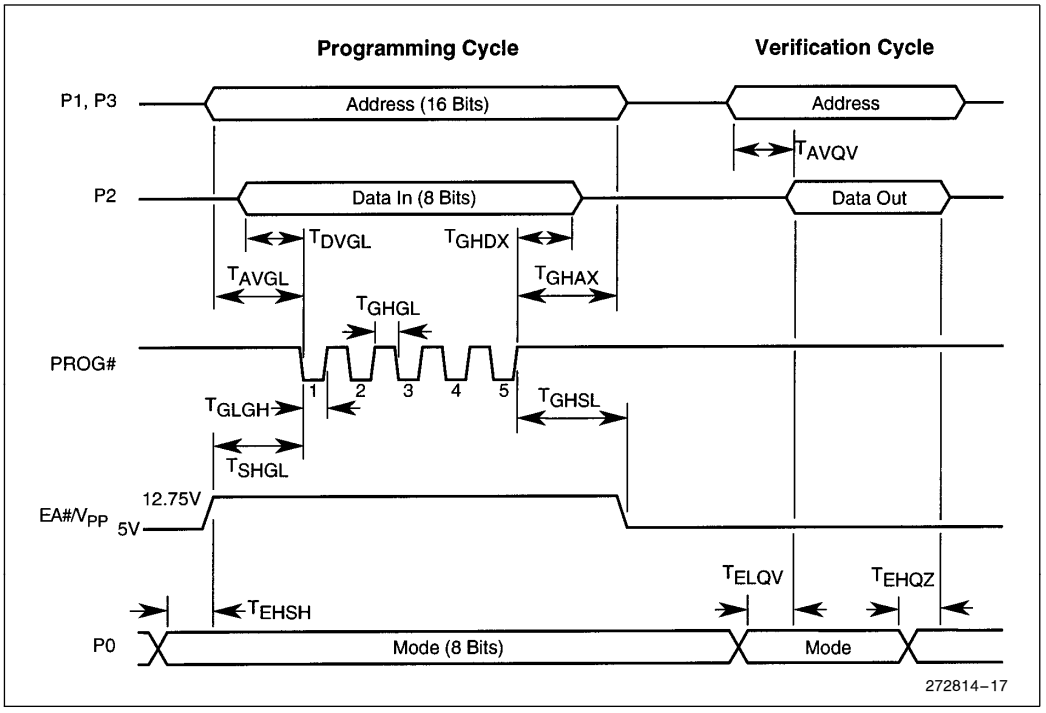


Figure 19. Timing for Programming and Verification of Nonvolatile Memory

Table 13. Nonvolatile Memory Programming and Verification Characteristics at T_A = 21 − 27°C, V_{CC} = 5V, and V_{SS} = 0V

Symbol	Definition	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.5	D.C. Volts
I_{PP}	Programming Supply Current		75	mA
F_{OSC}	Oscillator Frequency	4.0	6.0	MHz
T_{AVGL}	Address Setup to PROG# Low	$48T_{OSC}$		
T_{GHAX}	Address Hold after PROG#	$48T_{OSC}$		
T_{DVGL}	Data Setup to PROG# Low	$48T_{OSC}$		
T_{GHDX}	Data Hold after PROG#	$48T_{OSC}$		
T_{EHSH}	ENABLE High to V_{PP}	$48T_{OSC}$		
T_{SHGL}	V_{PP} Setup to PROG# Low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{GLGH}	PROG# Width	90	110	µs
T_{AVQV}	Address to Data Valid		$48T_{OSC}$	
T_{ELQV}	ENABLE Low to Data Valid		$48To_{SC}$	
T_{EHQZ}	Data Float after ENABLE	0	$48T_{OSC}$	
T_{GHGL}	PROG# High to PROG# Low	10		µs

NOTE:
Notation for timing parameters:

A = Address D = Data E = Enable G = PROG# H = High L = Low
Q = Data out S = Supply (V_{PP}) V = Valid X = No Longer Valid Z = Floating

Table 14. Contents of the Signature Bytes

ADDRESS	CONTENTS	DEVICE TYPE
30H	89H	Indicates Intel Devices
31H	48H	Indicates MCS 151 core product
60H	7BH	Indicates 83C151SB device
60H	FBH	Indicates 87C151SB device
60H	7AH	Indicates 83C151SA device
60H	FAH	Indicates 87C151SA device